

## TPS74801-Q1 具有可编程软启动功能的汽车级 1.5A 低压降线性稳压器

### 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 +125°C， $T_A$
- $V_{OUT}$  范围：0.8V 至 3.6V
- 超低  $V_{IN}$  范围：0.8V 至 5.5V
- $V_{BIAS}$  范围：2.7V 至 5.5V
- 低压降：1.5A、 $V_{BIAS} = 5V$  下的典型值为 60mV
- 电源正常 (PG) 输出可实现电源监视或为其他电源提供时序信号
- 线路、负载和温度范围内的精度为 2%
- 可编程软启动可提供线性电压启动
- $V_{BIAS}$  支持低  $V_{IN}$  运行，具有良好的瞬态响应
- 任何输出电容器  $\geq 2.2 \mu F$  时保持稳定
- 提供小型 3mm × 3mm × 1mm VSON-10 封装和 5mm × 5mm VQFN-20 封装

### 2 应用

- 远程信息处理控制单元
- 信息娱乐系统与仪表组
- 汽车音响主机
- 中距和短距雷达

### 3 说明

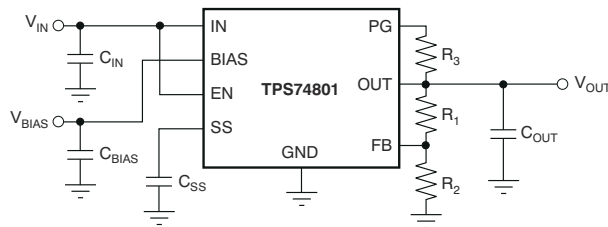
TPS74801-Q1 低压降 (LDO) 线性稳压器可面向多种应用提供易于使用的稳健型电源管理解决方案。用户可编程软启动通过减少启动时的电容涌入电流，更大幅度地减少了输入电源上的应力。软启动具有单调性，旨在为各类处理器和 ASIC 供电。借助使能输入和电源正常输出，可通过外部稳压器轻松实现上电排序。凭借全方位的灵活性，该器件可为 FPGA、DSP 等具有特殊启动要求的应用配置可满足其时序要求的解决方案。

具有精密基准的误差放大器可在整个负载、线路、温度和过程范围内提供 2% 精度。该器件对于大于或等于 2.2  $\mu F$  的任何类型的输出电容器均能保持稳定运行，对于新芯片，额定工作温度范围为  $T_J = -40^\circ C$  至 +150°C；对于 DRC 封装，额定工作温度范围为  $T_J = -40^\circ C$  至 +105°C；对于 RGW 封装，额定工作温度范围为  $T_J = -40^\circ C$  至 +125°C。TPS74801-Q1 采用小型 3mm x 3mm VSON-10 封装，从而生成一个高度紧凑的总体解决方案尺寸。该器件还提供 5mm x 5mm VQFN-20 封装。

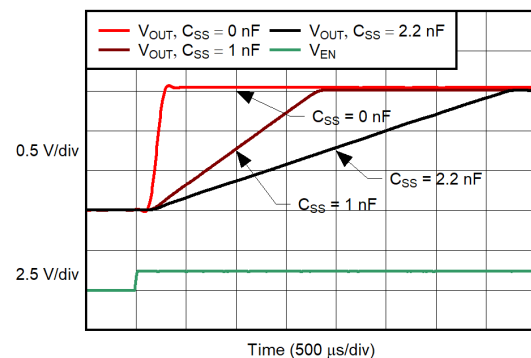
#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
TPS74801-Q1	DRC ( VSON , 10 )	3mm × 3mm
	RGW ( VQFN , 20 )	5mm × 5mm

- 如需更多信息，请参阅 [机械、封装和可订购信息](#)。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



典型应用电路 (可调节)



导通响应



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## 4 Pin Configuration and Functions

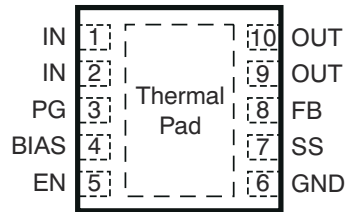


图 4-1. DRC Package, 10-Pin VSON With Exposed Thermal Pad (Top View)

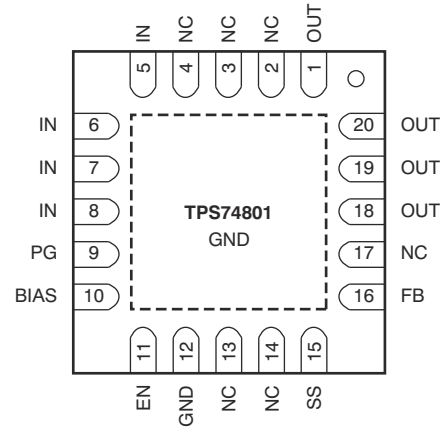


图 4-2. RGW Package, 20-Pin VQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

NAME	PIN NO.		TYPE	DESCRIPTION
	DRC (VSON)	RGW (VQFN)		
BIAS	4	10	I	Bias input voltage for error amplifier, reference, and internal control circuits.
EN	5	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
FB	8	16	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	6	12	—	Ground
IN	1, 2	5-8	I	Input to the device.
NC	N/A	2-4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	9, 10	1, 18-20	O	Regulated output voltage. A small capacitor (total typical capacitance $\geq 2.2 \mu\text{F}$ , ceramic) is needed from this pin to ground to provide stability.
PG	3	9	O	Power-good pin. An open-drain, active-high output that indicates the status of $V_{\text{OUT}}$ . When $V_{\text{OUT}}$ exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When $V_{\text{OUT}}$ is below this threshold the pin is driven to a low-impedance state. Connect a pullup resistor from 10 k $\Omega$ to 1 M $\Omega$ from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
SS	7	15	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 $\mu\text{s}$ .
Thermal Pad			—	Solder the thermal pad to the ground plane for increased thermal performance.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN}, V_{BIAS}$	Input voltage	- 0.3	6	V
$V_{EN}$	Enable voltage	- 0.3	6	V
$V_{PG}$	Power-good voltage	- 0.3	6	V
$I_{PG}$	PG sink current	0	1.5	mA
$V_{SS}$	Soft-start voltage	- 0.3	6	V
$V_{FB}$	Feedback voltage	- 0.3	6	V
$V_{OUT}$	Output voltage	- 0.3	$V_{IN} + 0.3$	V
$I_{OUT}$	Output current	Internally limited		
$I_{CL}$	Output short-circuit duration	Indefinite		
$P_{DISS}$	Continuous total power dissipation	See Thermal Information		
$T_J$	Junction temperature	- 40	150	°C
$T_{stg}$	Storage temperature	- 55	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC specification Q100-011	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input supply voltage	$V_{OUT} + V_{DO}$ ( $V_{IN}$ )	$V_{OUT} + 0.3$	5.5	V
$V_{EN}$	Enable supply voltage		$V_{IN}$	5.5	V
$V_{BIAS}$ <sup>(1)</sup>	Bias supply voltage	$V_{OUT} + V_{DO}$ ( $V_{BIAS}$ ) <sup>(2)</sup>	$V_{OUT} + 1.6$ <sup>(2)</sup>	5.5	V
$V_{OUT}$	Output voltage	0.8		3.6	V
$I_{OUT}$	Output current	0		1.5	A
$C_{OUT}$	Output capacitor	2.2			µF
$C_{IN}$	Input capacitor <sup>(3)</sup>	1			µF
$C_{BIAS}$	Bias capacitor	0.1	1		µF
$T_J$	Operating junction temperature	- 40		150	°C

- (1) BIAS supply is required when  $V_{IN}$  is below  $V_{OUT} + 1.62$  V.  
(2)  $V_{BIAS}$  has a minimum voltage of 2.7 V or  $V_{OUT} + V_{DO}$  ( $V_{BIAS}$ ), whichever is higher.  
(3) If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS74801-Q1				UNIT
		RGW (VQFN) (legacy chip)	RGW (VQFN) (new chip)	DRC (VSON) (legacy chip)	DRC (VSON) (new chip)	
		20 PINS	20 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.6	34.7	44.2	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.3	31	50.3	63.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	13.5	19.6	19.5	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	0.4	1.4	0.7	4.2	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	15.2	13.5	17.8	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	3.6	4.3	3.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

## 5.5 Electrical Characteristics

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\ \mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\ \mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (DRC),  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (RGW) and  $T_J = -40$  to  $150^\circ\text{C}$  (New Chip) (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF}$	Internal reference (Adj.)	$T_A = 25^\circ\text{C}$	0.796	0.8	0.804	V
$V_{OUT}$	Output voltage range	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 1.5\text{ A}$	$V_{REF}$		3.6	V
	Accuracy <sup>(1)</sup>	$2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$ (legacy chip)	-2	$\pm 0.5$	2	%
$2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$ (new chip)		-1.35	$\pm 0.3$	1.35		
$\Delta V_{OUT} (\Delta V_{IN})$	Line regulation	$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (legacy chip)		0.03		%/V
		$V_{OUT(nom)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$ (new chip)		0.001		
$\Delta V_{OUT} (\Delta I_{OUT})$	Load regulation	$50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$		0.09		%/A
$V_{DO}$	$V_{IN}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 3.25\text{ V}$ (legacy chip) <sup>(3)</sup>		60	165	mV
		$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 3.25\text{ V}$ (DRC: new chip) <sup>(3)</sup>		50	100	
		$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(nom)} \geq 3.25\text{ V}$ (RGW: new chip) <sup>(3)</sup>		50	110	
	$V_{BIAS}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (legacy chip)		1.31	1.6	V
$I_{OUT} = 1.5\text{ A}$ , $V_{IN} = V_{BIAS}$ (new chip)			1.31	1.43		
$I_{CL}$	Output current limit	$V_{OUT} = 80\% \times V_{OUT(nom)}$	2		5.5	A
$I_{BIAS}$	BIAS pin current	(Legacy chip)		1	2	mA
		(New chip)		1	1.2	
$I_{SHDN}$	Shutdown supply current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{ V}$ (legacy chip)		1	50	$\mu\text{A}$
$I_{SHDN}$ (smart enable)		$V_{EN} \leq 0.4\text{ V}$ (new chip)		0.85	10	
$I_{FB}$	Feedback pin current	(Legacy chip)	-1	0.15	1	$\mu\text{A}$
		(New chip)	-30	0.15	30	nA
PSRR	Power-supply rejection ( $V_{IN}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (legacy chip)		60		dB
		1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (new chip)		69		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (legacy chip)		30		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (new chip)		49		
	Power-supply rejection ( $V_{BIAS}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (legacy chip)		50		dB
		1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (new chip)		59		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (legacy chip)		30		
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$ (new chip)		50		
$V_n$	Output noise voltage	BW = 100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (legacy chip)		$25 \times V_{OUT}$		$\mu\text{V}_{rms}$
		BW = 100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$ , $C_{SS} = 1\text{ nF}$ (new chip)		$20 \times V_{OUT}$		

## 5.5 Electrical Characteristics (续)

at  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\ \mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\ \mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (DRC),  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (RGW) and  $T_J = -40$  to  $150^\circ\text{C}$  (New Chip) (unless otherwise noted); typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{STR}$	Minimum startup time	$R_{LOAD}$ for $I_{OUT} = 1.0\text{ A}$ , $C_{SS} = \text{open}$ (legacy chip)		200		$\mu\text{s}$
		$R_{LOAD}$ for $I_{OUT} = 1.0\text{ A}$ , $C_{SS} = \text{open}$ (new chip)		250		
$I_{SS}$	Soft-start charging current	$V_{SS} = 0.4\text{ V}$ (legacy chip)		440		nA
		$V_{SS} = 0.4\text{ V}$ (new chip)		530		
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis	(Legacy chip)		50		mV
		(New chip)		55		
$V_{EN(dg)}$	Enable pin deglitch time			20		$\mu\text{s}$
$I_{EN}$	Enable pin current	$V_{EN} = 5\text{ V}$ (legacy chip)		0.1	1	$\mu\text{A}$
		$V_{EN} = 5\text{ V}$ (new chip)		0.1	0.3	
$V_{IT}$	PG trip threshold	$V_{OUT}$ decreasing	85	90	94	$\%V_{OUT}$
$V_{HYS}$	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$ (legacy chip)			0.3	V
		$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$ (new chip)			0.125	
$I_{PG(lkg)}$	PG leakage current	$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$ (legacy chip)		0.1	1	$\mu\text{A}$
		$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$ (new chip)		0.001	0.05	
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^\circ\text{C}$
		Reset, temperature decreasing		140		
$R_{PULLDOWN}$		$V_{BIAS} = 5\text{ V}$ , $V_{EN} = 0\text{ V}$		0.83		$\text{k}\Omega$

- (1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
- (2) Dropout is defined as the voltage from  $V_{IN}$  to  $V_{OUT}$  when  $V_{OUT}$  is 3% below nominal.
- (3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6-6.

### 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

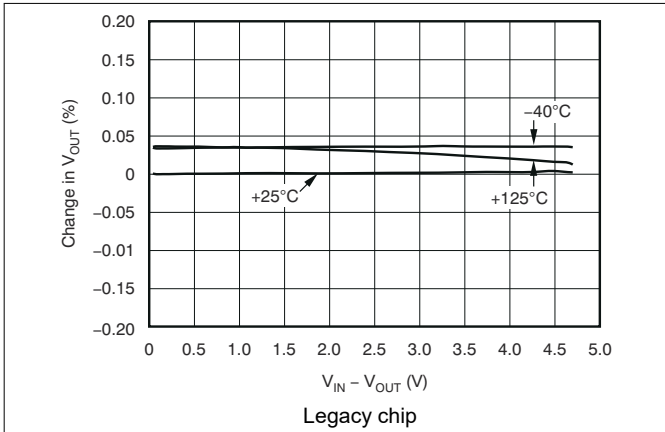


图 5-1.  $V_{IN}$  Line Regulation

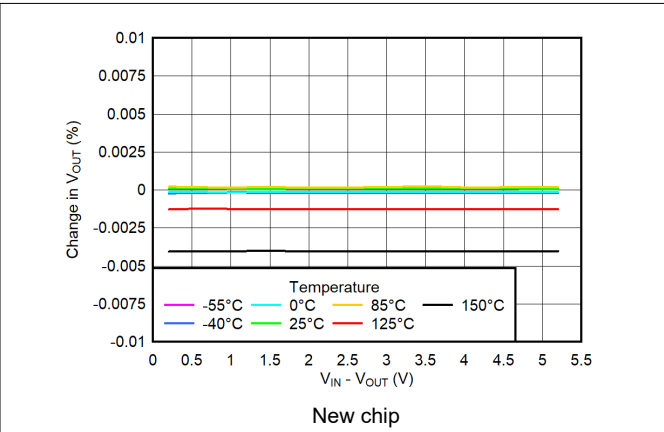


图 5-2.  $V_{IN}$  Line Regulation

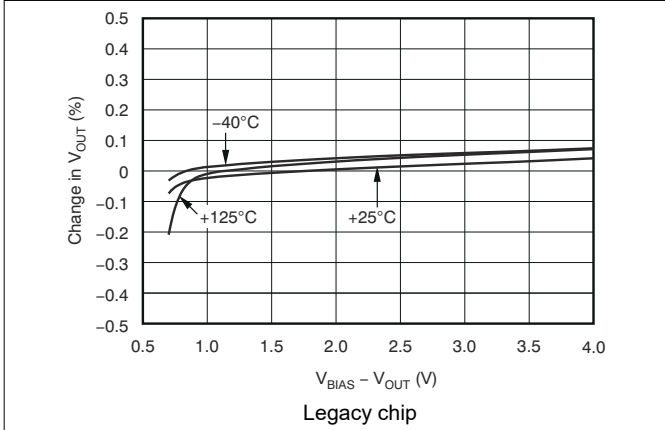


图 5-3.  $V_{BIAS}$  Line Regulation

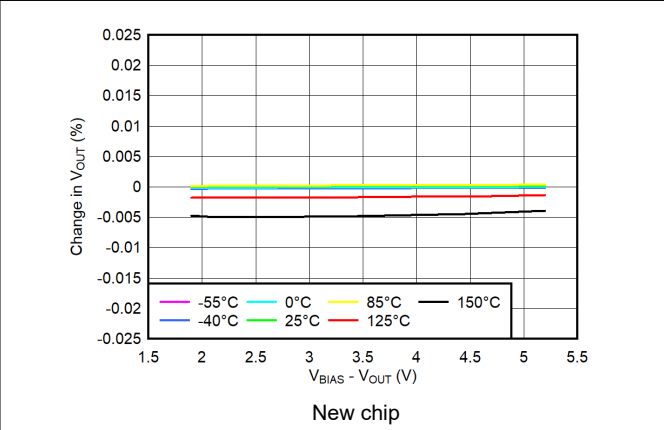


图 5-4.  $V_{BIAS}$  Line Regulation

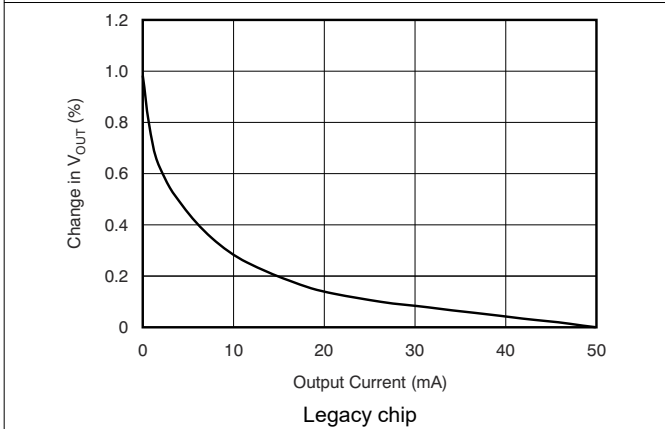


图 5-5. Load Regulation at Light Load

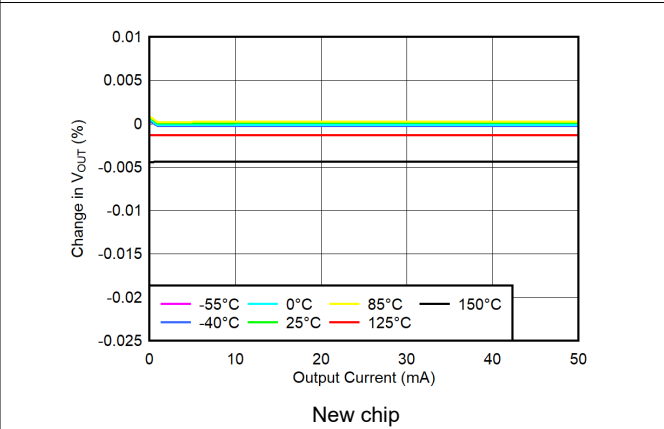


图 5-6. Load Regulation at Light Load



### 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

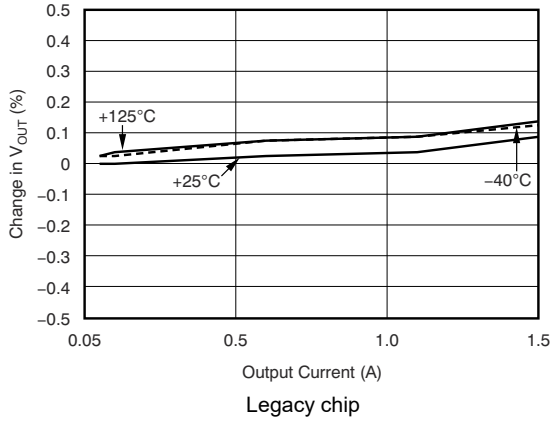


图 5-7. Load Regulation

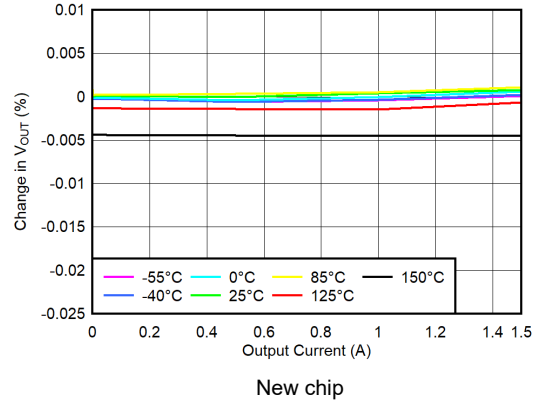


图 5-8. Load Regulation

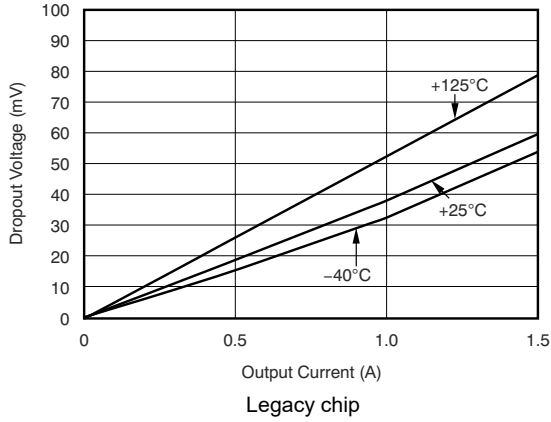


图 5-9.  $V_{IN}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

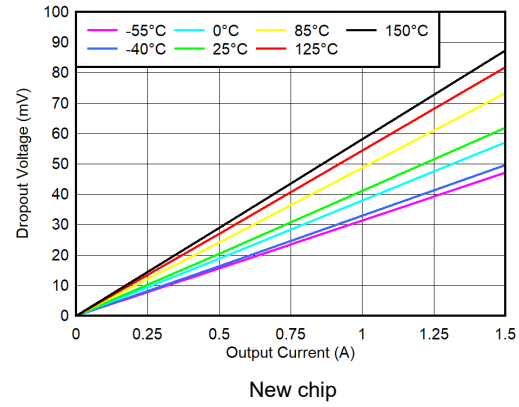


图 5-10.  $V_{IN}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

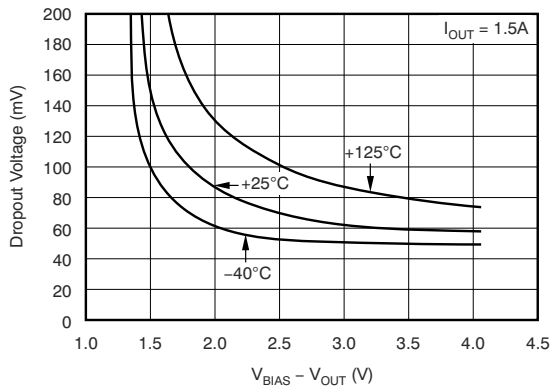


图 5-11.  $V_{IN}$  Dropout Voltage vs  $(V_{BIAS} - V_{OUT})$  and Temperature ( $T_A$ )

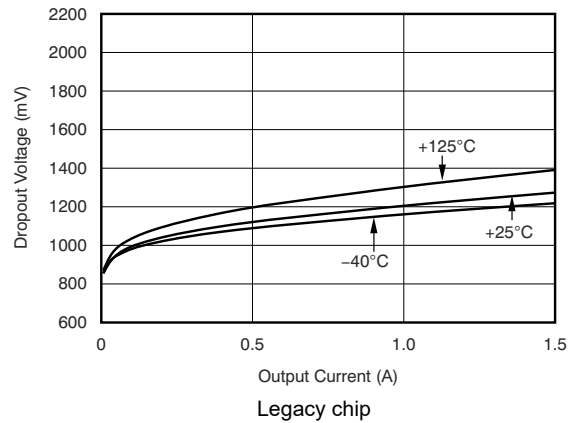
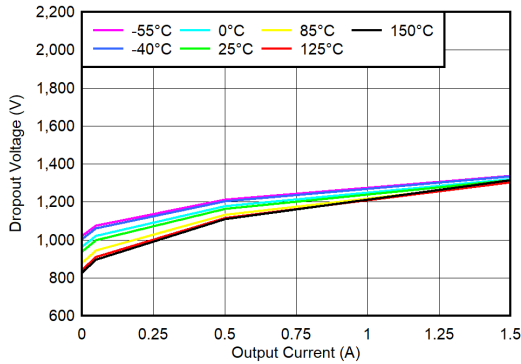


图 5-12.  $V_{BIAS}$  Dropout Voltage vs  $I_{OUT}$  and Temperature ( $T_J$ )

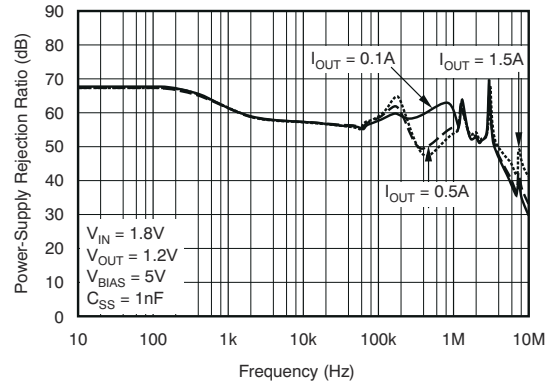
### 5.6 Typical Characteristics: I<sub>OUT</sub> = 50 mA (continued)

at T<sub>J</sub> = 25°C, V<sub>IN</sub> = V<sub>OUT(nom)</sub> + 0.3 V, V<sub>BIAS</sub> = 5 V, I<sub>OUT</sub> = 50 mA, V<sub>EN</sub> = V<sub>IN</sub>, C<sub>IN</sub> = 1 μF, C<sub>BIAS</sub> = 4.7 μF, and C<sub>OUT</sub> = 10 μF (unless otherwise noted)



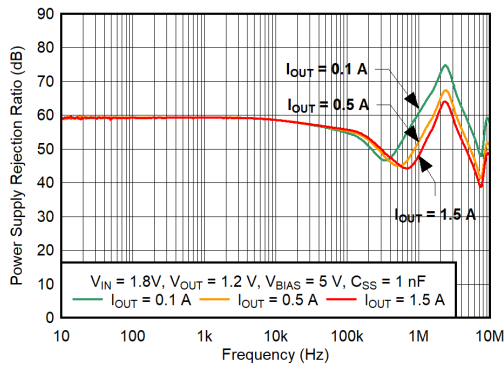
New chip

图 5-13. V<sub>BIAS</sub> Dropout Voltage vs I<sub>OUT</sub> and Temperature (T<sub>J</sub>)



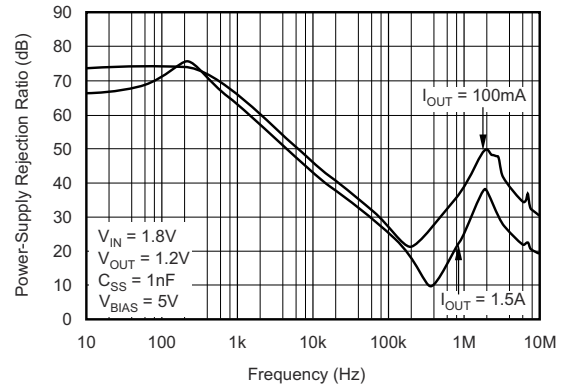
Legacy chip

图 5-14. V<sub>BIAS</sub> PSRR vs Frequency



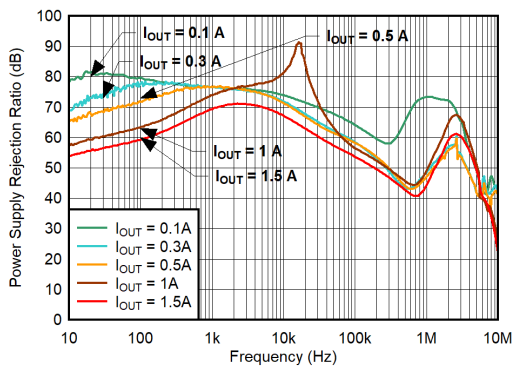
New chip

图 5-15. V<sub>BIAS</sub> PSRR vs Frequency



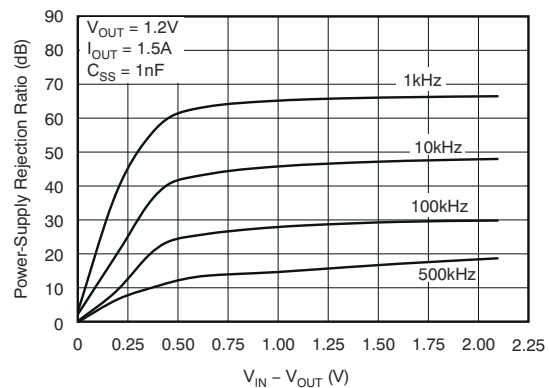
Legacy chip

图 5-16. V<sub>IN</sub> PSRR vs Frequency



New chip

图 5-17. V<sub>IN</sub> PSRR vs Frequency



Legacy chip

图 5-18. V<sub>IN</sub> PSRR vs (V<sub>IN</sub> - V<sub>OUT</sub>)

### 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

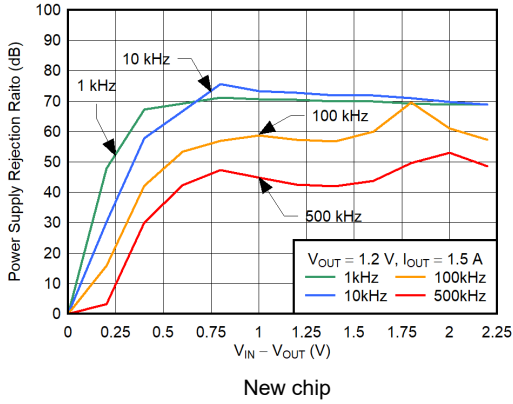


图 5-19.  $V_{IN}$  PSRR vs  $(V_{IN} - V_{OUT})$

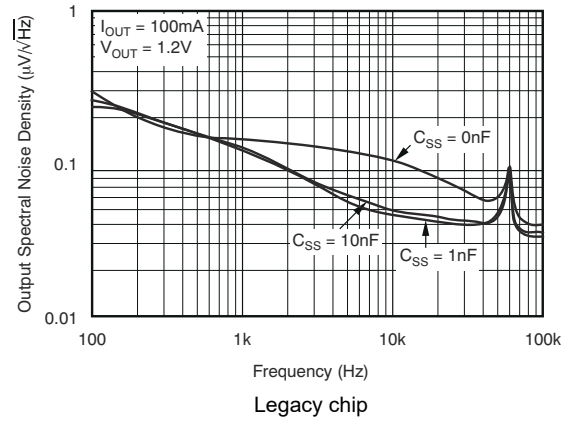


图 5-20. Noise Spectral Density

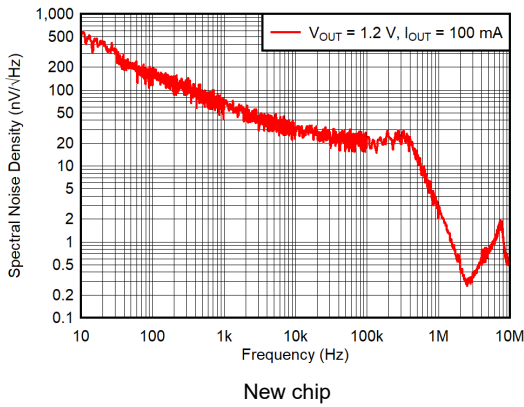


图 5-21. Noise Spectral Density

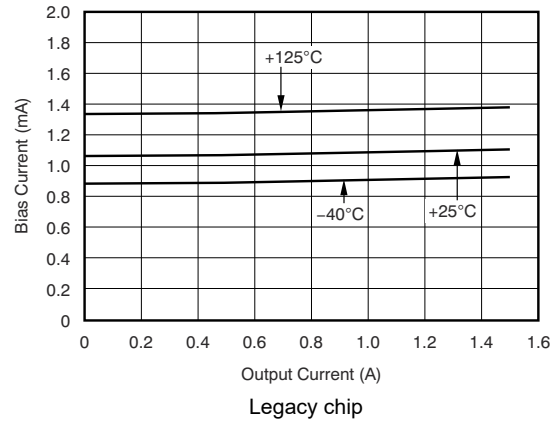


图 5-22. BIAS Pin Current vs Output Current and Temperature ( $T_J$ )

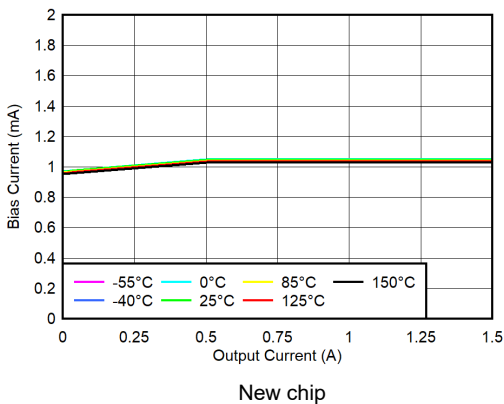


图 5-23. BIAS Pin Current vs Output Current and Temperature ( $T_J$ )

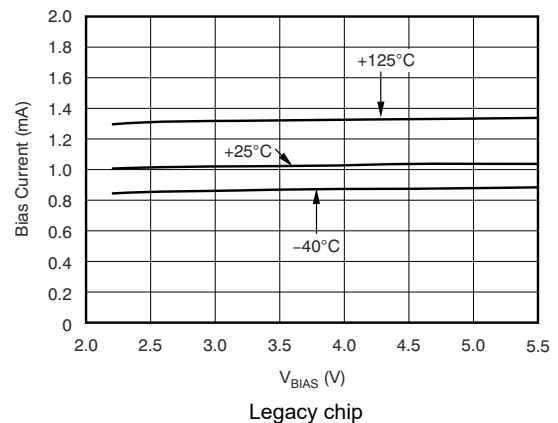


图 5-24. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

### 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

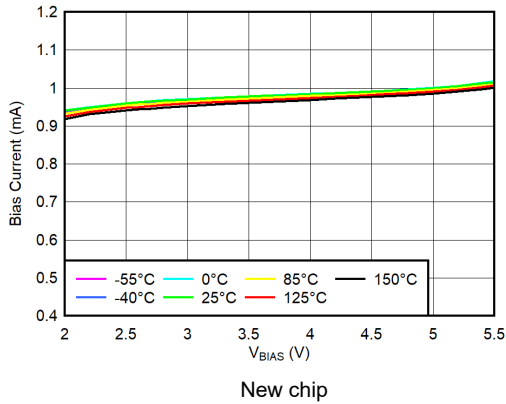


图 5-25. BIAS Pin Current vs  $V_{BIAS}$  and Temperature ( $T_J$ )

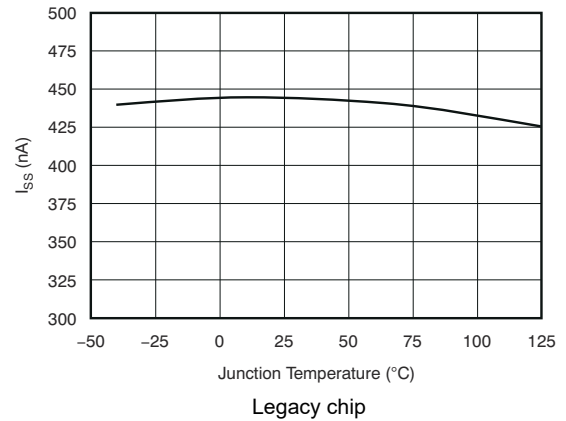


图 5-26. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

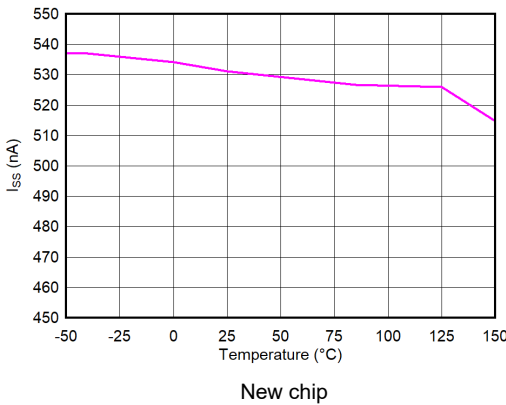


图 5-27. Soft-Start Charging Current ( $I_{SS}$ ) vs Temperature ( $T_J$ )

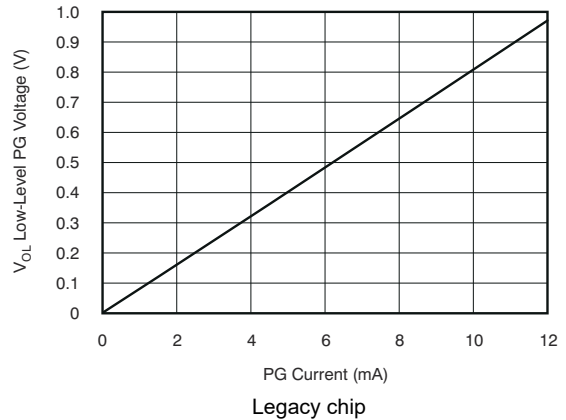


图 5-28. Low-Level PG Voltage vs Current

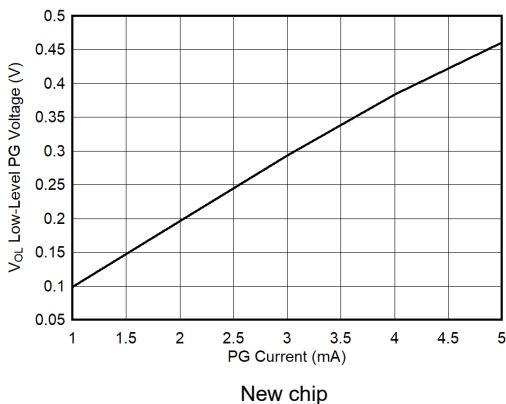


图 5-29. Low-Level PG Voltage vs Current

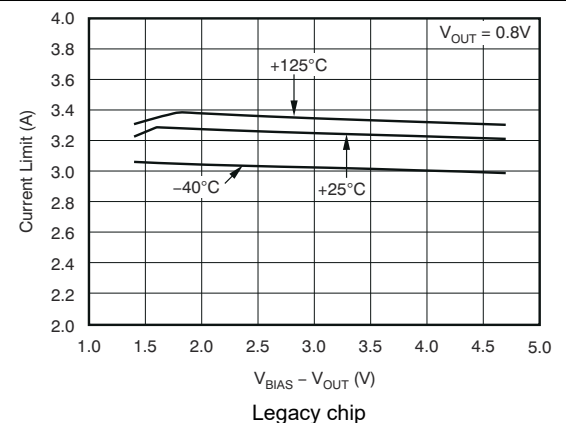


图 5-30. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

### 5.6 Typical Characteristics: $I_{OUT} = 50 \text{ mA}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3 \text{ V}$ ,  $V_{BIAS} = 5 \text{ V}$ ,  $I_{OUT} = 50 \text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1 \mu\text{F}$ ,  $C_{BIAS} = 4.7 \mu\text{F}$ , and  $C_{OUT} = 10 \mu\text{F}$  (unless otherwise noted)

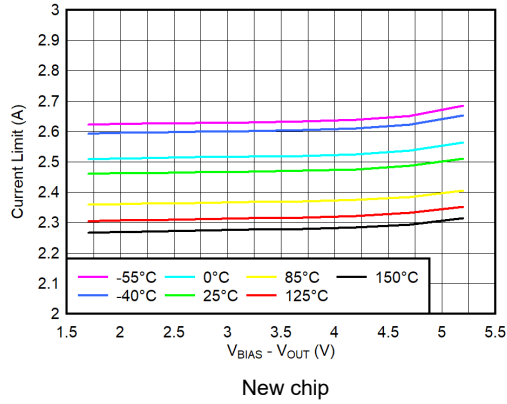


图 5-31. Current Limit vs ( $V_{BIAS} - V_{OUT}$ )

### 5.7 Typical Characteristics: I<sub>OUT</sub> = 1 A

at T<sub>J</sub> = 25°C, V<sub>IN</sub> = V<sub>OUT(nom)</sub> + 0.3 V, V<sub>BIAS</sub> = 5 V, I<sub>OUT</sub> = 1 A, V<sub>EN</sub> = V<sub>IN</sub> = 1.8 V, V<sub>OUT</sub> = 1.5 V, C<sub>IN</sub> = 1 μF, C<sub>BIAS</sub> = 4.7 μF, and C<sub>OUT</sub> = 10 μF (unless otherwise noted)

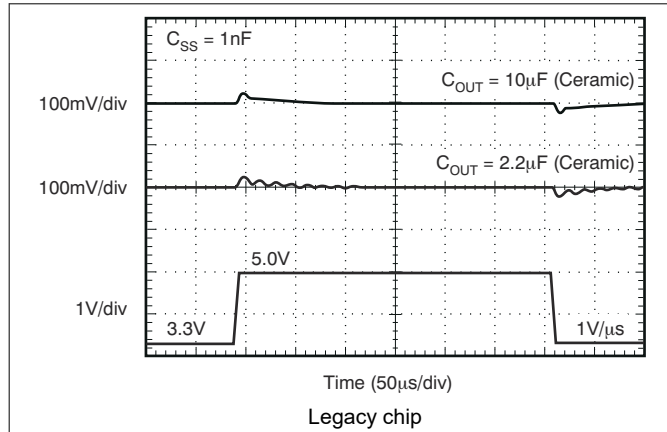


图 5-32. V<sub>BIAS</sub> Line Transient

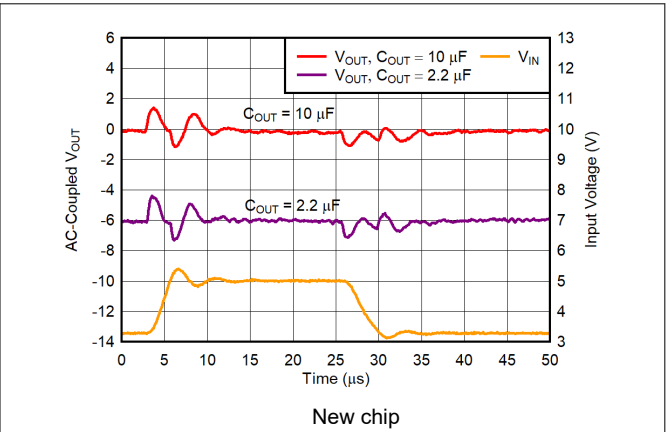


图 5-33. V<sub>BIAS</sub> Line Transient

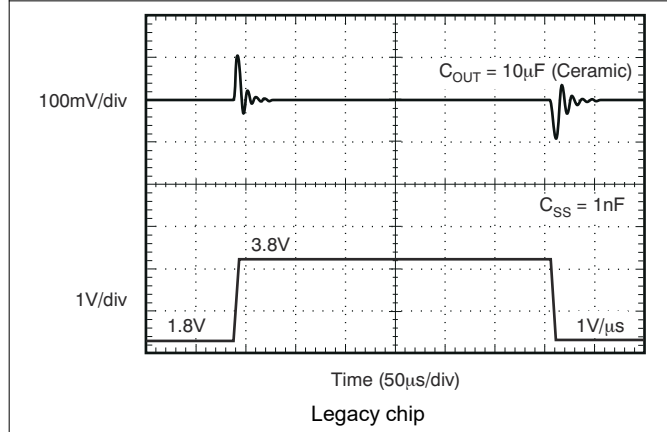


图 5-34. V<sub>IN</sub> Line Transient

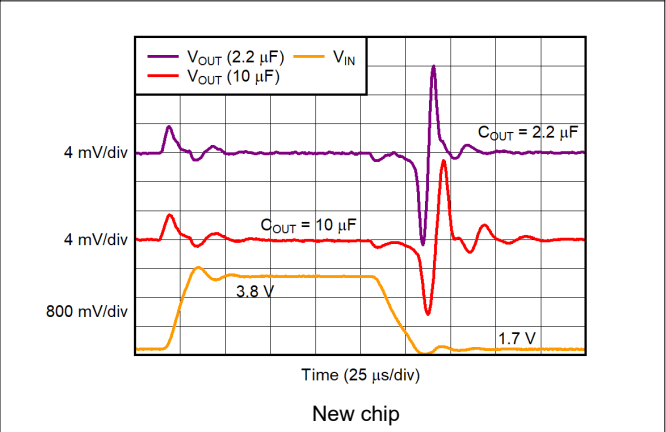


图 5-35. V<sub>IN</sub> Line Transient

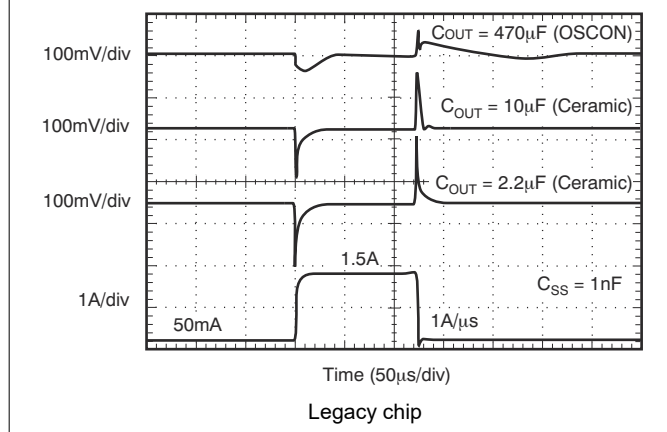


图 5-36. Output Load Transient Response

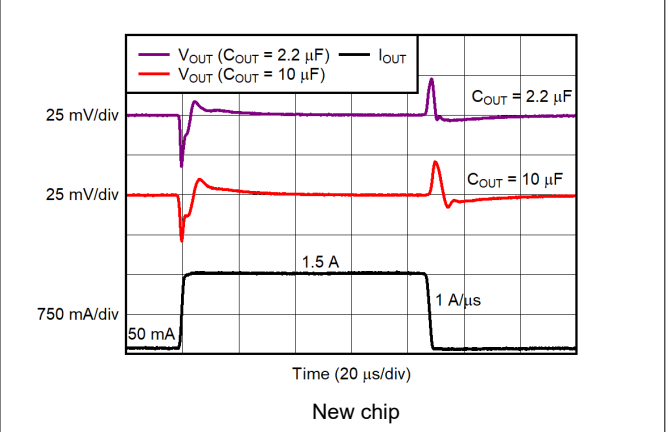


图 5-37. Output Load Transient Response

### 5.7 Typical Characteristics: $I_{OUT} = 1\text{ A}$ (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 4.7\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$  (unless otherwise noted)

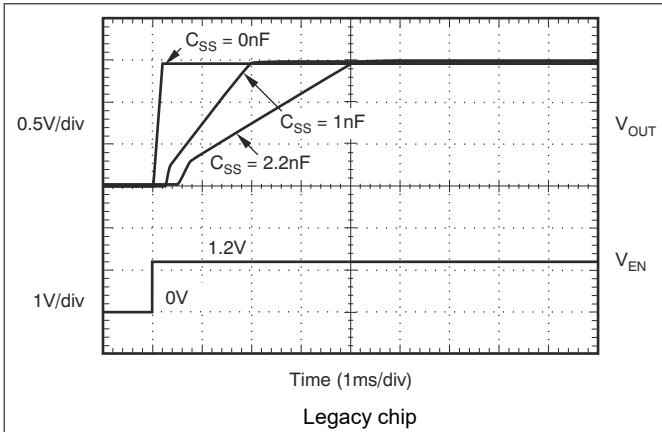


图 5-38. Turn-On Response

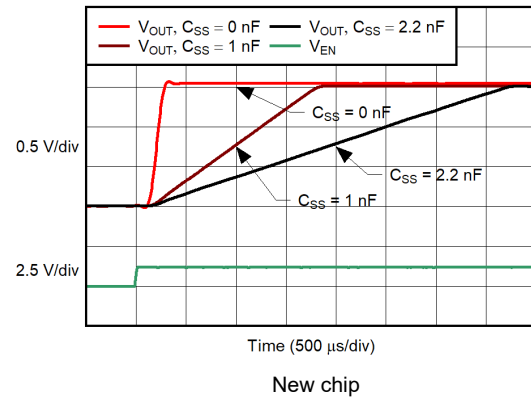


图 5-39. Turn-On Response

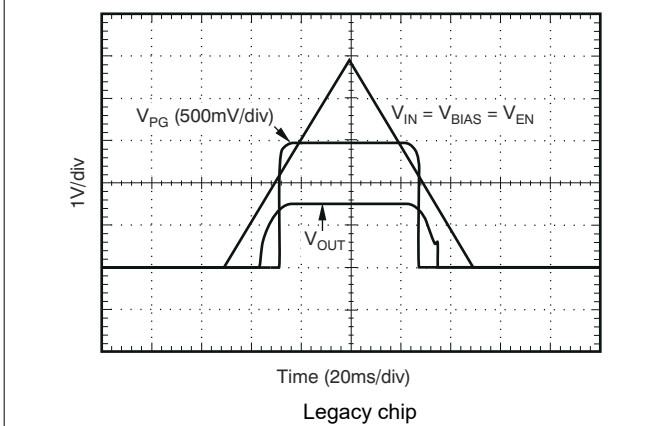


图 5-40. Power-Up, Power-Down

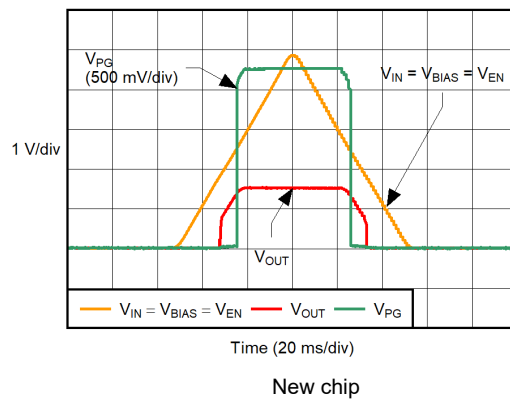


图 5-41. Power-Up, Power-Down

## 6 Detailed Description

### 6.1 Overview

The TPS748 is a low-dropout regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS-pass transistor to regulate very low input and output voltages. Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74801-Q1 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low  $V_{\text{IN}}$  applications. The TPS74801-Q1 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

### 6.2 Functional Block Diagrams

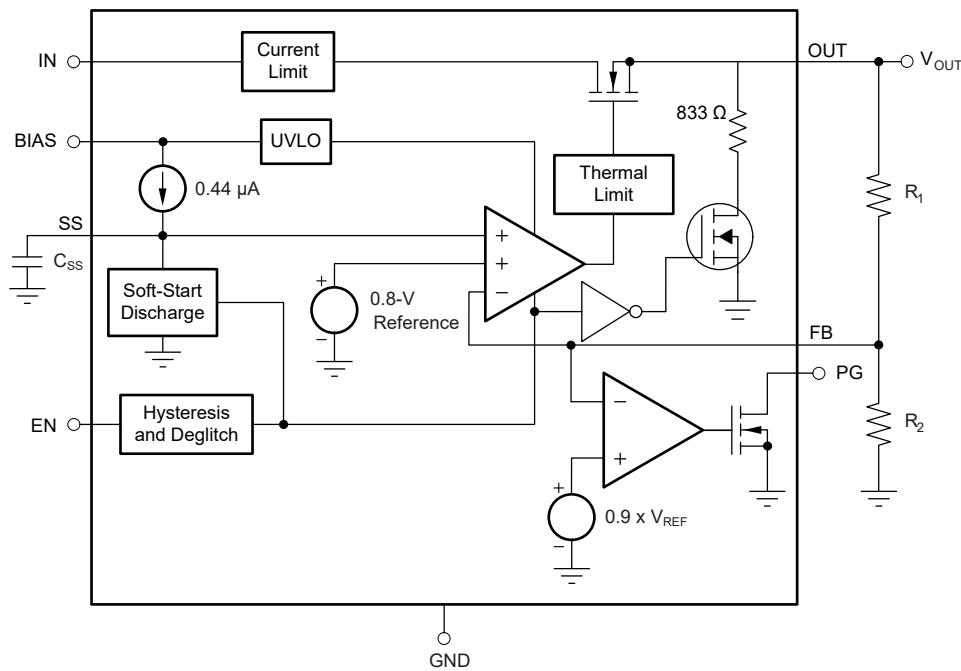


图 6-1. Legacy Chip Functional Block Diagram



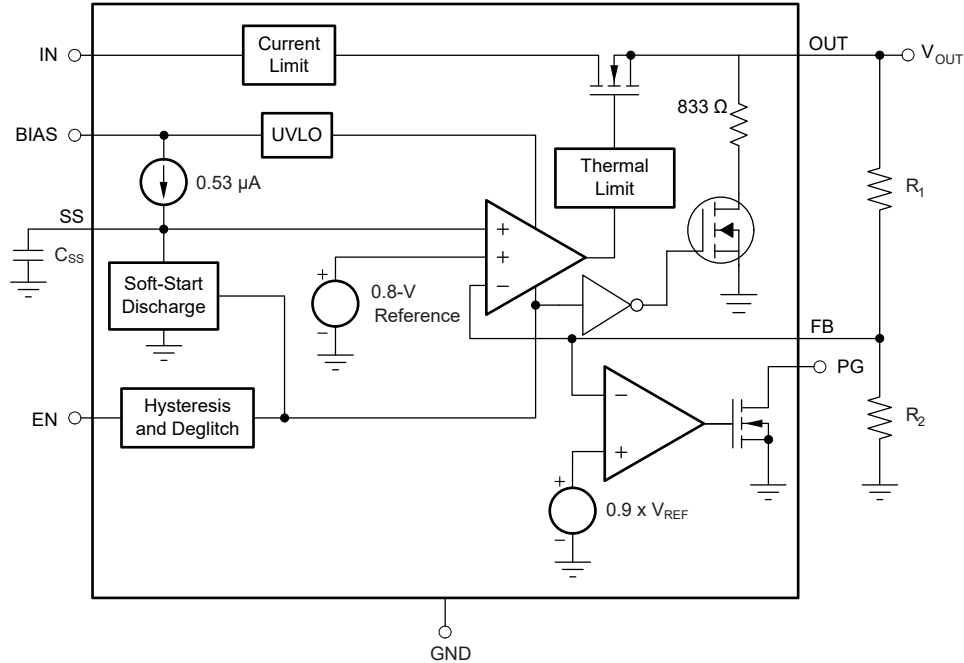


图 6-2. New Chip Functional Block Diagram

## 6.3 Feature Description

### 6.3.1 Programmable Soft-Start

The TPS74801-Q1 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{SS}$ ). This feature is important for many applications because soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74801-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ( $I_{SS}$ ), soft-start capacitance ( $C_{SS}$ ), and the internal reference voltage ( $V_{REF}$ ), and can be calculated using 方程式 1:

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit ( $I_{CL}$ ) and the output capacitor can set the start-up time. In this case, the start-up time is given by 方程式 2:

$$t_{SSCL} = \frac{V_{OUT(NOM)} \times C_{OUT}}{I_{CL(MIN)}} \quad (2)$$

where:

- $V_{OUT(NOM)}$  is the nominal output voltage
- $C_{OUT}$  is the output capacitance
- $I_{CL(MIN)}$  is the minimum current limit for the device

In applications where monotonic start-up is required, the soft-start time given by 方程式 1 must be set greater than 方程式 2.

The maximum recommended soft-start capacitor is 0.015  $\mu$ F. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015  $\mu$ F can be a problem in applications where the enable pin must be rapidly pulsed while still requiring the device to soft-start from ground.  $C_{SS}$  must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 7-3 for suggested soft-start capacitor values.

### 6.3.2 Sequencing Requirements

$V_{IN}$ ,  $V_{BIAS}$ , and  $V_{EN}$  can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as  $V_{IN}$  is greater than 1.1 V and the ramp rate of  $V_{IN}$  and  $V_{BIAS}$  is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device soft-starts as programmed, provided that  $V_{IN}$  is present before  $V_{BIAS}$ . If  $V_{BIAS}$  and  $V_{EN}$  are present before  $V_{IN}$  is applied and the set soft-start time has expired, then  $V_{OUT}$  tracks  $V_{IN}$ . If the soft-start time has not expired, the output tracks  $V_{IN}$  until  $V_{OUT}$  reaches the value set by the charging soft-start capacitor. 图 6-3 shows the use of an RC-delay circuit to hold off  $V_{EN}$  until  $V_{BIAS}$  has ramped. This technique can also be used to drive EN from  $V_{IN}$ . An external control signal can also be used to enable the device after  $V_{IN}$  and  $V_{BIAS}$  are present.

#### 备注

When  $V_{BIAS}$  and  $V_{EN}$  are present and  $V_{IN}$  is not supplied, this device outputs approximately 50  $\mu$ A of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 k $\Omega$ .

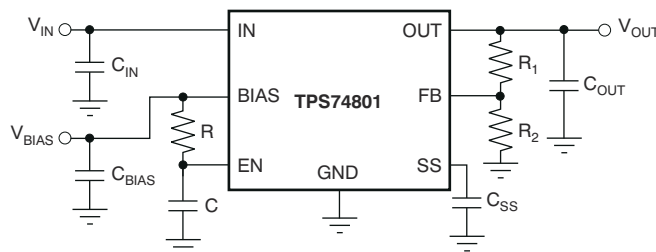


图 6-3. Soft-Start Delay Using an RC Circuit to Enable the Device

### 6.3.3 Output Noise

The TPS74801-Q1 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001- $\mu$ F soft-start capacitor, the output noise is reduced by half and is typically 30- $\mu$ V<sub>RMS</sub> for a 1.2-V output (10 Hz to 100 kHz). Further increasing C<sub>SS</sub> has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The following equations calculate the RMS noise with a 0.001- $\mu$ F soft-start capacitor for the legacy and new chip, respectively:

$$V_N = 25 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \text{ (Legacy Chip)} \quad (3)$$

$$V_N = 20 \left( \frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \text{ (New Chip)} \quad (4)$$

The low output noise of the TPS74801-Q1 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

### 6.3.4 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V<sub>EN</sub> below 0.4 V turns the regulator off, while V<sub>EN</sub> above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74801-Q1 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V<sub>EN</sub> signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately -1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS74801-Q1.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect the EN pin as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

### 6.3.5 Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V<sub>BIAS</sub> in order to have a valid output. The PG output is high-impedance when V<sub>OUT</sub> is greater than V<sub>IT</sub> + V<sub>HYS</sub>. If V<sub>OUT</sub> drops below V<sub>IT</sub> or if V<sub>BIAS</sub> drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 k $\Omega$  to 1 M $\Omega$ . If output voltage monitoring is not needed, the PG pin can be left floating.

### 6.3.6 Internal Current Limit

The TPS74801-Q1 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 2 A and maintain regulation. The current limit responds in approximately 10  $\mu$ s to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS74801-Q1 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74801-Q1 above the rated current degrades device reliability.

### 6.3.7 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, junction temperature must be limited to 150°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 150°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74801-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS74801-Q1 into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

**表 6-1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER				
	$V_{IN}$	$V_{BIAS}$	$V_{EN}$	$I_{OUT}$	$T_J$
Normal mode	$V_{IN} \geq V_{OUT(nom)} + V_{DO(IN)}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

### 6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(nom)} + V_{DO(IN)}$ )
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(nom)} + V_{DO(BIAS)}$ )
- The output current is less than the current limit ( $I_{OUT} < I_{CL}$ )
- The device junction temperature is less than the thermal shutdown temperature ( $T_J < T_{SD(shutdown)}$ )
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state, defined as when the device is in dropout ( $V_{IN} < V_{OUT} + V_{DO(IN)}$  or  $V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$  directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO(IN)}$ ), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

### 6.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than  $V_{IL(EN)}$  (see the [Electrical Characteristics](#) table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Application Information

The TPS74801-Q1 belongs to a family of low dropout regulators that feature soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74801-Q1 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low  $V_{\text{IN}}$  applications.

The TPS74801-Q1 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

### 7.2 Typical Application

图 7-1 shows the typical application circuit for the TPS74801-Q1 adjustable output device.

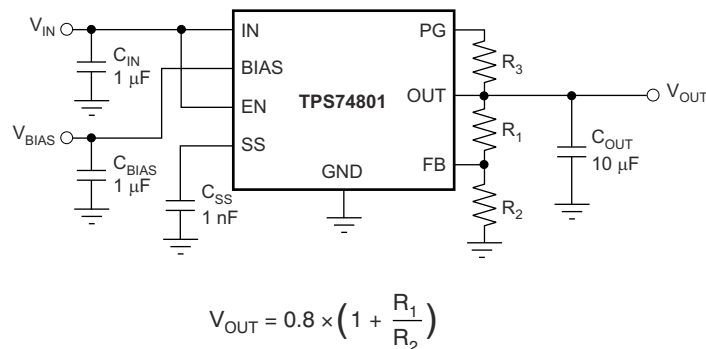


图 7-1. Typical Application Circuit for the TPS74801-Q1 (Adjustable)

#### 7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.1 V, $\pm 3\%$
Bias voltage	5.0 V
Output voltage	1.8 V, $\pm 1\%$
Output current	1.5 A (maximum), 10 mA (minimum)
Start-up time	< 25 ms

### 7.2.2 Detailed Design Procedure

$R_1$  and  $R_2$  can be calculated for any output voltage using the formula shown in 图 7-1. See 表 7-2 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications,  $R_2$  must be  $\leq 4.99 \text{ k}\Omega$ .

**表 7-2. Standard 1% Resistor Values for Programming the Output Voltage (1)**

$R_1$ (k $\Omega$ )	$R_2$ (k $\Omega$ )	$V_{OUT}$ (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1)  $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$ .

**表 7-3. Standard Capacitor Values for Programming the Soft-Start Time (1)**

$C_{SS}$	SOFT-START TIME (Legacy Chip)	SOFT-START TIME (New Chip)
Open	0.1 ms	0.25 ms
270 pF	0.5 ms	0.4 ms
560 pF	1 ms	0.8 ms
2.7 nF	5 ms	4.1 ms
5.6 nF	10 ms	8.5 ms
0.01 $\mu$ F	18 ms	15 ms

(1)  $t_{SS(s)} = 0.8 \times C_{SS}(F) / I_{SS}$ .

#### 7.2.2.1 Input, Output, and Bias Capacitor Requirements

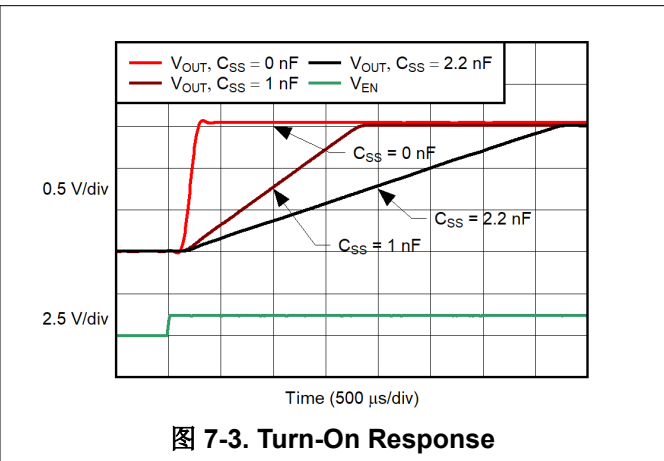
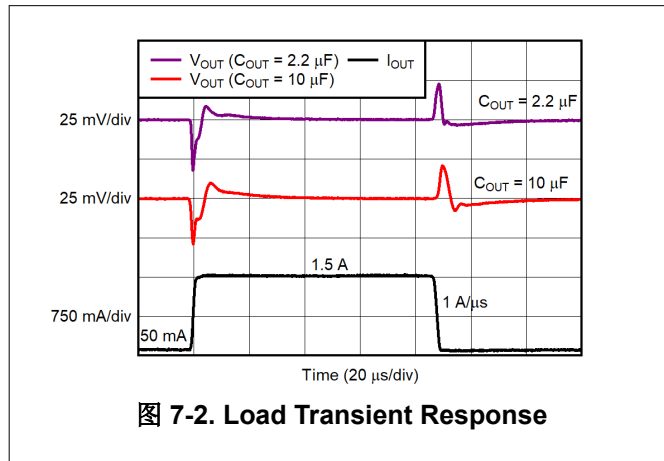
The device is designed to be stable for all available types and values of output capacitors  $\geq 2.2 \mu\text{F}$ . The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for  $V_{IN}$  and  $V_{BIAS}$  is  $1 \mu\text{F}$ . If  $V_{IN}$  and  $V_{BIAS}$  are connected to the same supply, the recommended minimum capacitor for  $V_{BIAS}$  is  $4.7 \mu\text{F}$ . Use good-quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance.

#### 7.2.2.2 Transient Response

The TPS74801-Q1 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see the *Output Load Transient Response* curves in the [Typical Characteristics](#) section. Because the TPS74801-Q1 is stable with output capacitors as low as  $2.2 \mu\text{F}$ , many applications can then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

### 7.2.3 Application Curves



## 7.3 Power Supply Recommendations

The TPS74801-Q1 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.3 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 μF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the BIAS rail with a separate 0.1 μF or larger capacitor. If the IN pin is tied to the BIAS pin, a minimum 4.7-μF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

## 7.4 Layout

### 7.4.1 Layout Guidelines

#### 7.4.1.1 Layout Recommendations and Power Dissipation

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R<sub>1</sub> in 图 7-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and to provide reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using 方程式 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

The primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 方程式 6:



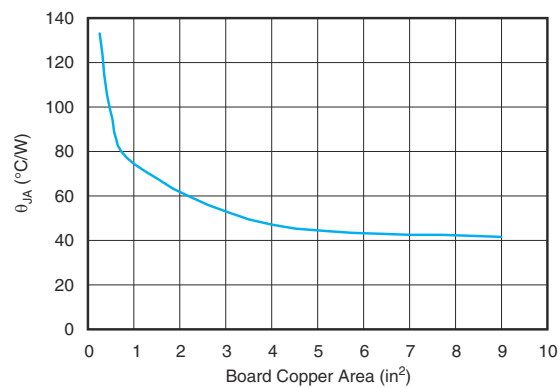
$$R_{\theta JA} = \frac{(150^{\circ}\text{C} - T_A)}{P_D} \quad (6)$$

Knowing the maximum  $R_{\theta JA}$ , the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 图 7-4.

图 7-4 shows the variation of  $R_{\theta JA}$  as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

备注

When the device is mounted on an application PCB, use  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the [Estimating Junction Temperature](#) section.



$R_{\theta JA}$  value at board size of 9 in<sup>2</sup> (that is, 3-in × 3-in) is a JEDEC standard.

图 7-4.  $R_{\theta JA}$  vs Board Size

#### 7.4.1.2 Estimating Junction Temperature

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in 方程式 7). For backwards compatibility, an older  $R_{\theta JC, Top}$  parameter is listed as well.

$$\begin{aligned} \Psi_{JT}: T_J &= T_T + \Psi_{JT} \cdot P_D \\ \Psi_{JB}: T_J &= T_B + \Psi_{JB} \cdot P_D \end{aligned} \quad (7)$$

Where  $P_D$  is the power dissipation shown by 方程式 7,  $T_T$  is the temperature at the center-top of the device package, and  $T_B$  is the PCB temperature measured 1mm away from the device package *on the PCB surface* (see 图 7-6).

备注

Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring  $T_T$  and  $T_B$ , see the [Using New Thermal Metrics application note](#), available for download at [www.ti.com](http://www.ti.com).

In reference to 图 7-5, the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with 方程式 7 is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.

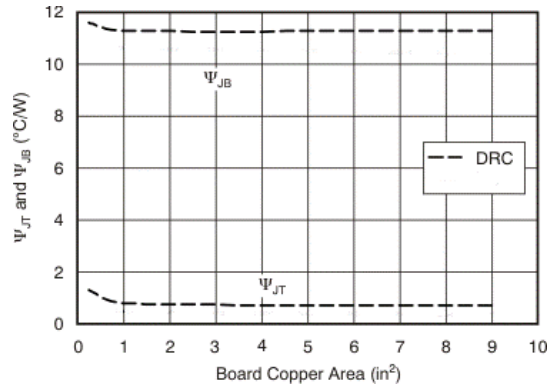
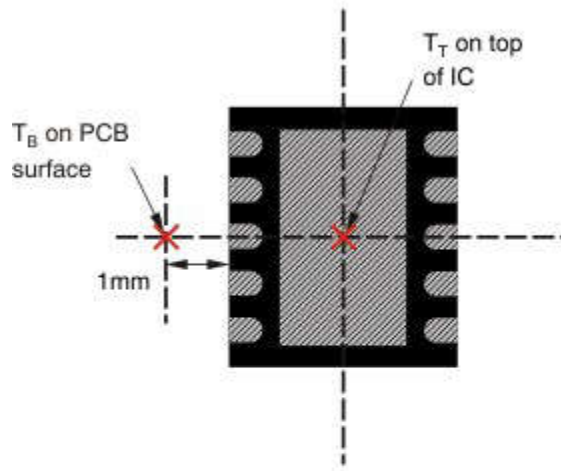


图 7-5.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size

For a more detailed discussion of why TI does not recommend using  $R_{\theta JC(top)}$  to determine thermal characteristics, see the [Using New Thermal Metrics application note](#), available for download at [www.ti.com](http://www.ti.com). For further information, see the [Semiconductor and IC Package Thermal Metrics application note](#), also available on the TI website.

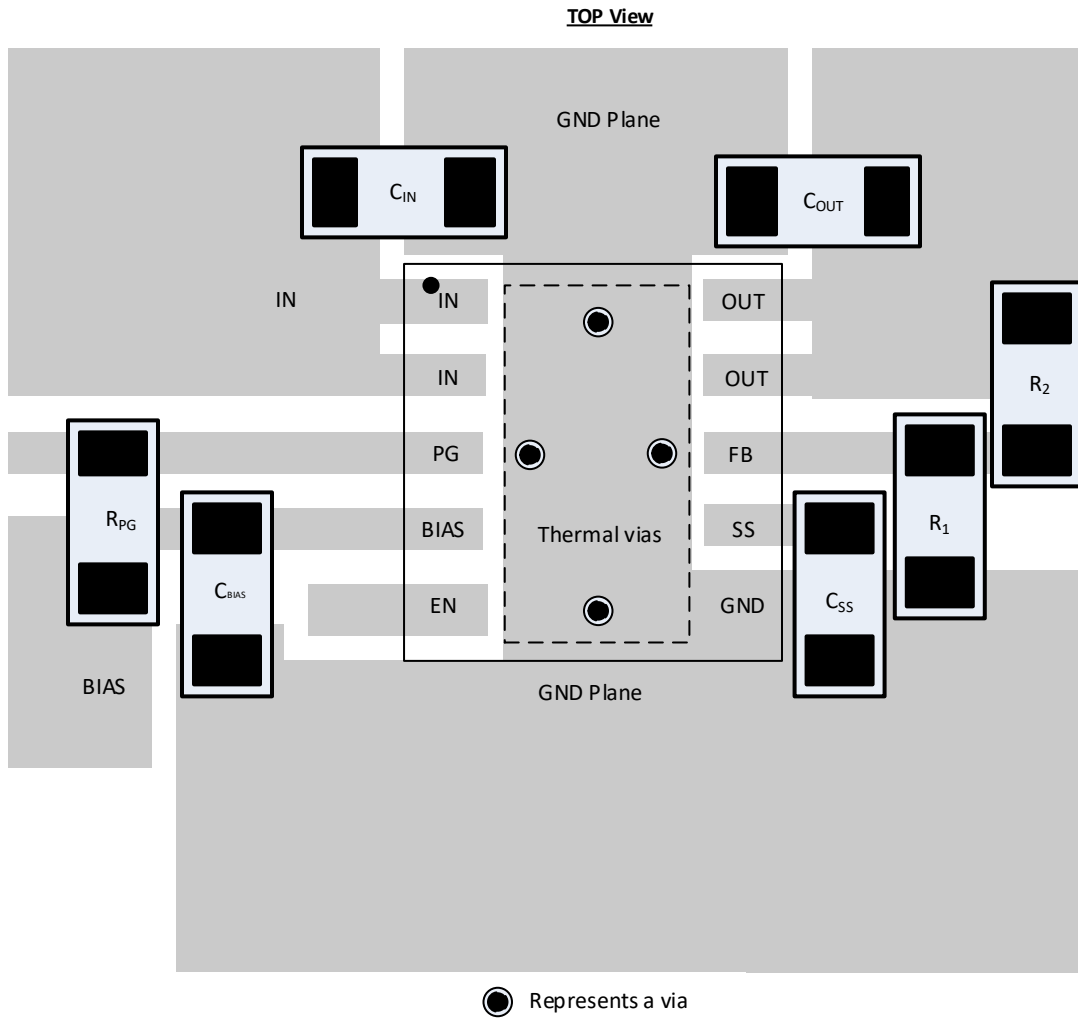


(a) Example DRC (SON) Package Measurement

- A.  $T_T$  is measured at the center of both the X- and Y-dimensional axes.
- B.  $T_B$  is measured *below* the package lead on the PCB surface.

图 7-6. Measuring Points for  $T_T$  and  $T_B$

### 7.4.2 Layout Example



**图 7-7. Layout Example: DRC Package**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, [Using New Thermal Metrics application note](#)

#### 8.1.2 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT <sup>(1)</sup>	V <sub>OUT</sub>
TPS74801Q(W)yyyzM3Q1	<p><b>Q</b> indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard.</p> <p><b>W</b> indicates that the package has wettable flanks (new chip only).</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity.</p> <p><b>M3</b> is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document.</p> <p><b>Q1</b> indicates that this device is an automotive grade (AEC-Q100) device.</p>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

#### TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision D (December 2023) to Revision E (September 2024)</b>	<b>Page</b>
• Added $V_{IN}$ Dropout Voltage vs ( $V_{BIAS} - V_{OUT}$ ) and Temperature ( $T_A$ ) curve to <i>Typical Characteristics: <math>I_{OUT} = 50\text{ mA}</math></i> section.....	8
• Added active pulldown to <i>Legacy Chip Functional Block Diagram</i> and added <i>New Chip Functional Block Diagram</i> .....	16

<b>Changes from Revision C (July 2023) to Revision D (December 2023)</b>	<b>Page</b>
• 通篇添加了器件措辞以区分旧芯片和新芯片信息.....	1
• 更改了 <i>说明</i> 部分：更改了 <i>导通响应</i> 图并为新芯片添加了温度范围.....	1
• Changed <i>Typical Characteristics</i> sections to show legacy chip and new chip data side by side and deleted $V_{IN}$ Dropout Voltage vs $V_{BIAS}-V_{OUT}$ curves.....	8
• Changed images in <i>Estimating Junction Temperature</i> section.....	25
• Deleted RGW Example figure from <i>Layout Example</i> section.....	27
• Added <i>Device Nomenclature</i> section.....	28

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74801QDRCRM3Q1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	QVK	<a href="#">Samples</a>
TPS74801QRGWRM3Q1	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801Q	<a href="#">Samples</a>
TPS74801QRGWRQ1	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 74801Q	<a href="#">Samples</a>
TPS74801QWDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	SMF	<a href="#">Samples</a>
TPS74801TDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	QVK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS74801-Q1 :**

- Catalog : [TPS74801](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801QDRCRM3Q1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801QRGWRM3Q1	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74801QRGWRQ1	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74801QWDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801TDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801QDRCRM3Q1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801QRGWRM3Q1	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801QRGWRQ1	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801QWDRCRQ1	VSON	DRC	10	3000	360.0	360.0	36.0
TPS74801TDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

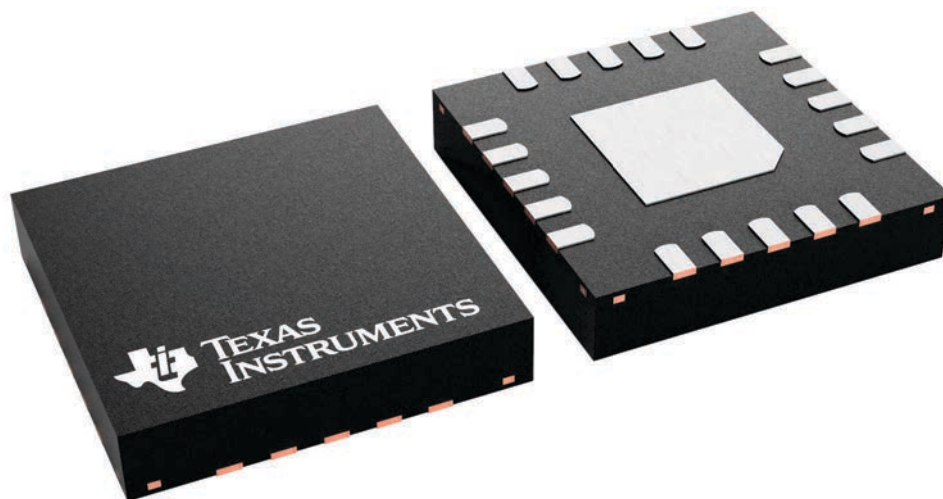
**RGW 20**

**VQFN - 1 mm max height**

5 x 5, 0.65 mm pitch

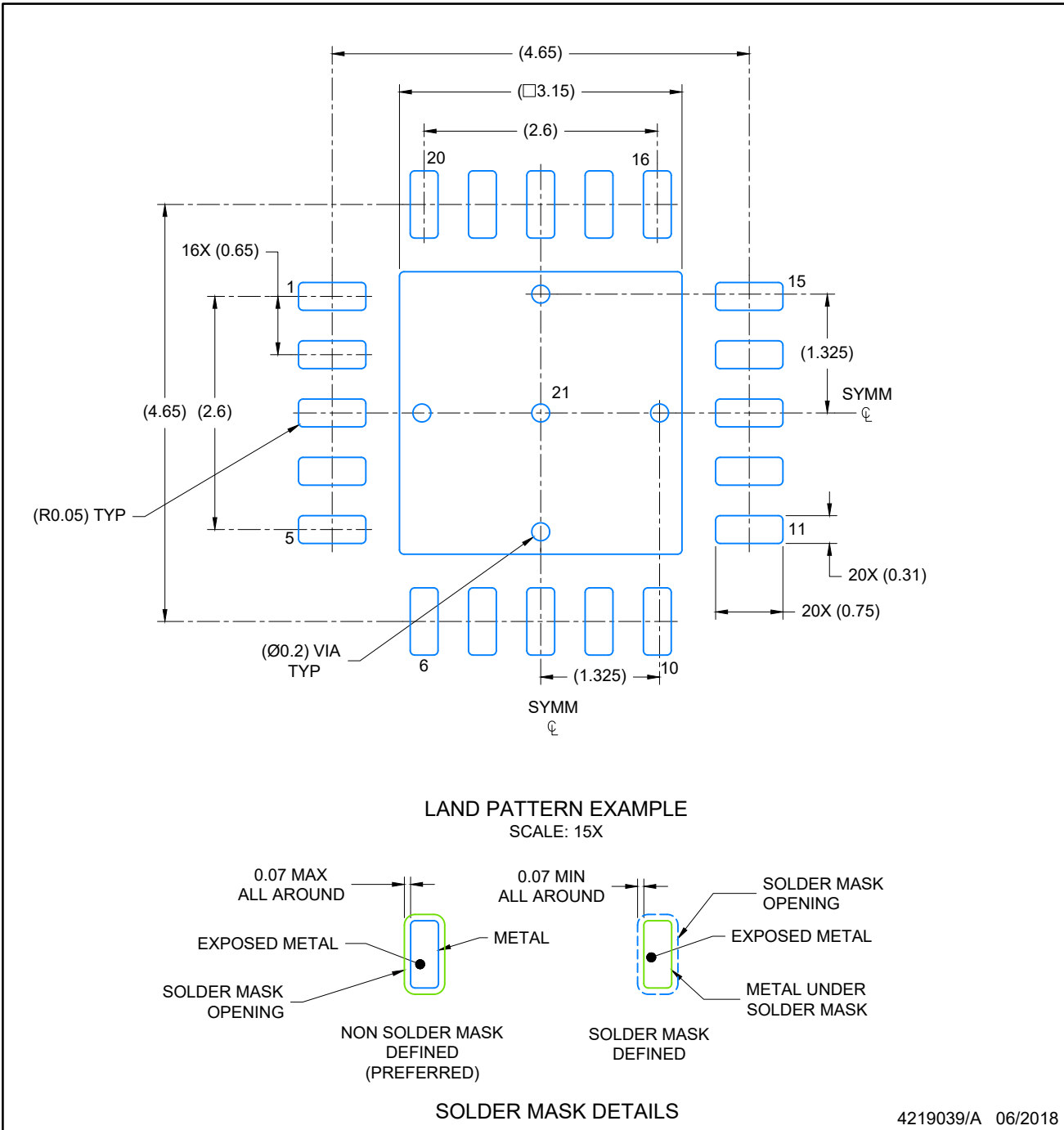
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227157/A





NOTES: (continued)

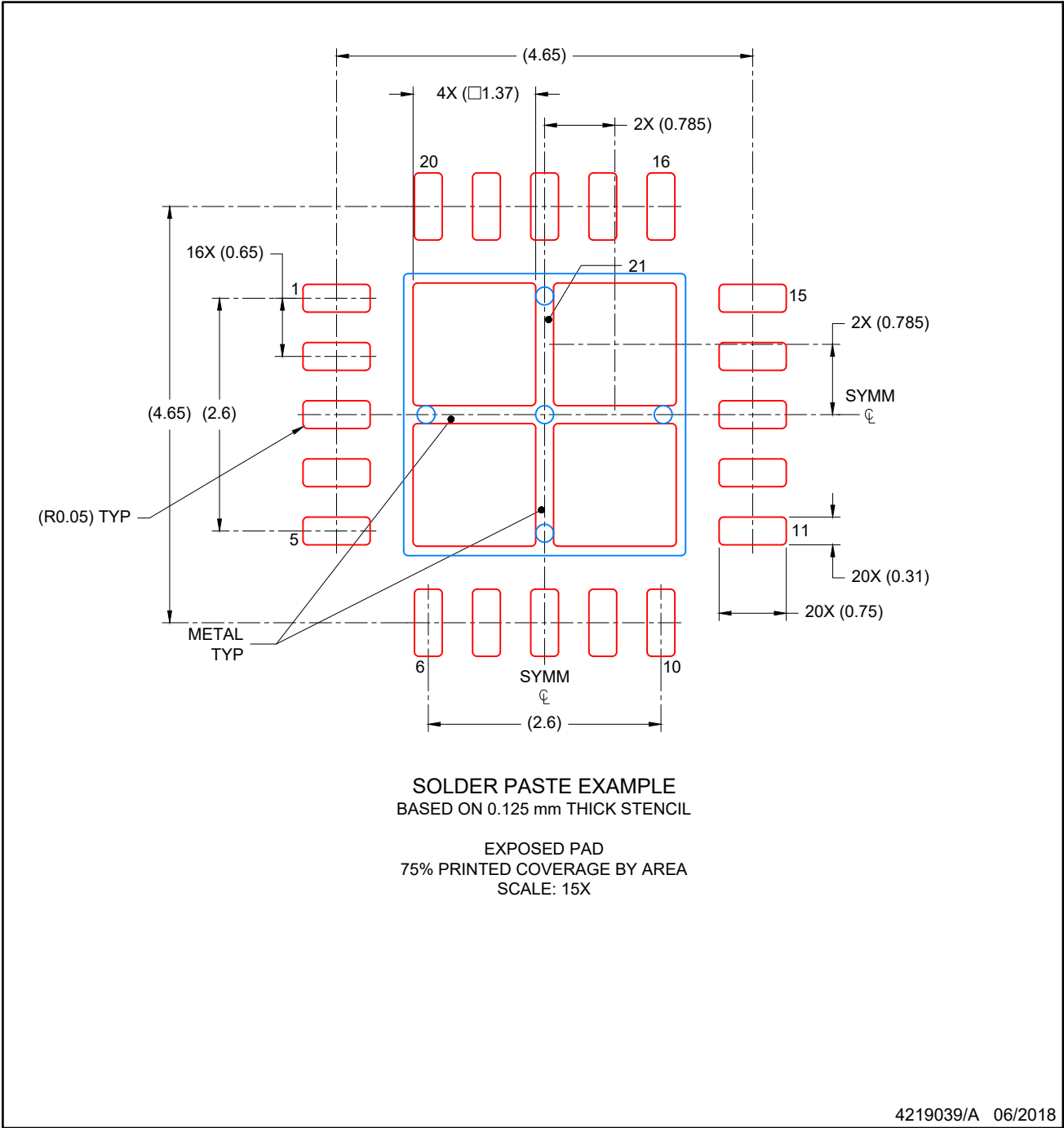
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGW0020A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

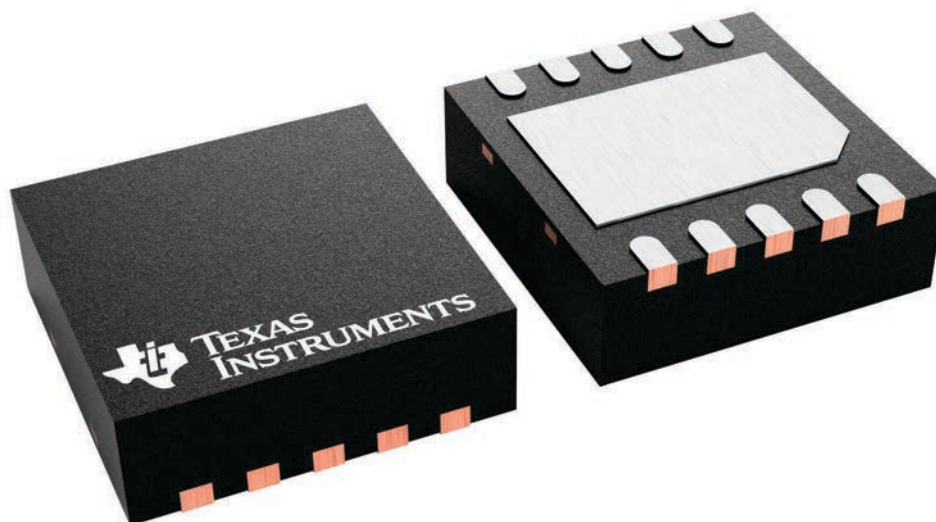
**DRC 10**

**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226193/A



# EXAMPLE BOARD LAYOUT

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



# EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



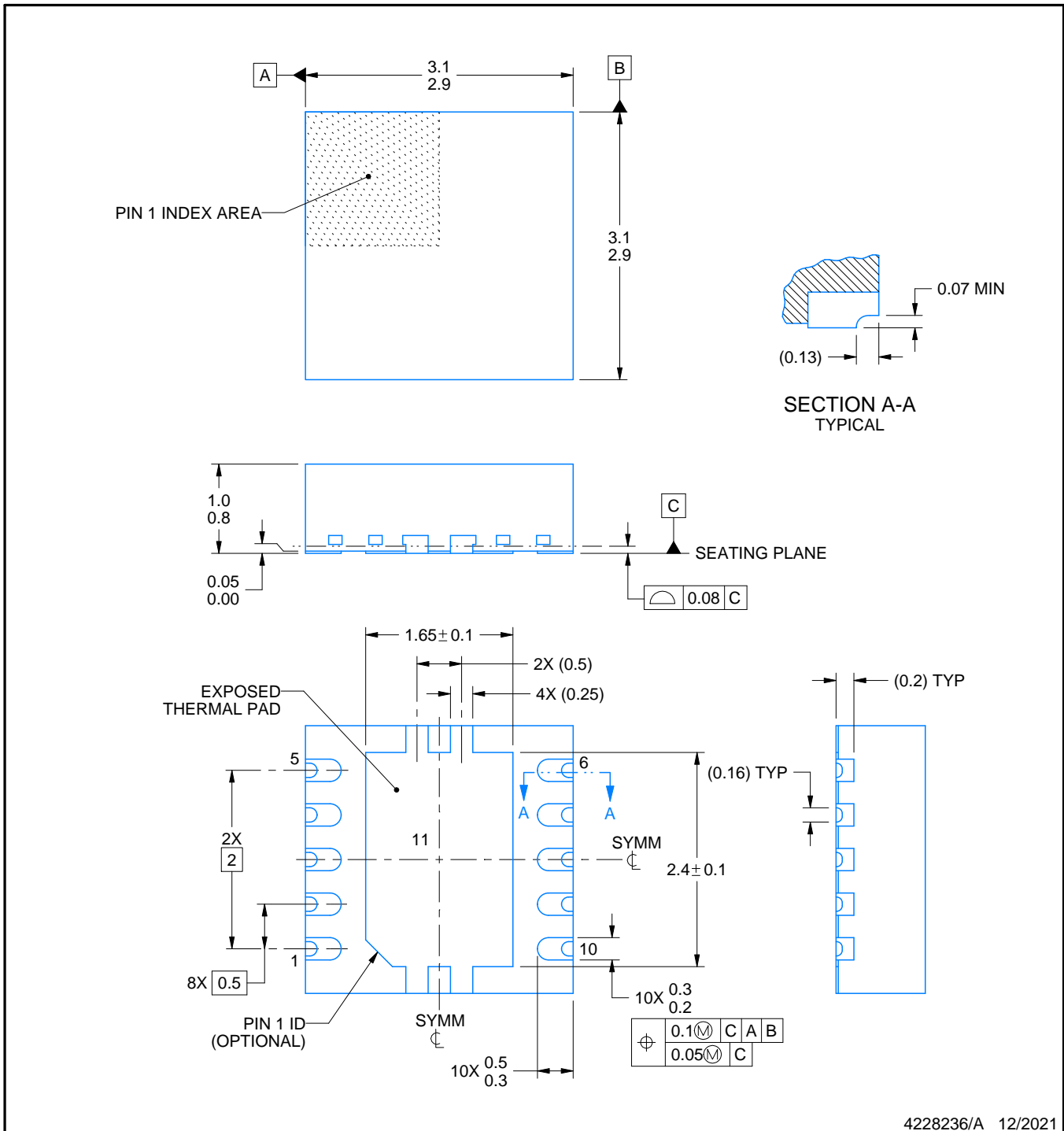
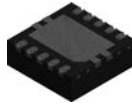
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4228236/A 12/2021

NOTES:

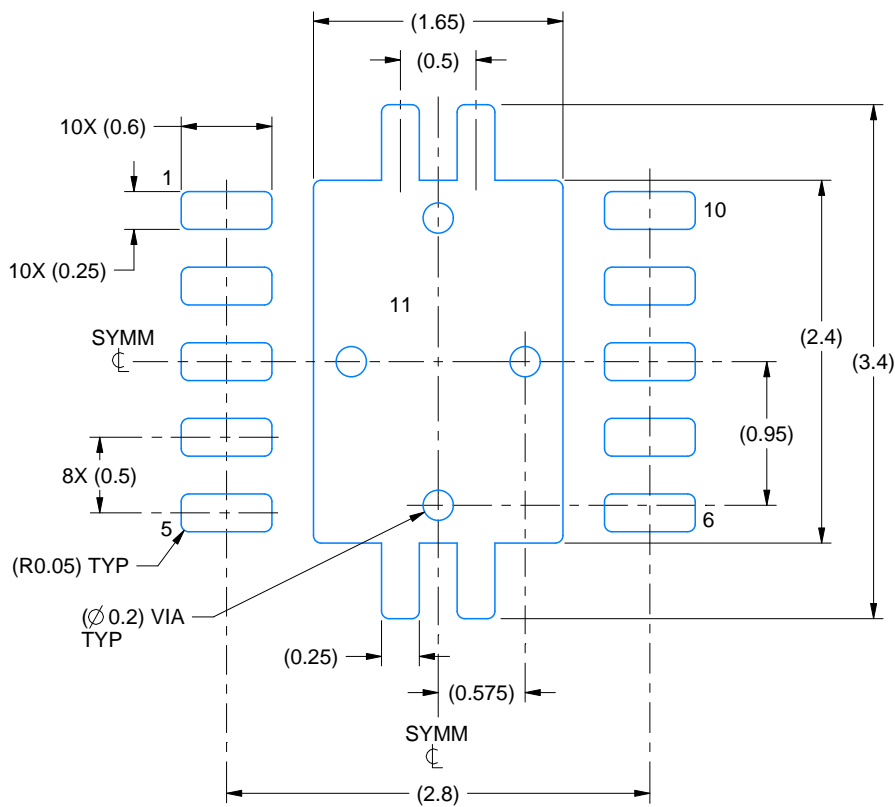
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

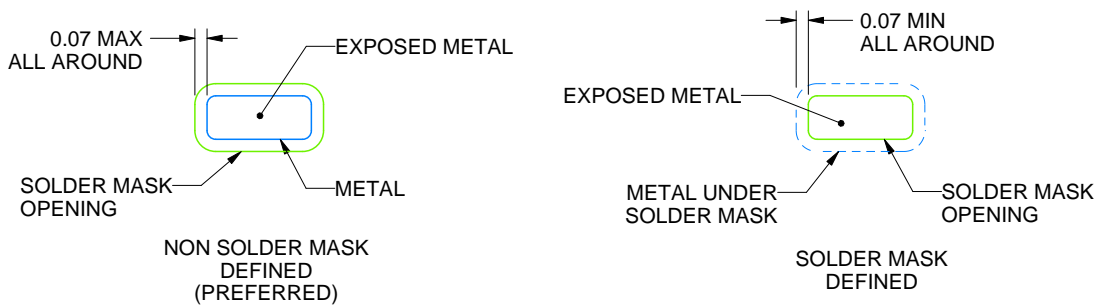
DRC0010W

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

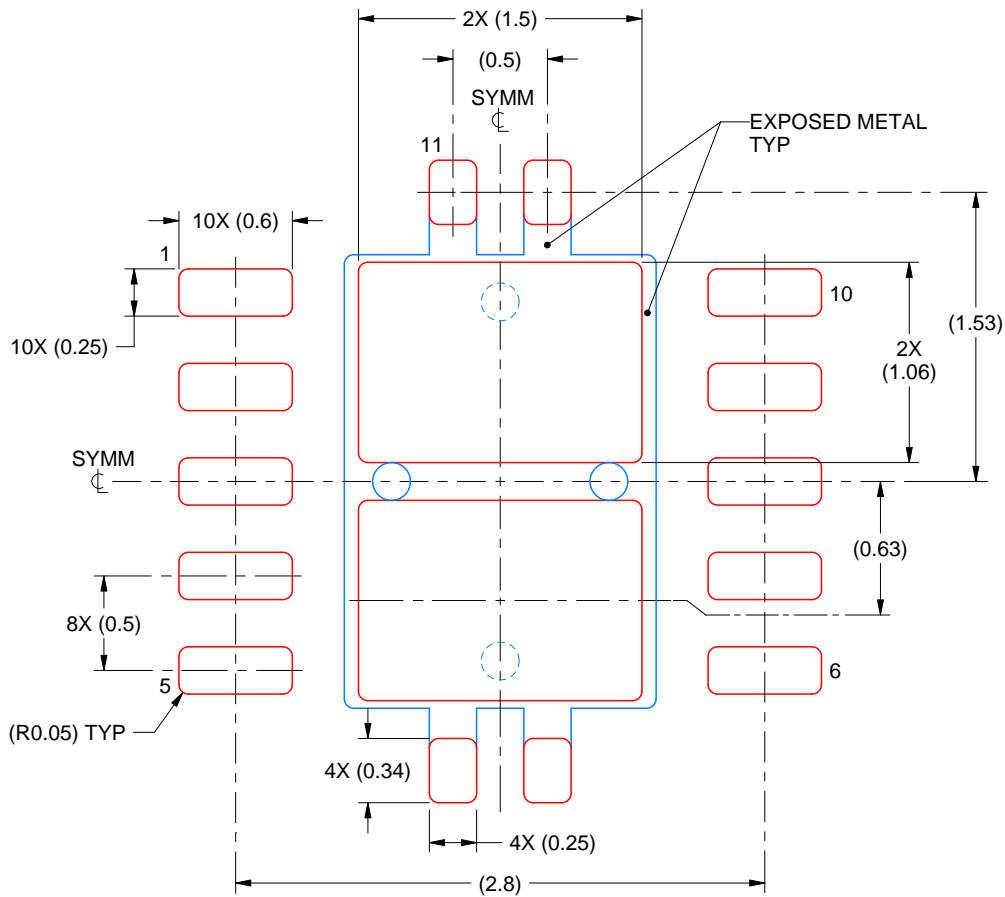
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRC0010W

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4228236/A 12/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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