150mA, Low-Dropout Regulator, Ultralow-Power, I_Q 1μA with Pin-Selectable, Dual-Level Output Voltage

FEATURES

- **Low I_Q: 1μA**
- **150mA, Low-Dropout Regulator with Pin-Selectable Dual Voltage Level Output**
- **Low Dropout: 200mV at 150mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Available in Dual-Level, Fixed Output Voltages from 1.5V to 4.2V Using Innovative Factory EPROM Programming**
- **Available in an Adjustable Version from 1.22V to 5.25V or a Dual-Level Output Version**
- **V_{SET} Pin Toggles Output Voltage Between Two Factory-Programmed Voltage Levels**
- **Stable with a 1.0μF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **CMOS Logic Level-Compatible Enable Pin**
- **Available in DDC (TSOT23-5) or DRV (2mm × 2mm SON-6) Package Options**

APPLICATIONS

- **TI MSP430 Attach Applications**
- **Power Rails with Programming Mode**
- **Dual Voltage Levels for Power-Saving Mode**
- **Wireless Handsets, Smartphones, PDAs, MP3 Players, and Other Battery-Operated Handheld Products**

DESCRIPTION

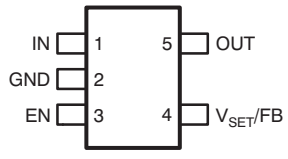
The TPS781 family of low-dropout (LDO) regulators offer the benefits of ultralow power (I_Q = 1μA), miniaturized packaging (2×2 SON-6), and selectable dual-level output voltage levels. An adjustable version is also available, but does not have the capability to shift voltage levels.

The V_{SET} pin allows the end user to switch between two voltage levels *on-the-fly* through a microprocessor-compatible input. This LDO is designed specifically for battery-powered applications where dual-level voltages are needed. With ultralow I_Q (1μA), microprocessors, memory cards, and smoke detectors are ideal applications for this device.

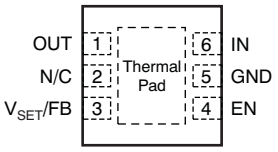
The ultralow-power and selectable dual-level output voltages allow designers to customize power consumption for specific applications. Designers can now shift to a lower voltage level in a battery-powered design when the microprocessor is in sleep mode, further reducing overall system power consumption. The two voltage levels are preset at the factory through a unique architecture using an EPROM. The EPROM technique allows for numerous output voltage options between V_{SET} low (1.5V to 4.2V) and V_{SET} high (2.0V to 3.0V) in the fixed output version only. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

The TPS781 series are designed to be compatible with the TI MSP430 and other similar products. The enable pin is compatible with standard CMOS logic. This LDO is stable with any output capacitor greater than 1.0μF. Therefore, implementations of this device require minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS781 series I_Q (1μA) also come with thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to +125°C. For high-performance applications requiring a dual-level voltage option, consider the TPS780 series, with an I_Q of 500nA and dynamic voltage scaling.

TPS781DDC
TSOT23-5
(TOP VIEW)



TPS781DRV
2mm x 2mm SON-6
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PRODUCT	V_{OUT}
TPS781**vvvxxxyyyz**	**VVV** is the nominal output voltage for $V_{OUT(HIGH)}$ and corresponds to V_{SET} pin low. **XXX** is the nominal output voltage for $V_{OUT(LOW)}$ and corresponds to V_{SET} pin high. **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250). Adjustable version(3)(4)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Additional output voltage combinations are available on a quick-turn basis using innovative, factory EPROM programming. Minimum-order quantities apply; contact your sales representative for details and availability.
(3) To order the adjustable version, use *TPS78101YYYZ*.
(4) The device is either fixed voltage, dual-level V_{OUT}, or adjustable voltage only. Device design does not permit a fixed and adjustable output simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

PARAMETER		TPS781 Series	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable and V_{SET} voltage range, V_{EN} and V_{VSET}		–0.3 to V_{IN} + 0.3(2)	V
Output voltage range, V_{OUT}		–0.3 to V_{IN} + 0.3V	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See the Dissipation Ratings table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–40 to +125	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} and V_{VSET} absolute maximum rating are V_{IN} + 0.3V or +6.0V, whichever is less.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(1)	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

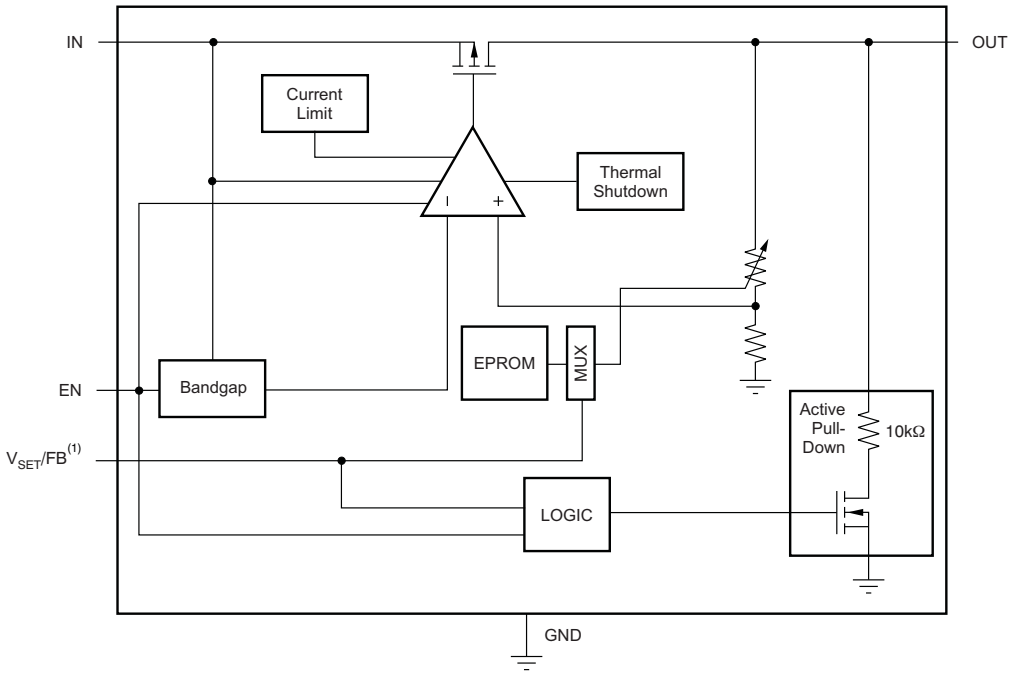
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{VSET} = V_{EN} = V_{IN}, C_{OUT} = 1.0µF, fixed or adjustable, unless otherwise noted. Typical values at T_J = +25°C.

PARAMETER			TEST CONDITIONS		TPS781 Series MIN	TPS781 Series TYP	TPS781 Series MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT} [1]	DC output accuracy	Nominal	T_J = +25°C, V_{SET} = high/low		–2	±1	+2	%
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 150mA, V_{SET} = high/low		–3.0	±2.0	+3.0	%
V_{FB}	Internal reference [2] (adjustable version only)		T_J = +25°C, V_{IN} = 4.0V, I_{OUT} = 75mA			1.216		V
V_{OUT_RANGE}	Output voltage range [3][4] (adjustable version only)		V_{IN} = 5.5V, I_{OUT} = 100µA [2]		V_{FB}	5.25		V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 5mA		–1		+1	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 150mA		–2		+2	%
V_{DO}	Dropout voltage [5]		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150mA				250	mV
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 1mA			86		μV_{RMS}
V_{HI}	V_{SET} high (output $V_{OUT(LOW)}$ selected), or EN high (enabled)				1.2		V_{IN}	V
V_{LO}	V_{SET} low (output $V_{OUT(HIGH)}$ selected), or EN low (disabled)				0		0.4	V
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(NOM)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA			1.0	1.3	µA
			I_{OUT} = 150mA			8		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.2V ≤ V_{IN} < 5.5V, T_J = –40°C to +100°C			18	130	nA
I_{VSET}	V_{SET} pin current		V_{EN} = V_{VSET} = 5.5V				70	nA
I_{EN}	EN pin current		V_{EN} = V_{VSET} = 5.5V				40	nA
I_{FB}	FB pin current [6] (adjustable version only)		V_{IN} = 5.5V, V_{OUT} = 1.2V, I_{OUT} = 100µA				10	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA	f = 10Hz		40		dB
				f = 100Hz		20		dB
				f = 1kHz		15		dB
$t_{TR(H\rightarrow L)}$	V_{OUT} transition time (high-to-low) V_{OUT} = 97% × $V_{OUT(HIGH)}$		V_{OUT_LOW} = 2.2V, $V_{OUT(HIGH)}$ = 3.3V, I_{OUT} = 10mA			800		µs
$t_{TR(L\rightarrow H)}$	V_{OUT} transition time (low-to-high) V_{OUT} = 97% × $V_{OUT(LOW)}$		V_{OUT_HIGH} = 3.3V, $V_{OUT(LOW)}$ = 2.2V, I_{OUT} = 10mA			800		µs
t_{STR}	Startup time [7]		C_{OUT} = 1.0µF, V_{OUT} = 10% $V_{OUT(NOM)}$ to V_{OUT} = 90% $V_{OUT(NOM)}$			500		µs
t_{SHDN}	Shutdown time [8]		I_{OUT} = 150mA, C_{OUT} = 1.0µF, V_{OUT} = 2.8V, V_{OUT} = 90% $V_{OUT(NOM)}$ to V_{OUT} = 10% $V_{OUT(NOM)}$			500 [9]		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			+160		°C
			Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature				–40		+125	°C

(1) The output voltage for V_{SET} = low/high is programmed at the factory.
(2) Adjustable version only.
(3) No V_{SET} pin on the adjustable version.
(4) No dynamic voltage scaling on the adjustable version.
(5) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.3V because minimum V_{IN} = 2.2V.
(6) The TPS78101 FB pin is tied to V_{OUT}. Adjustable version only.
(7) Time from V_{EN} = 1.2V to V_{OUT} = 90% ($V_{OUT(NOM)}$).
(8) Time from V_{EN} = 0.4V to V_{OUT} = 10% ($V_{OUT(NOM)}$).
(9) See *Shutdown* in the *Application Information* section for more details.

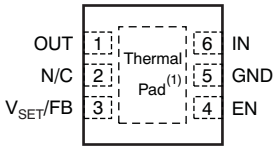
FUNCTIONAL BLOCK DIAGRAM



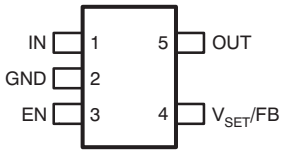
(1) Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions.

PIN CONFIGURATIONS

TPS781DRV
2mm x 2mm SON-6
(TOP VIEW)



TPS781DDC
TSOT23-5
(TOP VIEW)



(1) It is recommended that the SON package thermal pad be connected to ground.

Table 1. TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	DRV	DDC	
OUT	1	5	Regulated output voltage pin. A small (1µF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the Application Information section for more details.
N/C	2	—	Not connected.
V_{SET}/FB	3	4	Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions. Driving the select pin (V_{SET}) below 0.4V selects preset output voltage high. Driving the V_{SET} pin over 1.2V selects preset output voltage low.
EN	4	3	Driving the enable pin (EN) over 1.2V turns on the regulator. Driving this pin below 0.4V puts the regulator into shutdown mode, reducing operating current to 18nA typical.
GND	5	2	Ground pin.
IN	6	1	Input pin. A small capacitor is needed from this pin to ground to assure stability. Typical input capacitor = 1.0µF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
Thermal pad	Thermal pad	—	It is recommended that the SON package thermal pad be connected to ground.

TYPICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 1.22V (typ)
TPS78101

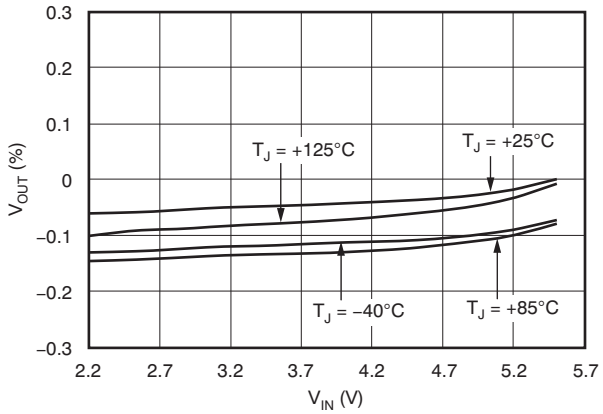


Figure 1.

LINE REGULATION
I_{OUT} = 5mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V (typ)
TPS781330220

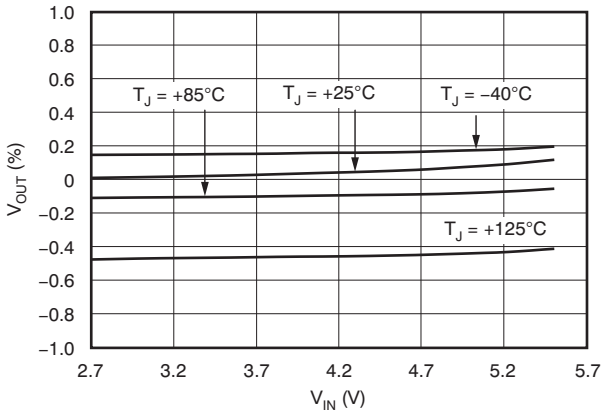


Figure 2.

LINE REGULATION
I_{OUT} = 150mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V (typ)
TPS781330220

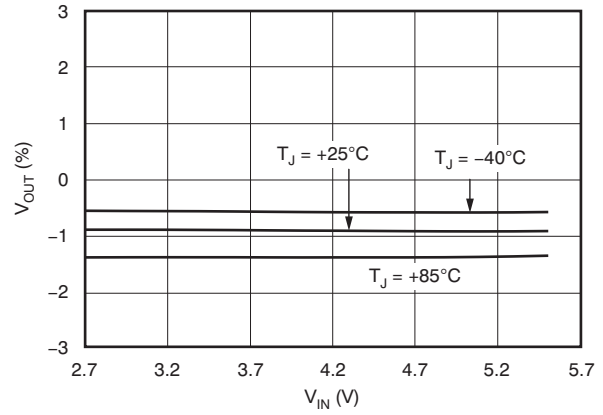


Figure 3.

LINE REGULATION
I_{OUT} = 5mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ)
TPS781330220

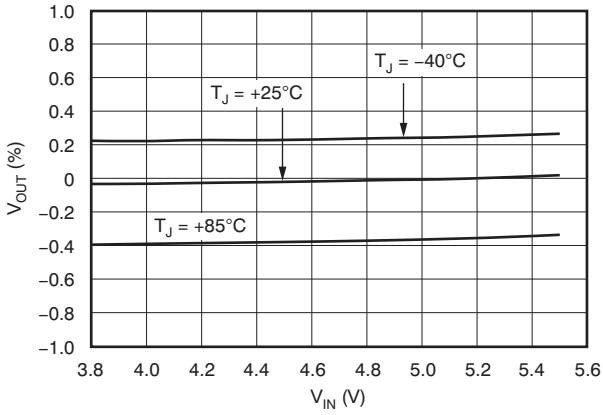


Figure 4.

LINE REGULATION
I_{OUT} = 150mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ)
TPS781330220

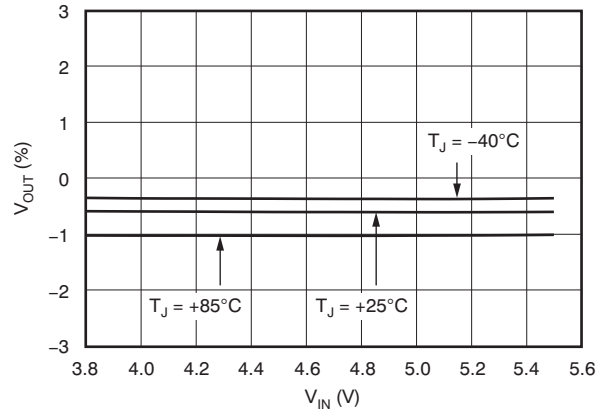


Figure 5.

LOAD REGULATION
V_{OUT} = 3.3V
TPS78101

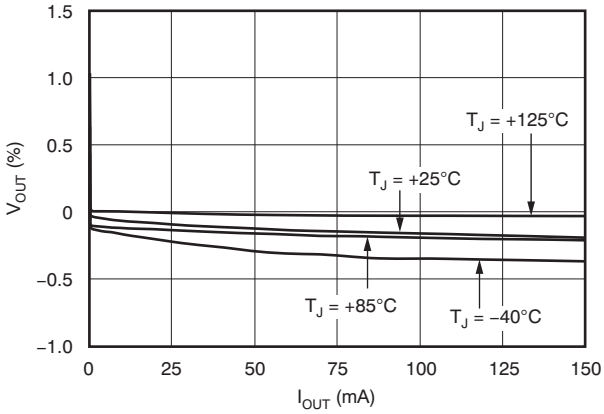


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

LOAD REGULATION
V_{VSET} = 1.2V, V_{IN} = 2.7V, V_{OUT} = 2.2V
TPS781330220

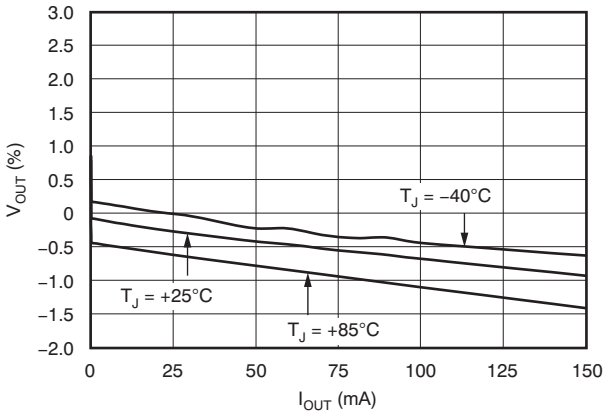


Figure 7.

LOAD REGULATION
V_{VSET} = 0.4V, V_{IN} = 3.8V, V_{OUT} = 3.3V
TPS781330220

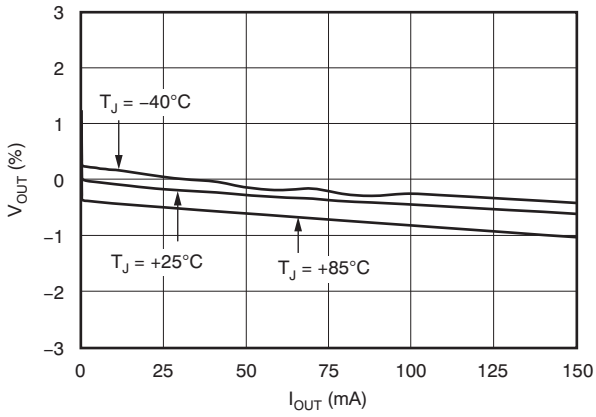


Figure 8.

DROPOUT VOLTAGE vs OUTPUT CURRENT
V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78101

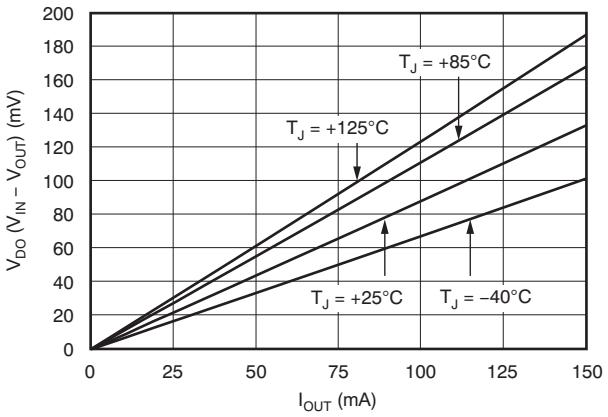


Figure 9.

DROPOUT VOLTAGE vs OUTPUT CURRENT
V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS781330220

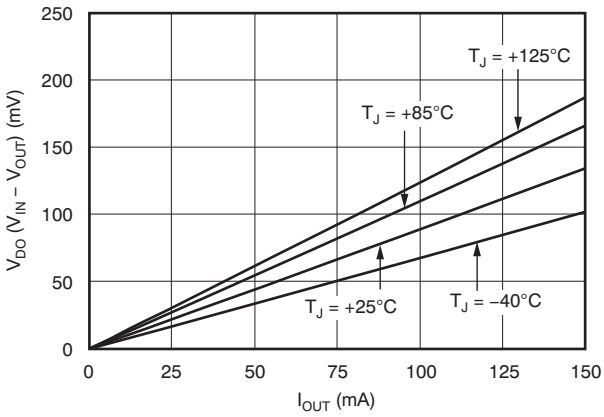


Figure 10.

DROPOUT VOLTAGE vs TEMPERATURE
V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS78101

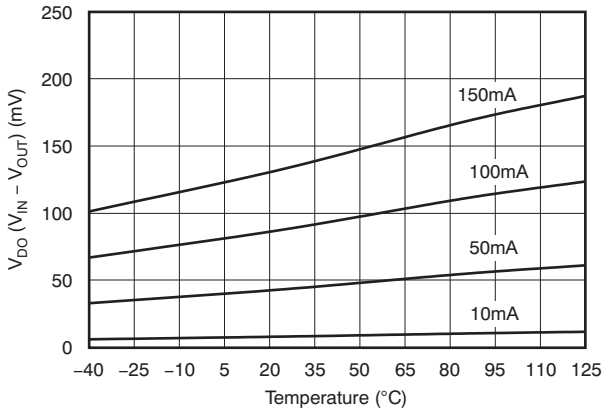


Figure 11.

DROPOUT VOLTAGE vs TEMPERATURE
V_{VSET} = 0.4V, V_{OUT} = 3.3V (typ), V_{IN} = 0.95 × V_{OUT} (typ)
TPS781330220

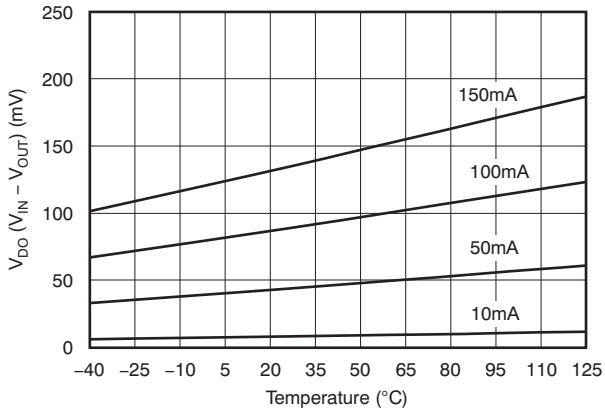


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{OUT} = 1.22V
TPS78101

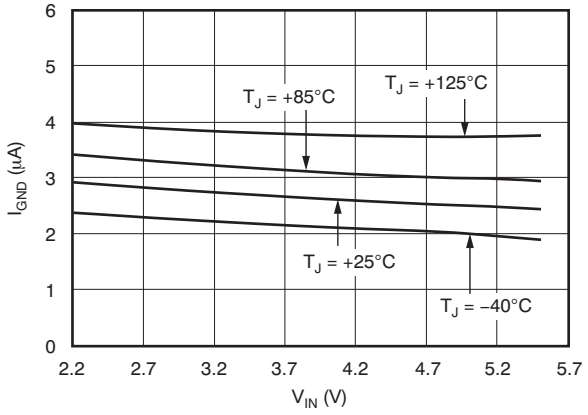


Figure 13.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{OUT} = 1.22V
TPS78101

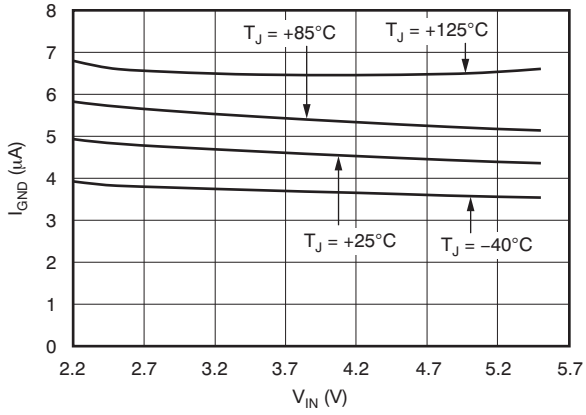


Figure 14.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS781330220

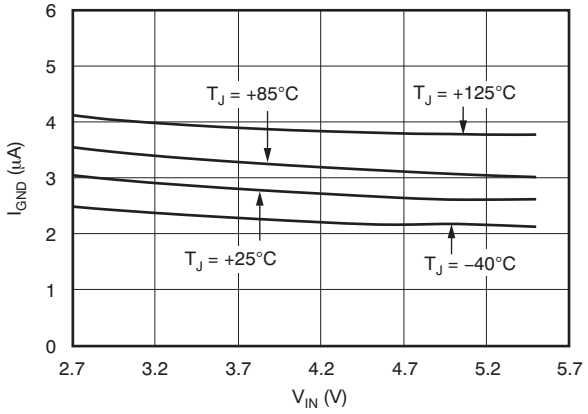


Figure 15.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS781330220

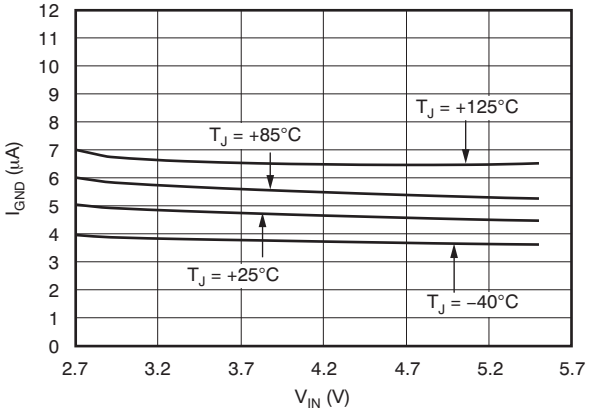


Figure 16.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 50mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS781330220

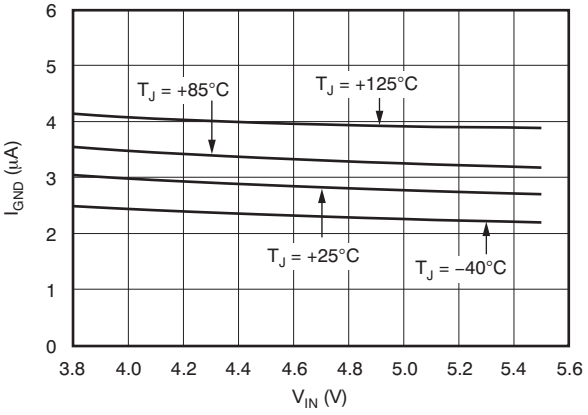


Figure 17.

GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 150mA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS781330220

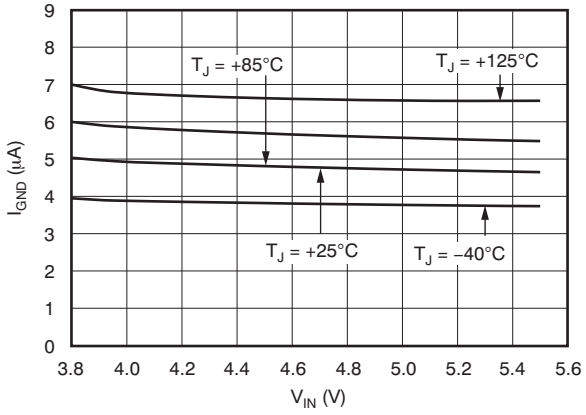


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

SHUTDOWN CURRENT vs INPUT VOLTAGE
I_{OUT} = 0mA, V_{VSET} = 0.4V
TPS78101

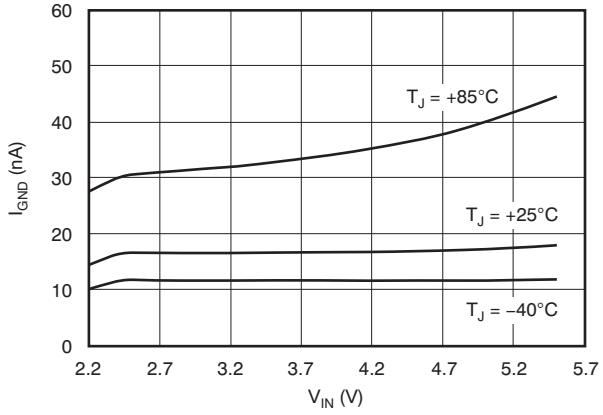


Figure 19.

CURRENT LIMIT vs INPUT VOLTAGE
V_{OUT} = 90% V_{OUT} (typ), V_{OUT} = 1.22V (typ)
TPS78101

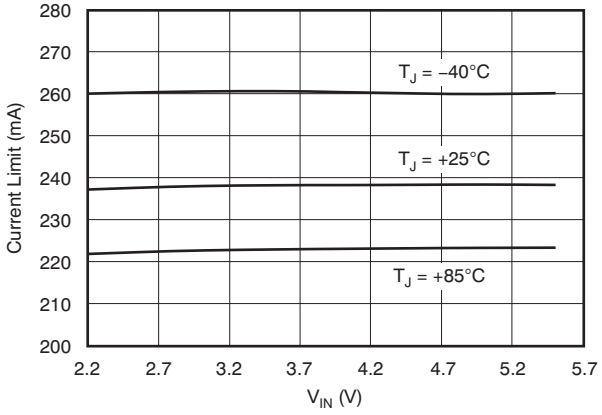


Figure 20.

CURRENT LIMIT vs INPUT VOLTAGE
V_{VSET} = 1.2V, V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 2.2V (typ)
TPS781330220

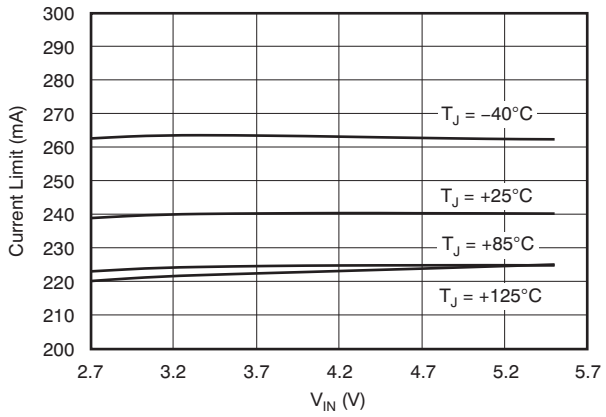


Figure 21.

CURRENT LIMIT vs INPUT VOLTAGE
V_{VSET} = 0.4V, V_{OUT} = 95% V_{OUT} (typ), V_{OUT} = 3.3V (typ)
TPS781330220

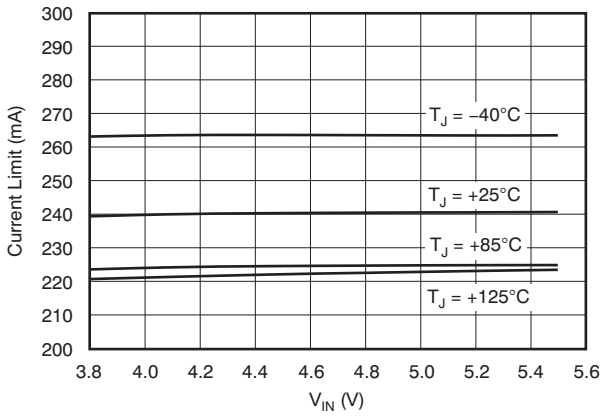


Figure 22.

FEEDBACK PIN CURRENT vs TEMPERATURE
I_{OUT} = 0mA, V_{OUT} = 1.22V
TPS78101

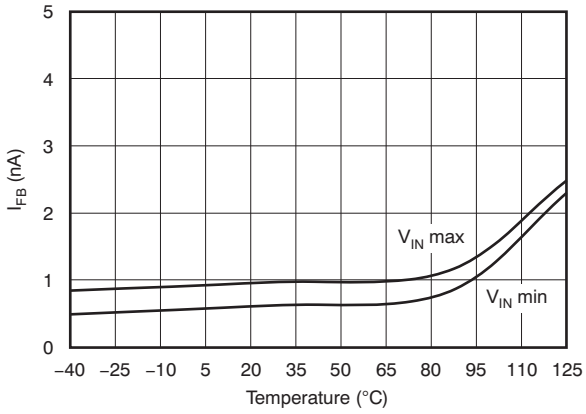


Figure 23.

V_{SET} PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 1.2V, V_{OUT} = 2.2V
TPS781330220

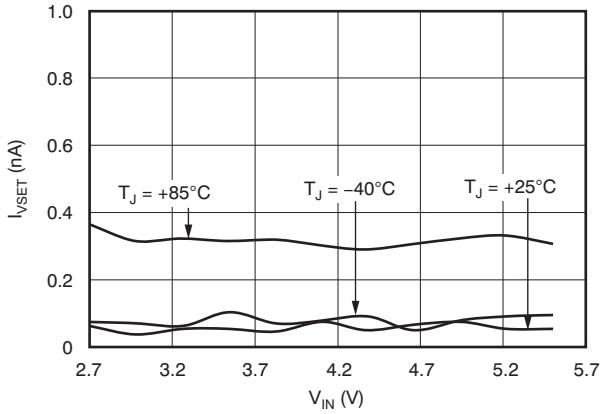


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

V_{SET} PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS781330220

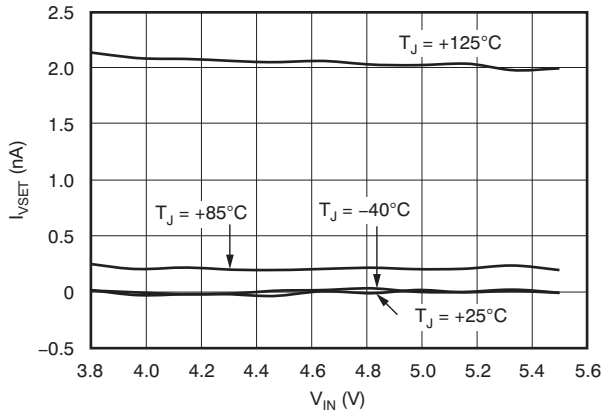


Figure 25.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 1mA, V_{OUT} = 1.22V
TPS78101

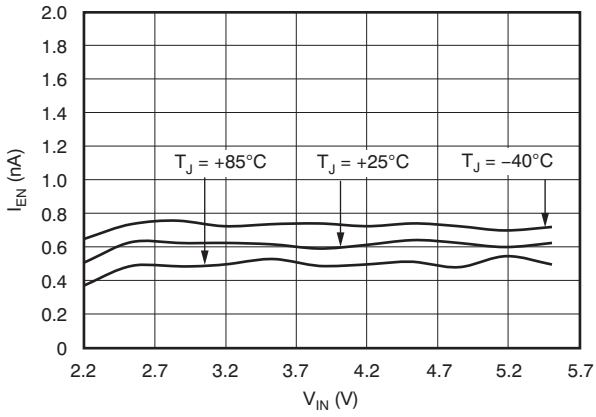


Figure 26.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{SET} = 1.2V, V_{OUT} = 2.2V
TPS781330220

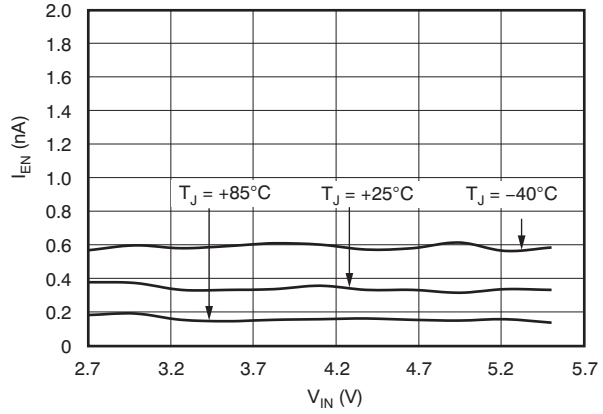


Figure 27.

ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, V_{VSET} = 0.4V, V_{OUT} = 3.3V
TPS781330220

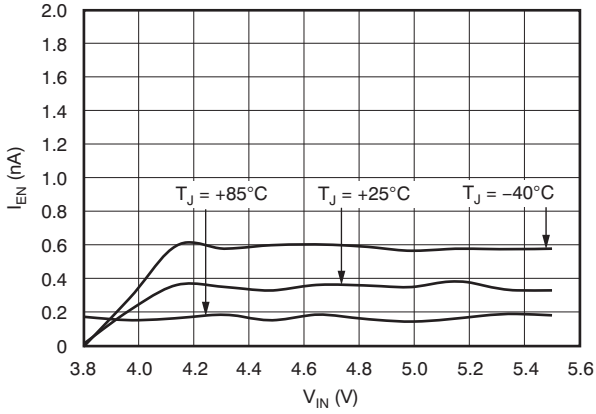


Figure 28.

ENABLE PIN HYSTERESIS vs TEMPERATURE
I_{OUT} = 1mA, TPS78101

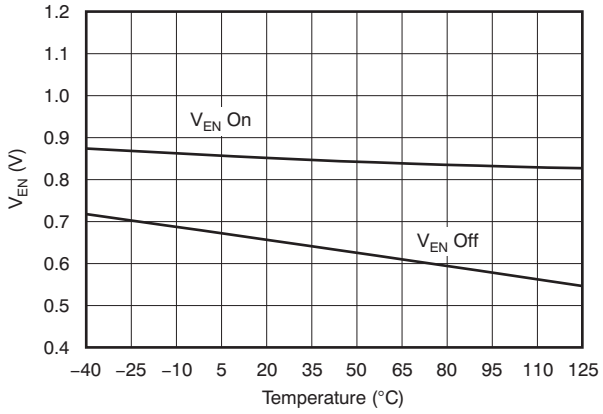


Figure 29.

ENABLE PIN HYSTERESIS vs TEMPERATURE
I_{OUT} = 1mA, TPS781330220

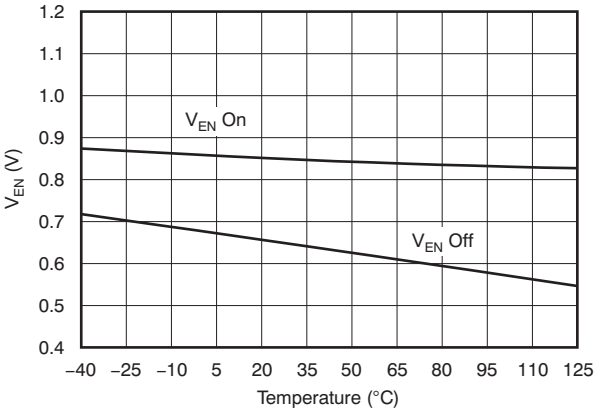


Figure 30.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

%ΔV$_{OUT}$ vs TEMPERATURE
I$_{OUT}$ = 1mA, V$_{IN}$ = 3.8V, V$_{OUT}$ = 3.3V
TPS78101

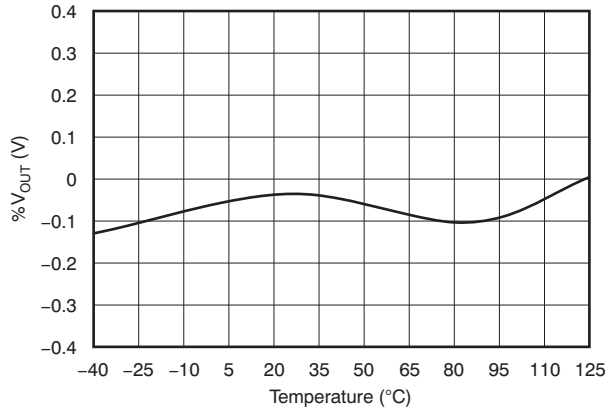


Figure 31.

%ΔV$_{OUT}$ vs TEMPERATURE
V$_{VSET}$ = 1.2V, V$_{IN}$ = 2.7V, V$_{OUT}$ = 2.2V (typ)
TPS781330220

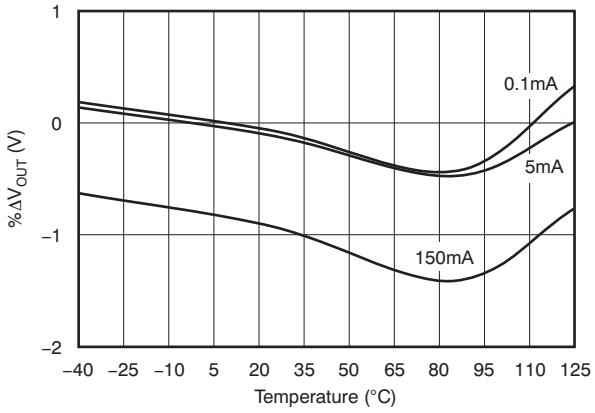


Figure 32.

%ΔV$_{OUT}$ vs TEMPERATURE
V$_{VSET}$ = 0.4V, V$_{IN}$ = 3.8V, V$_{OUT}$ = 3.3V (typ)
TPS781330220

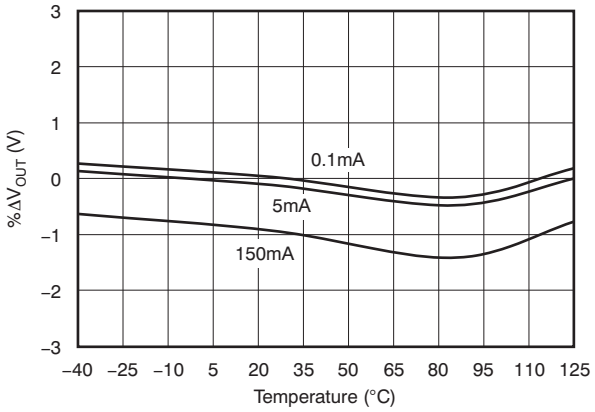


Figure 33.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY
C$_{IN}$ = 1µF, C$_{OUT}$ = 2.2µF, V$_{VSET}$ = 1.2V, V$_{IN}$ = 2.7V
TPS781330220

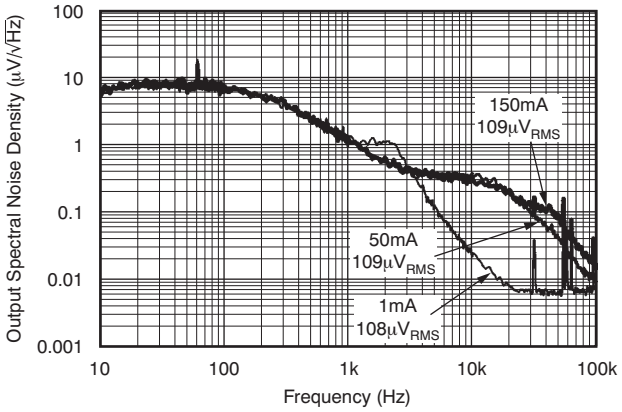


Figure 34.

RIPPLE REJECTION vs FREQUENCY
V$_{IN}$ = 2.7V, V$_{OUT}$ = 1.2V, C$_{OUT}$ = 2.2µF
TPS78101

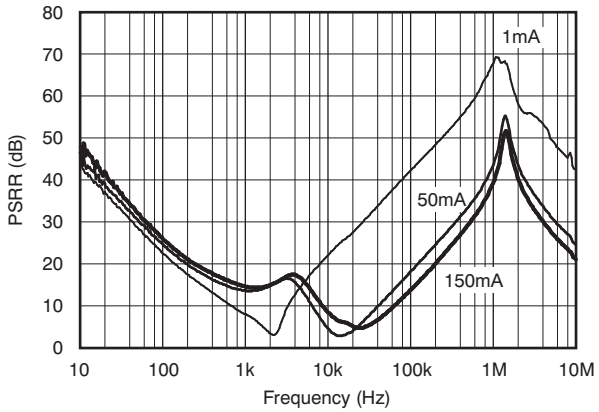


Figure 35.

INPUT VOLTAGE RAMP vs OUTPUT VOLTAGE
TPS781330220

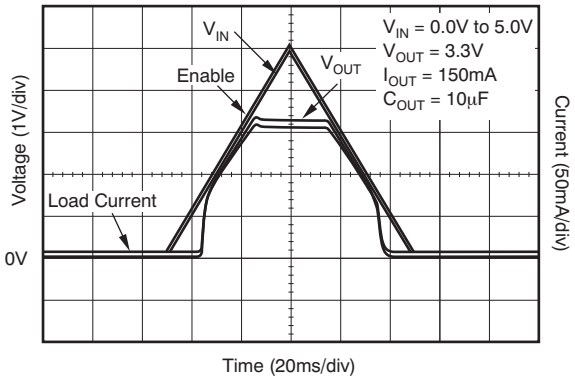


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

OUTPUT VOLTAGE vs ENABLE (SLOW RAMP)
TPS781330220

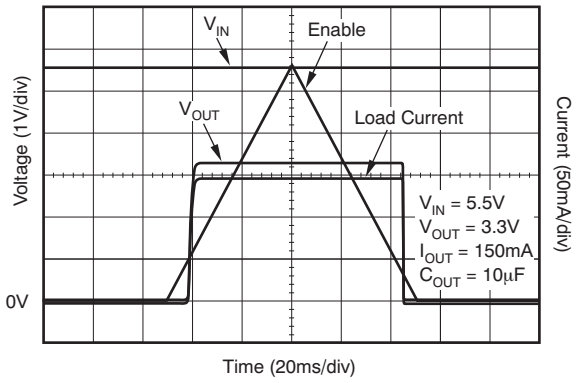


Figure 37.

INPUT VOLTAGE vs DELAY TO OUTPUT
TPS781330220

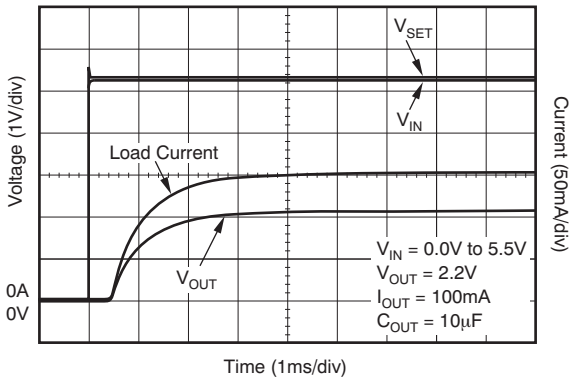


Figure 38.

LINE TRANSIENT RESPONSE
TPS781330220

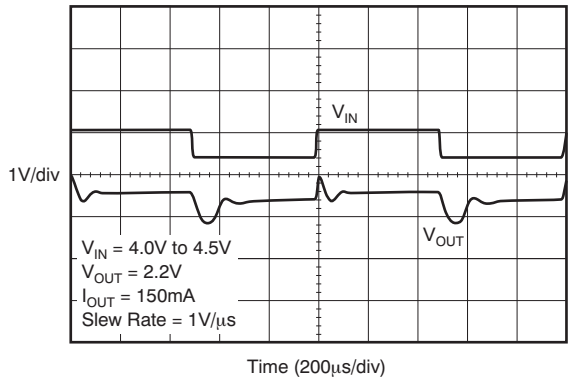


Figure 39.

LINE TRANSIENT RESPONSE
TPS781330220

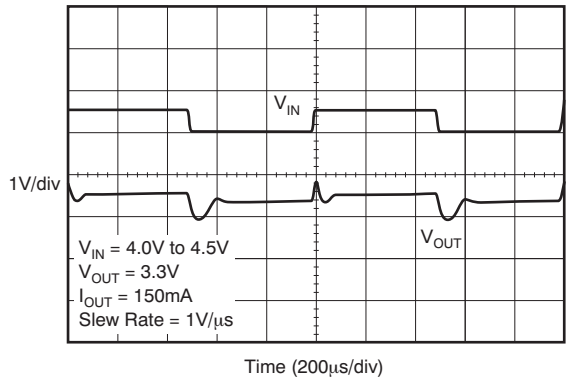


Figure 40.

LOAD TRANSIENT RESPONSE
TPS781330220

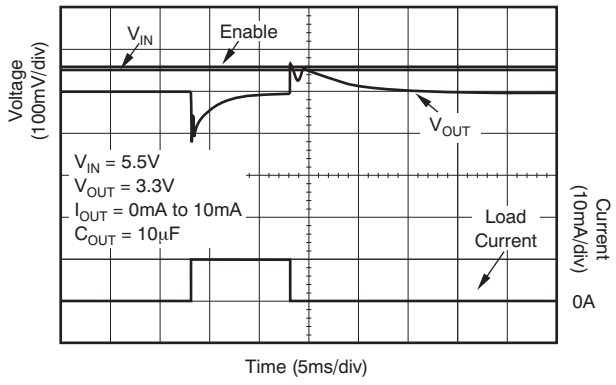


Figure 41.

LOAD TRANSIENT RESPONSE
TPS781330220

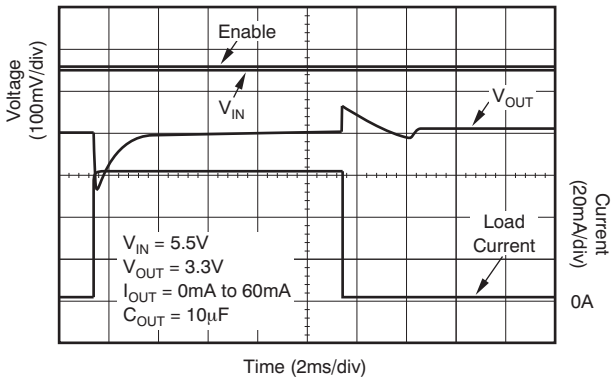


Figure 42.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

ENABLE PIN vs OUTPUT VOLTAGE RESPONSE AND OUTPUT CURRENT TPS781330220

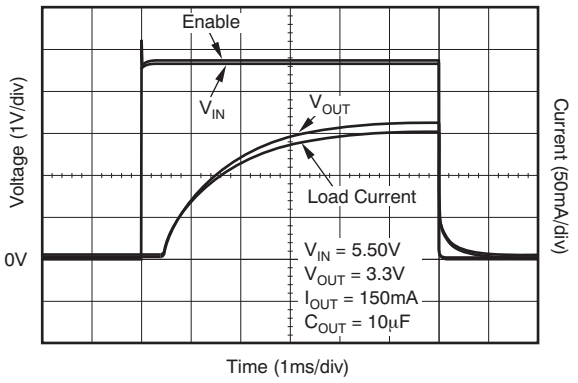


Figure 43.

ENABLE PIN vs OUTPUT VOLTAGE DELAY TPS781330220

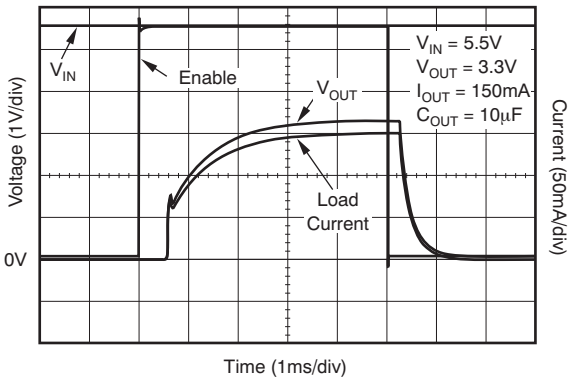


Figure 44.

V_{SET} PIN TOGGLE TPS781330220

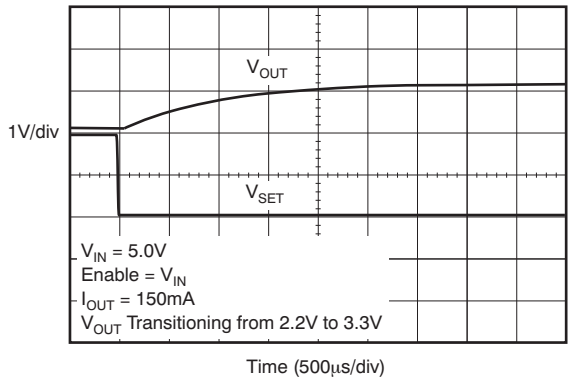


Figure 45.

V_{SET} PIN TOGGLE TPS781330220

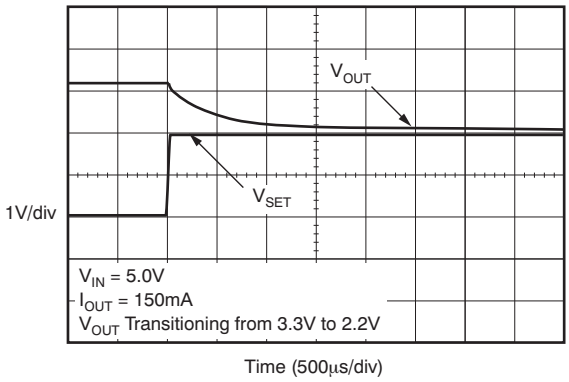


Figure 46.

V_{SET} PIN TOGGLE (SLOW RAMP) TPS781330220

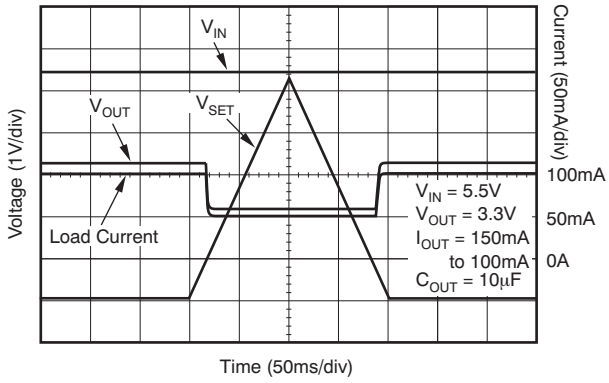


Figure 47.

APPLICATION INFORMATION

APPLICATION EXAMPLES

The TPS781 series of LDOs typically take less than 800µs to transition from a lower voltage of 2.2V to a higher voltage of 3.3V under an output load of 150mA; see Figure 45. Additionally, the TPS781 series contain active pull-down circuitry that automatically pulls charge out of the voltage capacitor to transition the output voltage from the higher voltage to the lower voltage, even with no load connected. Output voltage overshoots and undershoots are minimal under this load condition. The TPS781 series typically take less than 800µs to transition from V_{SET} low (3.3V to 2.2V), or V_{SET} high (2.2V to 3.3V); see Figure 45 and Figure 46. Both output states of the TPS781 series are factory-programmable between 1.5V to 4.2V. Note that during startup or steady-state conditions, it is important that the EN pin and V_{SET} pin voltages never exceed V_{IN} + 0.3V.

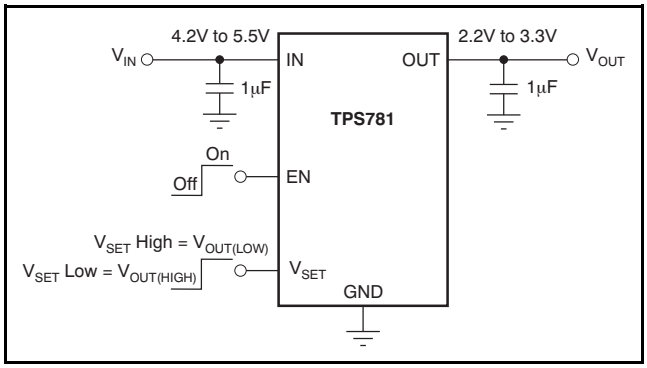


Figure 48. Typical Application Circuit

The TPS781 series is also used effectively in dynamic voltage scaling (DVS) applications. DVS applications are required to dynamically switch between a high operational voltage to a low standby voltage in order to reduce power consumption. Modern multimillion gate microprocessors fabricated with the latest sub-micron processes save power by transitioning to a lower voltage to reduce leakage currents while maintaining content. This architecture enables the microprocessor to transition quickly into an operational state (wake up) without requiring a reload of the states from external memory, or a reboot.

Programming the TPS78101 Adjustable LDO Regulator

The output voltage of the TPS78101 adjustable regulator is programmed using an external resistor divider as shown in Figure 49. The output voltage operating range is 1.2V to 5.1V, and is calculated using Equation 1:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

V_{FB} = 1.216V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 1.2µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R_1/R_2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT}. Table 2 lists several common output voltages and resistor values. The recommended design procedure is to choose R_2 = 1MΩ to set the divider current at 1.2µA, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \times R_2 \quad (2)$$

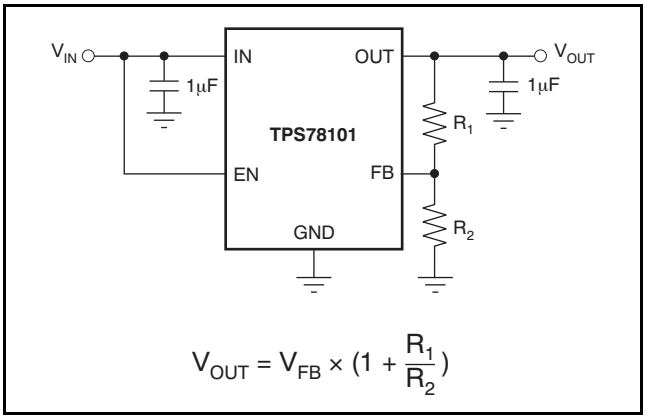


Figure 49. TPS78101 Adjustable LDO Regulator Programming

Table 2. Output Voltage Programming Guide

OUTPUT VOLTAGE	R_1	R_2
1.8V	0.499MΩ	1MΩ
2.8V	1.33MΩ	1MΩ
5.0V	3.16MΩ	1MΩ

Powering the MSP430 Microcontroller

Several versions of the TPS781 are ideal for powering the MSP430 microcontroller. Table 3 shows potential applications of some voltage versions.

Table 3. Typical MSP430 Applications

DEVICE	$V_{OUT(HIGH)}$ (TYP)	$V_{OUT(LOW)}$ (TYP)	APPLICATION
TPS781360200	3.6V	2.0V	$V_{OUT, MIN}$ > 1.800V required by many MSP430s. Allows lowest power consumption operation.
TPS781360220	3.6V	2.2V	$V_{OUT, MIN}$ > 2.200V required by some MSP430s FLASH operation.
TPS781360300	3.6V	3.0V	$V_{OUT, MIN}$ > 2.700V required by some MSP430s FLASH operation.
TPS781360220	3.6V	2.2V	$V_{OUT, MIN}$ < 3.600V required by some MSP430s. Allows highest speed operation.

The TPS781 family offers many output voltage versions to allow designers to optimize the supply voltage for the processing speed required of the MSP430. This flexible architecture minimizes the supply current consumed by the particular MSP430 application. The MSP430 total system power can be reduced by substituting the 1μA I_Q TPS781 series LDO in place of an existing, older-technology LDO. Additionally, DVS allows for increasing the clock speed in active mode (MSP430 V_{CC} = 3.6V). The 3.6V V_{CC} reduces the MSP430 time in active mode. In low-power mode, MSP430 system power can be further reduced by lowering the MSP430 V_{CC} to 2.2V in sleep mode.

Key features of the TPS781 series are an ultralow quiescent current (1μA), DVS, and miniaturized packaging. The TPS781 family are available in SON-6 and TSOT-23 packages. Figure 50 shows a typical MSP430 circuit powered by an LDO without DVS. Figure 51 is an MSP430 circuit using a TPS781 LDO that incorporates an integrated DVS, thus simplifying the circuit design. In a circuit without DVS, as Figure 50 illustrates, V_{CC} is always at 3.0V. When the MSP430 goes into sleep mode, V_{CC} remains at 3.0V; if DVS is applied, V_{CC} could be reduced in sleep mode. In Figure 51, the TPS781 LDO with integrated DVS maintains 3.6V V_{CC} until a logic high signal from the MSP430 forces V_{OUT} to level shift V_{OUT} from 3.6V down to 2.2V; thus reducing power in sleep mode.

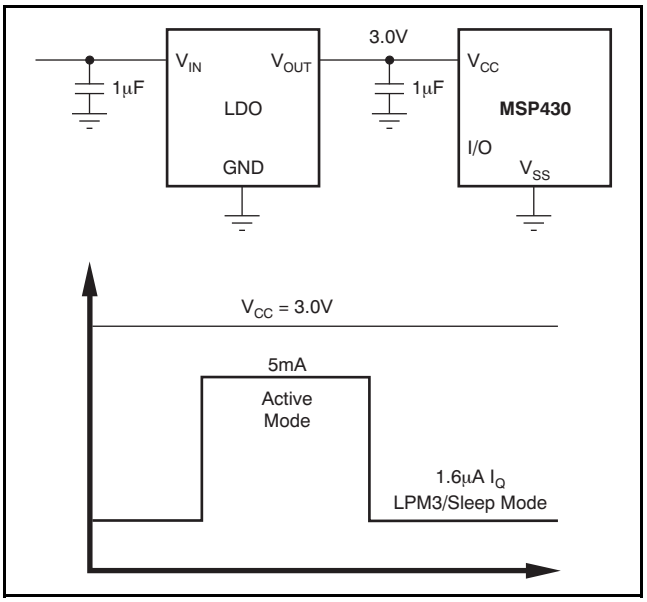


Figure 50. Typical LDO without DVS

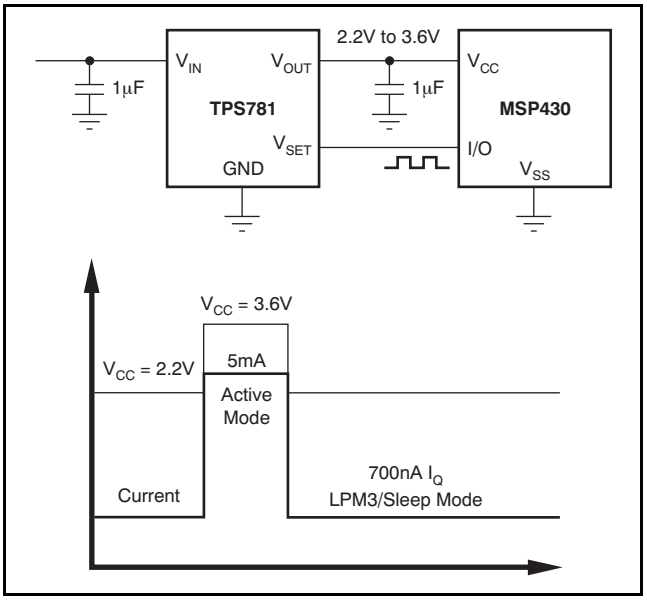


Figure 51. TPS781 with Integrated DVS

The other benefit of DVS is that it allows a higher V_{CC} voltage on the MSP430, increasing the clock speed and reducing the active mode dwell time.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS781 series are designed to be stable with standard ceramic capacitors with values of 1.0µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1µF.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS781 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS781 series has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, EN should be connected to the IN pin, as shown in Figure 52. Figure 53 shows both EN and V_{SET} connected to IN. The TPS781 series, with internal active output pull-down circuitry, discharges the output to within 5% V_{OUT} with a time (*t*) shown in Equation 3:

$$t = 3 \left(\frac{10k\Omega \times R_L}{10k\Omega + R_L} \right) \times C_{OUT} \quad (3)$$

Where:

R_L= output load resistance

C_{OUT} = output capacitance

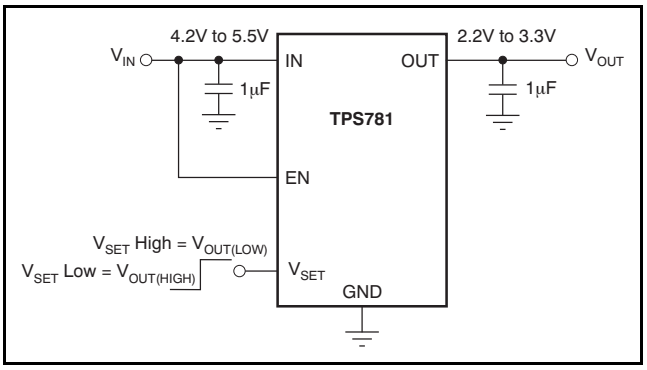


Figure 52. Circuit Showing EN Tied High when Shutdown Capability is Not Required

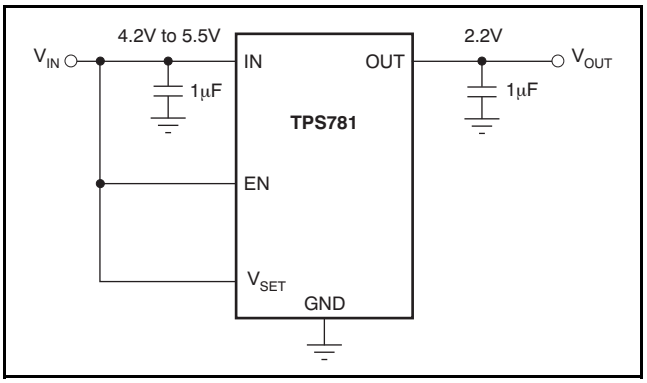


Figure 53. Circuit to Tie Both EN and V_{SET} High

DROPOUT VOLTAGE

The TPS781 series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section. Refer to application report SLVA207, *Understanding LDO Dropout*, available for download from www.ti.com.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. For more information, see Figure 42.

ACTIVE V_{OUT} PULL-DOWN

In the TPS781 series, the active pull-down discharges V_{OUT} when the device is off. However, the input voltage must be greater than 2.2V for the active pull-down to work.

MINIMUM LOAD

The TPS781 series are stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS781 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See Figure 41 for the load transient response.

THERMAL INFORMATION

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. Once the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS781 series has been designed to protect against overload conditions. However, it is not intended to replace proper heatsinking. Continuously running the TPS781 series into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS781 series are available from the Texas Instruments web site at www.ti.com through the TPS781 series product folders.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS78101DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEB	Samples
TPS78101DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEB	Samples
TPS78101DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEB	Samples
TPS78101DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEB	Samples
TPS781250200DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAN	Samples
TPS781250200DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAN	Samples
TPS781330220DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CED	Samples
TPS781330220DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CED	Samples
TPS781330220DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CED	Samples
TPS781330220DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CED	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

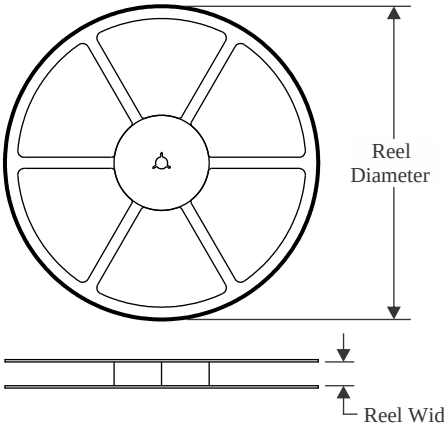
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

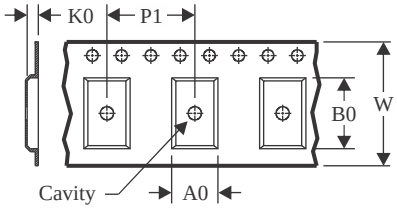
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

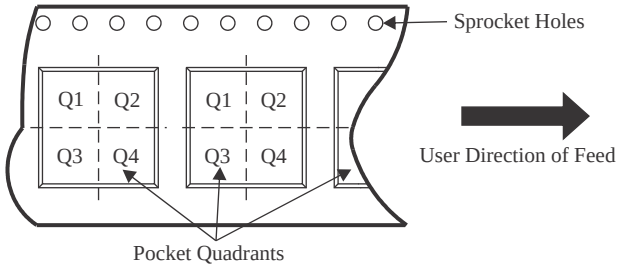


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

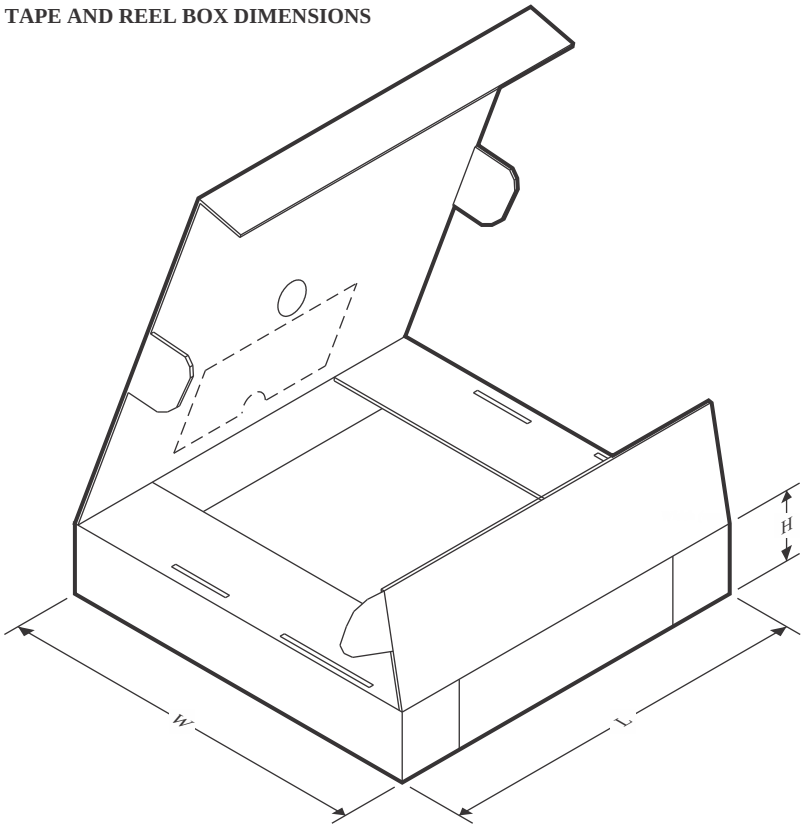


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78101DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78101DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78101DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS78101DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS78101DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS781250200DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS781250200DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS781330220DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS781330220DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS781330220DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS781330220DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS781330220DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS781330220DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

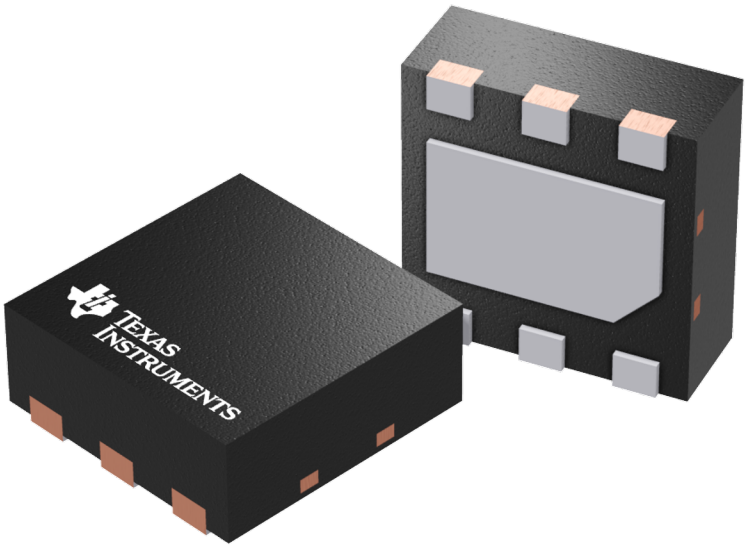


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78101DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78101DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78101DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS78101DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS78101DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS781250200DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS781250200DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS781330220DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS781330220DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS781330220DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS781330220DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS781330220DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS781330220DRVT	WSON	DRV	6	250	200.0	183.0	25.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



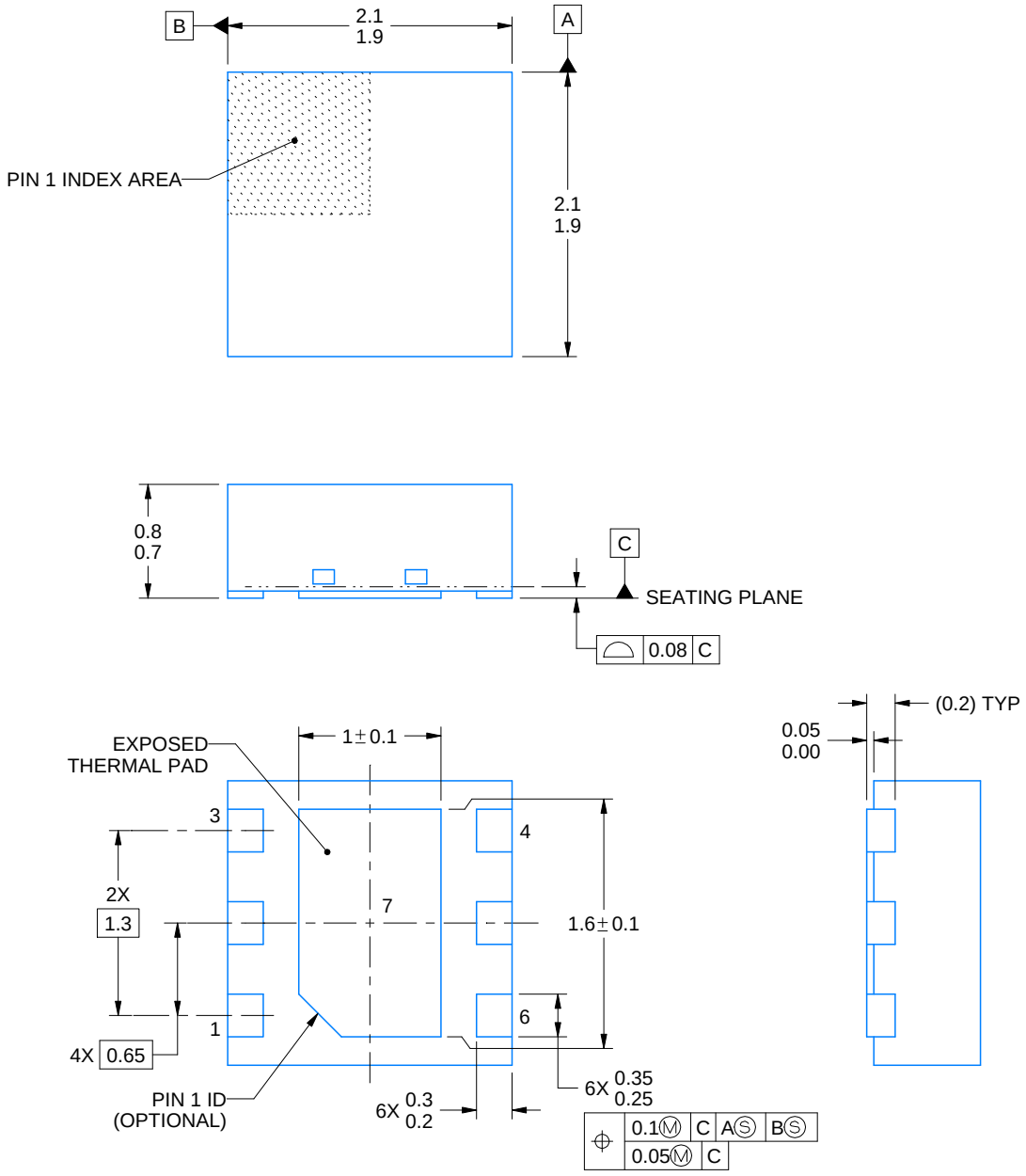
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

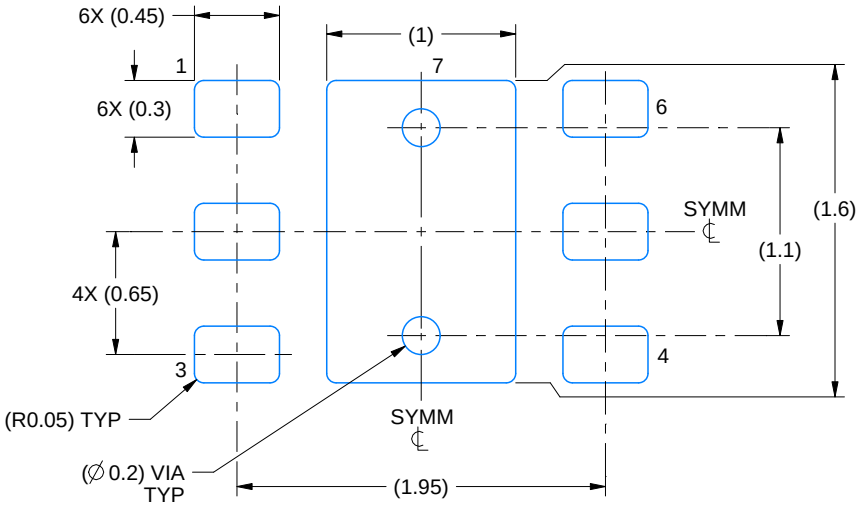
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

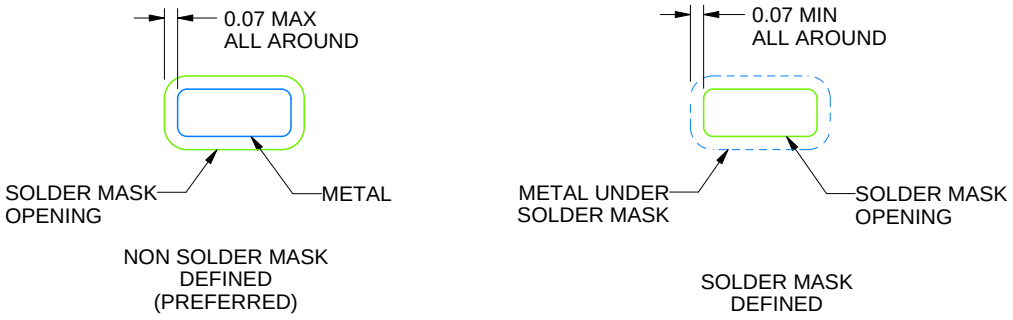


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

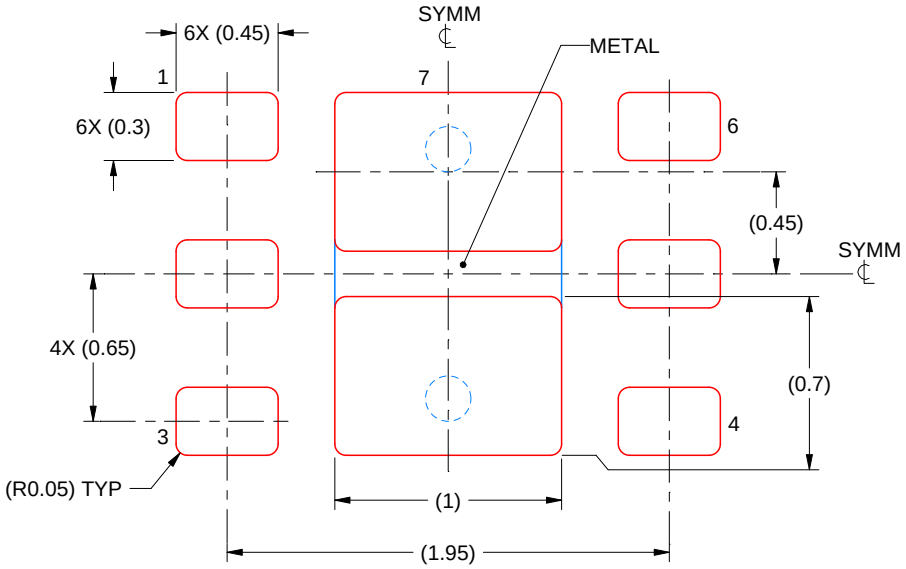
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

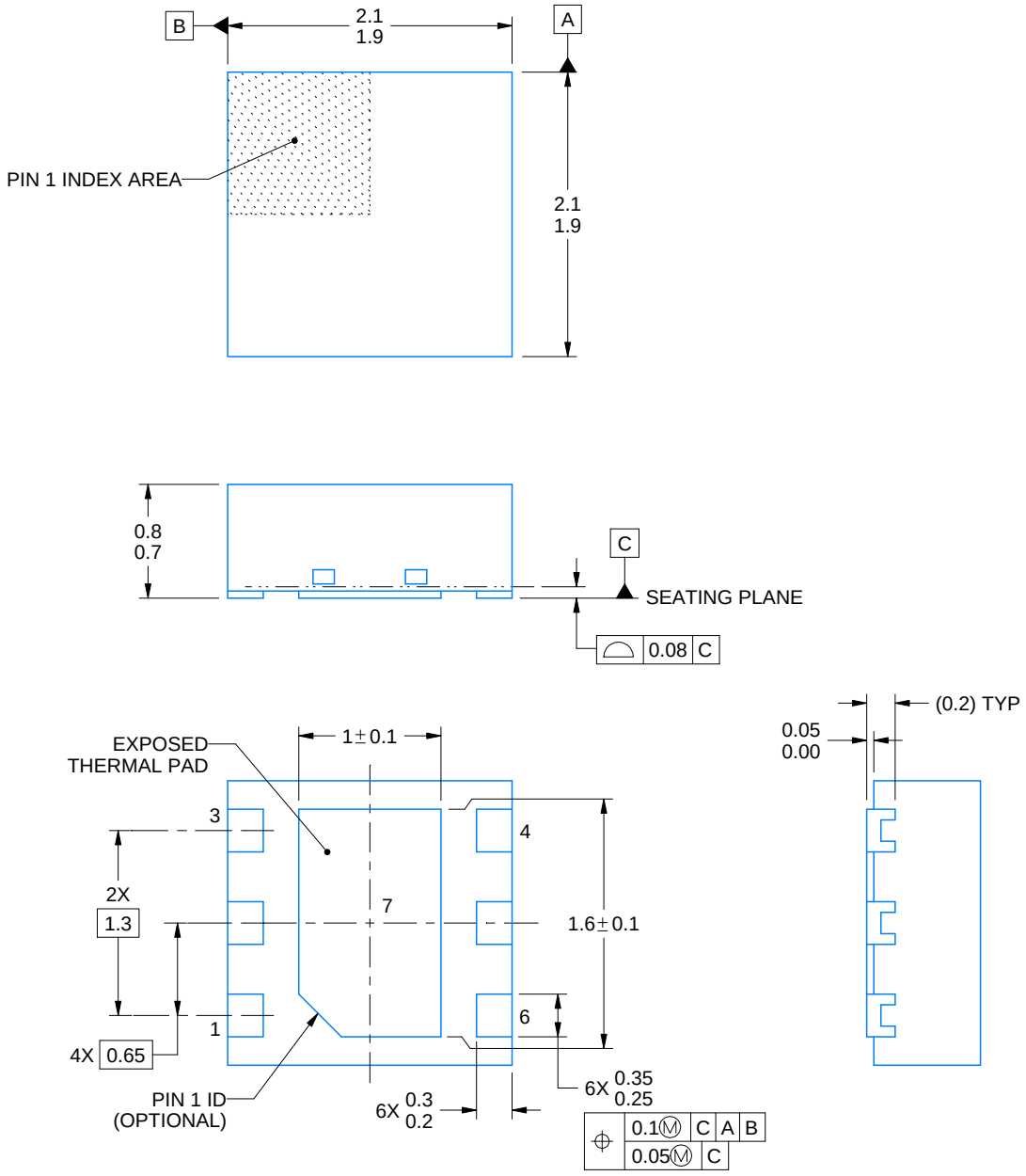
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

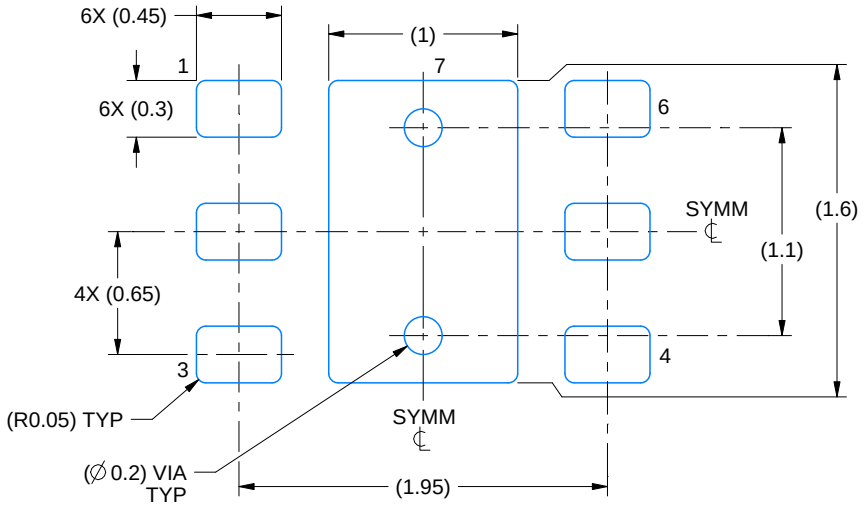
PLASTIC SMALL OUTLINE - NO LEAD



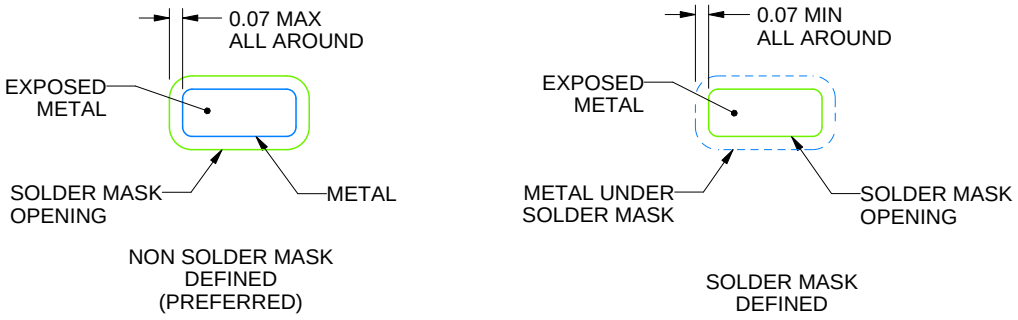
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

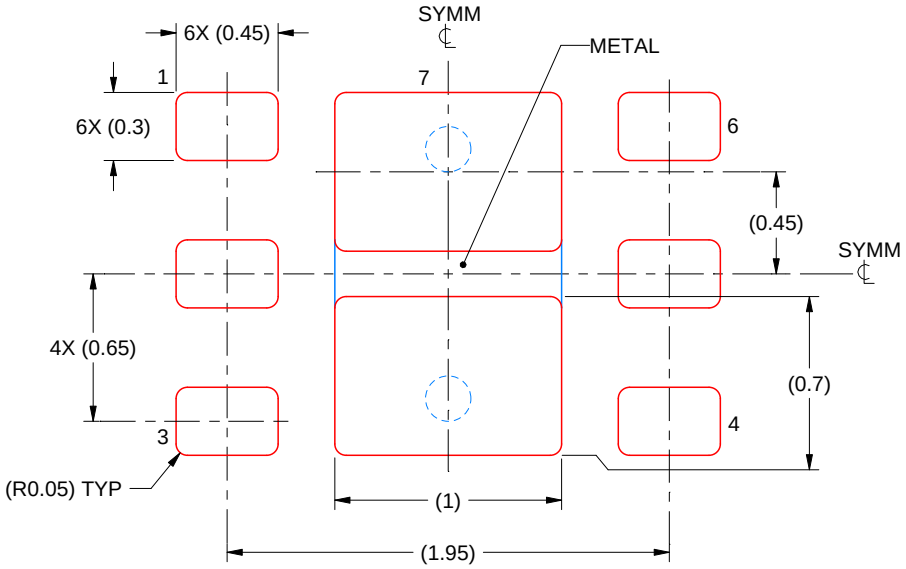


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

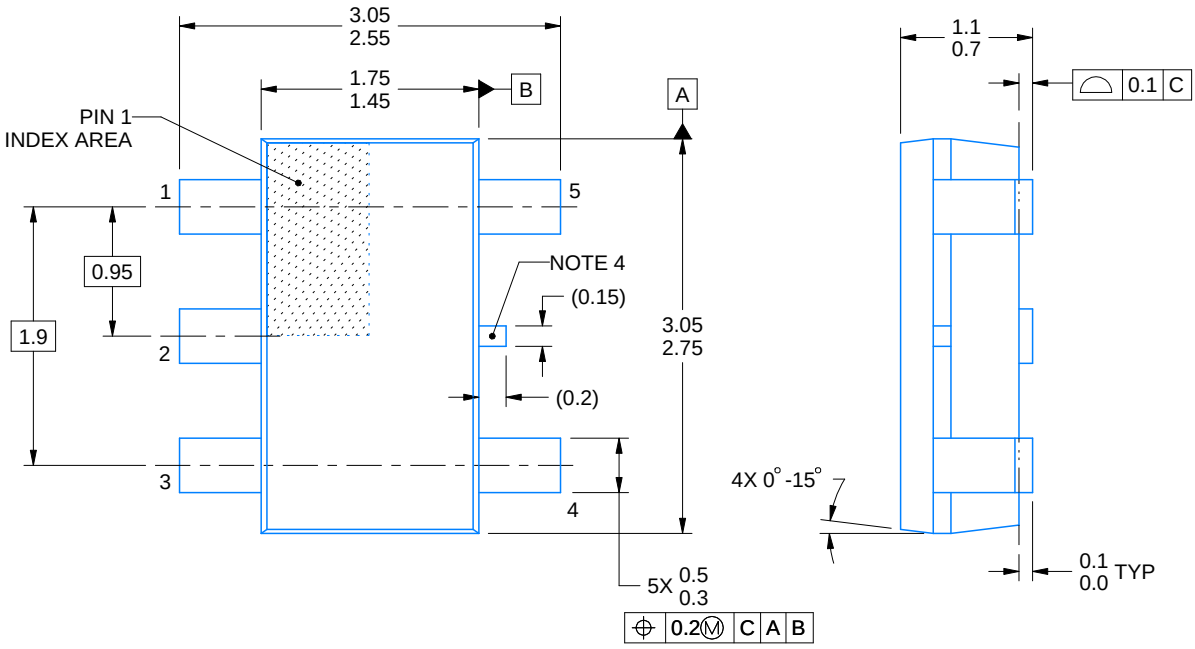
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

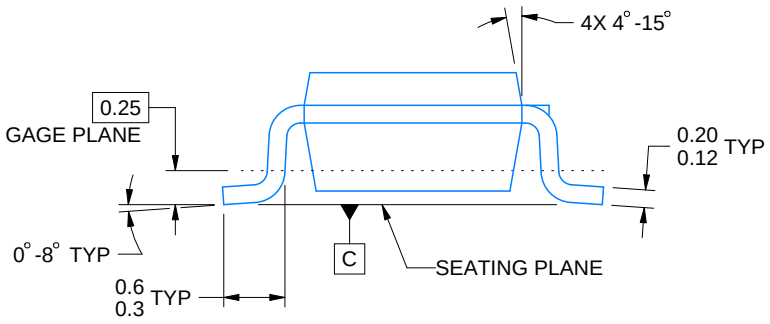
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

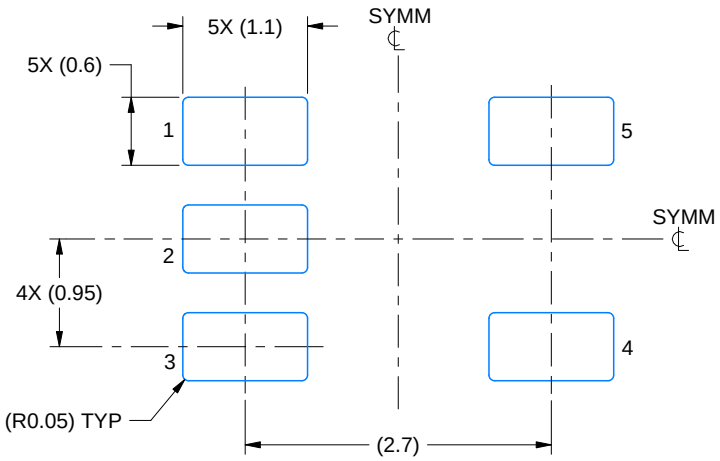




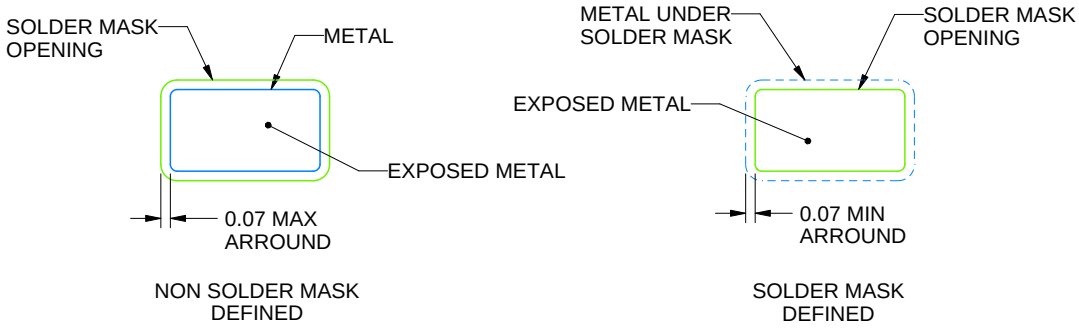
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

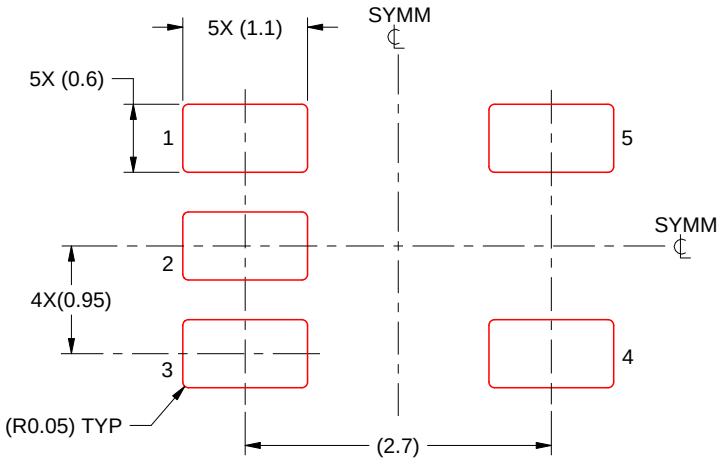


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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