TPS7A10 300mA 低输入电压、低输出电压、超低压降稳压器

1 特性

- 超低输入电压范围：0.75V 至 3.3V
- 可实现最低功率损耗的超低压降：
  - 在 300mA 下为 70mV（最大值）(V_{OUT} > 1.0V)，YKA 封装
- 低静态电流：
  - V_{IN} I_Q= 1.6μA（典型值）
  - V_{BIAS} I_Q= 6μA（典型值）
- 负载、线路和温度上的精度为 1.5%
- 高 PSRR：频率 1kHz 时为 60dB
- 可提供固定输出电压：
  - 0.5V 至 3.0V（阶跃 为 50mV）
- V_{BIAS} 范围：1.7V 至 5.5V
- 封装：
  - 0.74mm × 1.09mm WCSP-5
  - 1.50mm × 1.50mm WSON-6
- 内置软启动功能，具有单调 V_{OUT} 上升
- 有源输出放电

2 应用

- 智能手表、健身追踪器
- 无线耳机和耳塞
- 摄像头模块
- 智能手机和平板电脑
- 便携式医疗设备

3 说明

TPS7A10 是一款超小型低静态电流低压降稳压器 (LDO)，它能够实现 300mA 的拉电流并具有出色的交流性能（负载和线路瞬态响应）。该器件具有 0.75V 至 3.3V 的输入范围以及 0.5V 至 3.0V 的输出范围，并在负载、线路和温度上具有 1.5% 的极高精度。此性能非常适合于为更低的现代 MCU 内核电压和模拟传感器供电。

主要电源路径通过 V_{IN}，可连接至高于输出电压的值低至 70mV 的电源。该器件使用一个用于为 LDO 的内部电路供电的附加 V_{BIAS} 电源轨，支持极低的输入电压。V_{IN} 和 V_{BIAS} 分别消耗 1.6μA 和 6μA 的极低静态电流。低 I_Q 和超低压降 特性 有助于提高功耗敏感型应用中解决方案的 效率。例如，V_{IN} 可以是高效直流/直流降压稳压器的输出，而 V_{BIAS} 引脚可以连接至一个可再充电电池。

TPS7A10 配备了一个有源下拉电路，用于在处于禁用状态时对输出进行快速放电，并提供已知的启动状态。

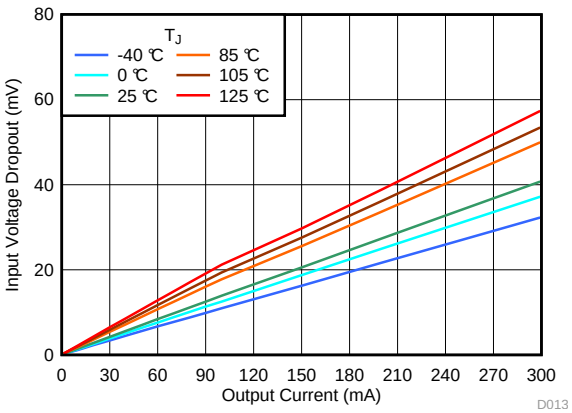
TPS7A10 可采用超小型 5 引脚 DSBGA (YKA) 封装，从而使其非常适合空间受限的 应用。该器件还可采用 6 引脚 WSON (DSE) 封装。

器件信息(1)

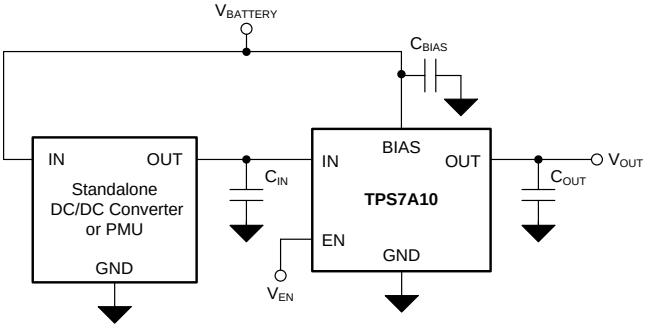
器件型号	封装	封装尺寸（标称值）
TPS7A10	WSON (6)	1.50mm × 1.50mm
	DSBGA (5)	0.74mm × 1.09mm（0.35mm 间距）

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

压降与 I_{OUT} 和温度间的关系（YKA 封装）



典型应用电路



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2018) to Revision B **Page**

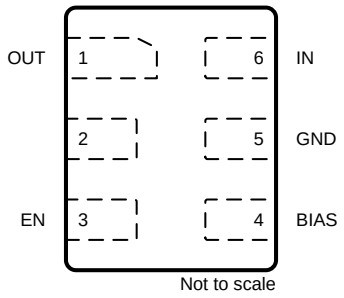
- 已添加 *YKA 封装* 添加至以下章节的*可实现最低功率损耗的超低压降* 项目的子项目： ... 1
- 已添加 在 *部分中添加了最后一个句子说明* 部分的关断相关文字 ... 1
- 已更改 将 WSON (DSE) 封装从“预告信息”更改为“生产数据（正在供货）” ... 1
- 已添加 *YKA 封装* 添加至*压降与 I_{OUT} 和温度间的关系（YKA 封装）* 一图的标题中 ... 1
- 已添加 *YKA Package* to captions of *Output Accuracy Over Temperature, YKA Package* and *Output Accuracy Over Temperature, YKA Package* figures ... 7
- 已添加 *Output Accuracy Over Temperature, DSE Package* and *Output Accuracy Over Temperature, DSE Package* figures ... 7
- 已添加 *YKA Package* to caption of *Dropout vs I_{OUT} and Temperature, YKA Package* figure ... 7
- 已添加 *Dropout vs I_{OUT} and Temperature, DSE Package* figure ... 8

Changes from Original (March 2018) to Revision A **Page**

- 已更改 从“预告信息”更改为“生产数据（正在供货）” ... 1

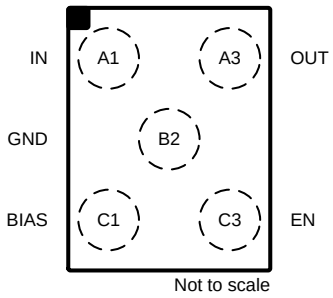
5 Pin Configuration and Functions

DSE Package
6-Pin WSON
Top View



Not to scale

YKA Package
5-Pin DSBGA
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSE	YKA		
IN	6	A1	I	Input pin. For best transient response and to minimize input impedance, use the recommended or larger value ceramic capacitor from IN to ground. as listed in the *Recommended Operation Conditions*. Place the input capacitor as close as possible to input of the device.
OUT	1	A3	O	Regulated output pin. A capacitor is required from OUT to ground for stability. For best transient response, use larger than the minimum recommended value ceramic capacitor. Follow the recommended capacitor value as listed in the *Recommended Operation Conditions*. Place the output capacitor as close as possible to output of the device.
GND	5	B2	—	Ground pin. This pin must be connected to ground.
BIAS	4	C1	I	BIAS pin. This pin enables the use of low-input voltage, low-output voltage conditions, (LILO). For best response, use the recommended or larger value ceramic capacitor from BIAS to ground as listed in the *Recommended Operation Conditions*. Place the bias capacitor as close as possible to input of the device.
EN	3	C3	I	Enable pin. Driving this pin to logic high enables the device. Driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN or BIAS; however, connecting EN to IN is only acceptable if the V_{IN} voltage is greater than 0.9 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	Supply, V_{IN}	–0.3	3.6	V
	Enable, V_{EN}	–0.3	6.0	
	Bias, V_{BIAS}	–0.3	6.0	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3(2)	
Current	Maximum output current		Internally limited	A
Temperature	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is 3.6 or (V_{IN} + 0.3) , whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.75		3.3	V
V_{BIAS}	Bias voltage	1.7		5.5	V
V_{OUT}	Output voltage	0.5		3.0	V
I_{OUT}	Peak output current	0		300	mA
C_{IN}	Input capacitor	2.2			µF
C_{BIAS}	Bias capacitor		0.1		µF
C_{OUT} (1)	Output capacitor	2.2		22	µF
T_J	Operating junction temperature	–40		125	℃

(1) Maximum ESR must be lower than 250 mΩ

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A10		UNIT
		DSE (WSON)	YKA (WSCP)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.8	169.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82.9	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.0	55.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.4	55.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* .

6.5 Electrical Characteristics

over T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Nominal Accuracy	T_J = 25°C	–0.5		0.5	%
	Accuracy over temperature	–20°C ≤ T_J ≤ 85, DSE package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.25		1.25	
		–40°C ≤ T_J ≤ 85, YKA package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.25		1.25	
		–40°C ≤ T_J ≤ 125, DSE and YKA package $V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V, $V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V, 1 mA ≤ I_{OUT} ≤ 300 mA	–1.5		1.5	
ΔV_{OUT} / ΔV_{IN}	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 3.3 V		0.001		%/V
ΔV_{OUT} / ΔV_{BIAS}	V_{BIAS} line regulation	$V_{OUT(NOM)}$ + 1.4 V ≤ V_{BIAS} ≤ 5.5 V		0.03		%/V
ΔV_{OUT} / ΔI_{OUT}	Load regulation	0.1 mA ≤ I_{OUT} ≤ 300 mA		0.2		%/A
$I_{Q(BIAS)}$	Bias pin current	T_J = 25°C, I_{OUT} = 0 mA	3	6	8	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			11	
		I_{OUT} = 0 mA			14	
		I_{OUT} = 300 mA			60	
$I_{Q(IN)}$	Input pin current(1)	T_J = 25°C, I_{OUT} = 0 mA		1.6	2.1	µA
		–40°C < T_J < 85°C, I_{OUT} = 0 mA			2.3	
		I_{OUT} = 0 mA			2.6	
		I_{OUT} = 300 mA			9	
$I_{SHDN(BIAS)}$	V_{BIAS} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			400	nA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1200	
$I_{SHDN(IN)}$	V_{IN} shutdown current	–40°C < T_J < 85°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			1	µA
		–40°C < T_J < 125°C, V_{IN} = 3.3 V, V_{BIAS} = 5.5 V, V_{EN} ≤ 0.4 V			3	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$, YKA package	325	450	600	mA
		V_{OUT} = 0.9 × $V_{OUT(NOM)}$, DSE package	350	450	625	mA
I_{SC}	Short circuit current limit	V_{OUT} = 0 V		150		mA
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 300 mA, YKA package		40	70	mV
		V_{IN} = $V_{OUT(NOM)}$ – 0.1 V, I_{OUT} = 300 mA, DSE package		55	90	
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	I_{OUT} = 300 mA		0.85	1.05	V
		I_{OUT} = 150 mA		0.75	0.95	

(1) This current flowing from V_{IN} to GND.
(2) Dropout is not measured for V_{OUT} < 1.0 V

Electrical Characteristics (continued)

over T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = 1.0 V, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); all typical values are at T_J = 25°C .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} PSRR	V_{IN} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		60		dB
		f = 100 kHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		36		
		f = 1 MHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		32		
		f = 1.5 MHz, V_{OUT} = 1.1 V, I_{OUT} = 50 mA		35		
V_{BIAS} PSRR	V_{BIAS} power-supply rejection ratio	f = 1 kHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		60		dB
		f = 100 kHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		40		
		f = 1 MHz, V_{OUT} = 1.1 V, I_{OUT} = 300 mA		35		
V_n	Output voltage noise	Bandwidth = 10 Hz to 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 50 mA		93.9		μV_{RMS}
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} rising	1.46	1.54	1.63	V
		V_{BIAS} falling	1.35	1.44	1.55	
$V_{UVLO\_HYST(BIAS)}$	Bias supply hysteresis	V_{BIAS} hysteresis		80		mV
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising	645	675	710	mV
		V_{IN} falling	565	600	640	mV
$V_{UVLO\_HYST(IN)}$	Input supply hysteresis	V_{IN} hysteresis		75		mV
t_{STR}	Start-up time(3)			525	1200	µs
$V_{HI(EN)}$	EN pin logic high voltage		0.9			V
$V_{LO(EN)}$	EN pin logic low voltage				0.4	V
I_{EN}	EN pin current	EN = 5.5 V		10		nA
$R_{PULLDOWN}$	Pulldown resistor	V_{BIAS} = 3.3 V, P version only		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature rising		160		°C
		Reset, temperature falling		145		

(3) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.

6.6 Typical Characteristics

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

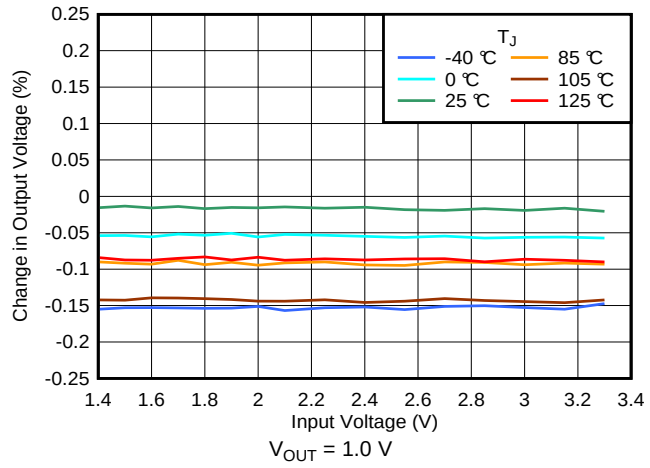


图 1. Output Accuracy Over Temperature, YKA Package

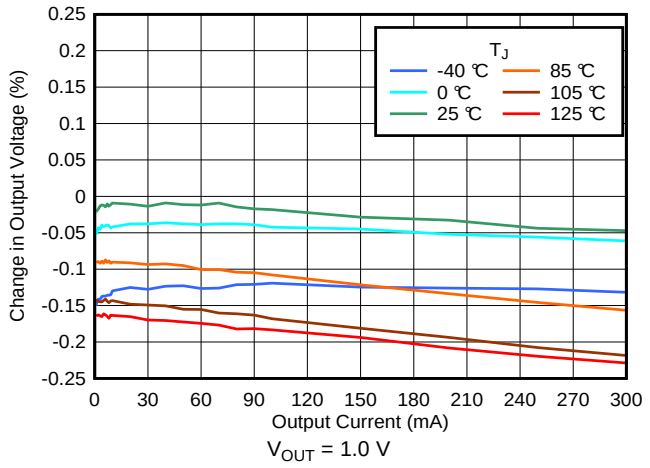


图 2. Output Accuracy Over Temperature, YKA Package

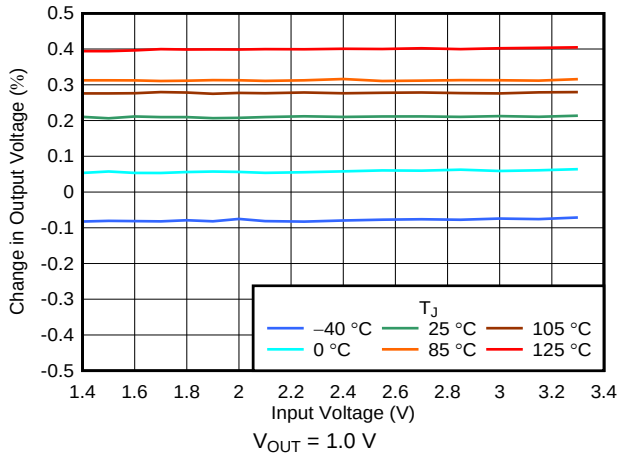


图 3. Output Accuracy Over Temperature, DSE Package

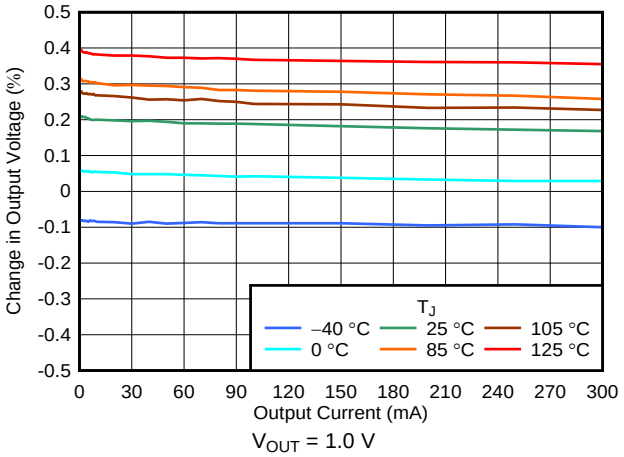


图 4. Output Accuracy Over Temperature, DSE Package

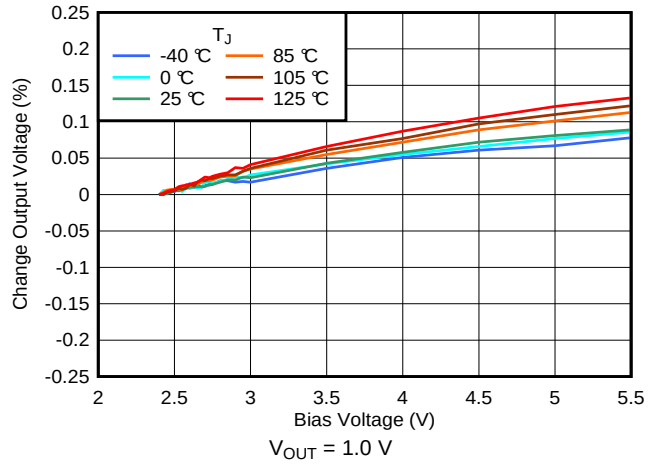


图 5. Output Accuracy Over Temperature and V_{BIAS}

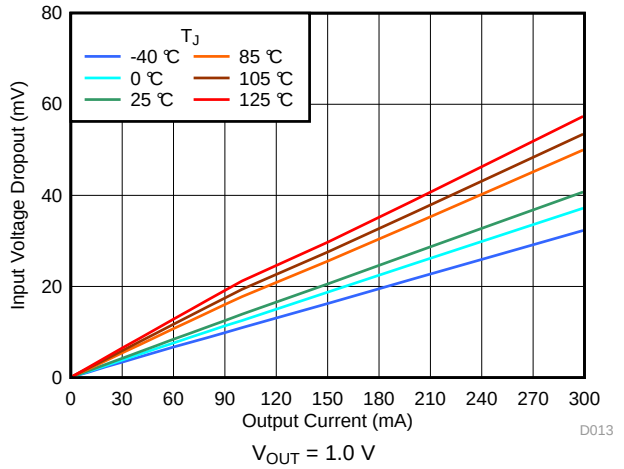


图 6. Dropout vs I_{IOUT} and Temperature, YKA Package

Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

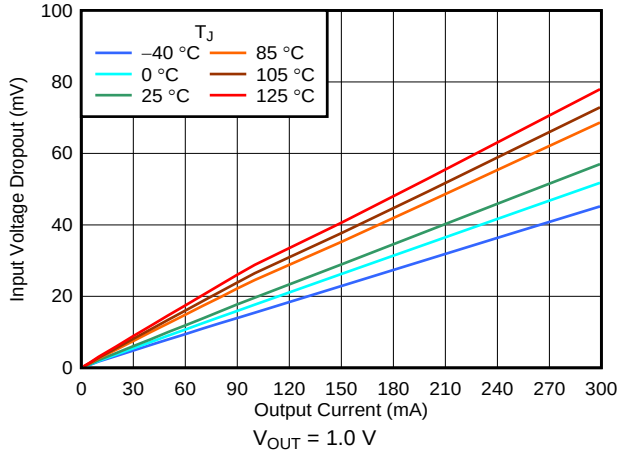


图 7. Dropout vs I_{IOUT} and Temperature, DSE Package

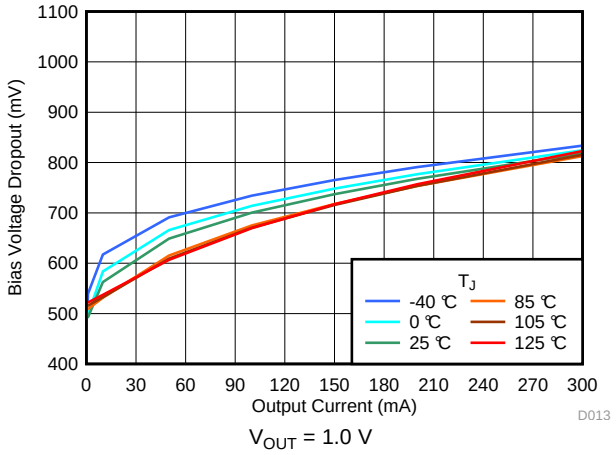


图 8. Dropout vs V_{BIAS} and Temperature

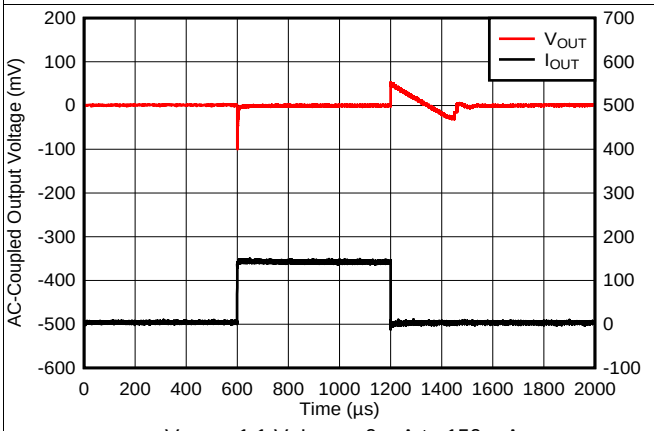


图 9. I_{OUT} Transient

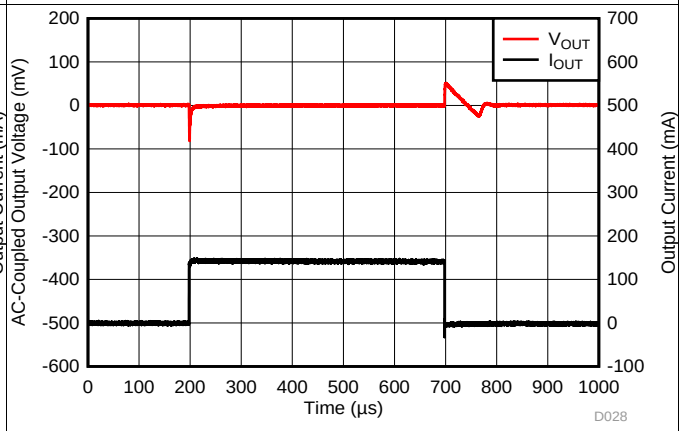


图 10. I_{OUT} Transient

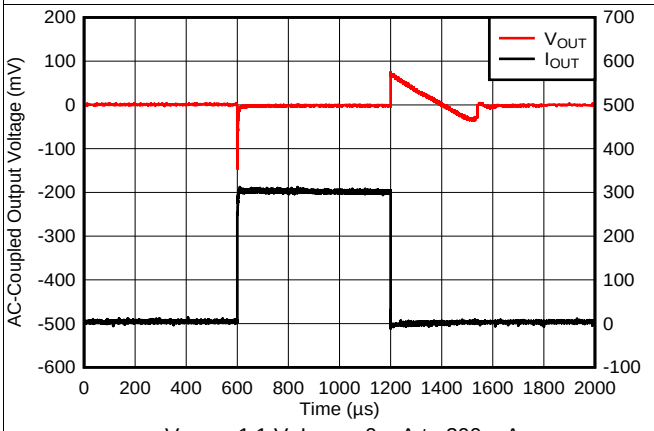


图 11. I_{OUT} Transient

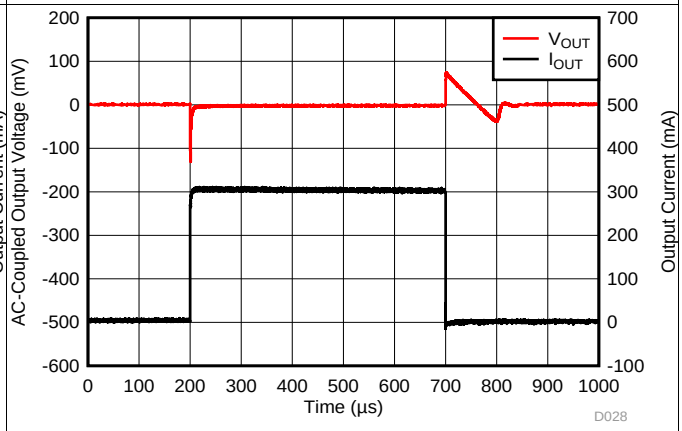
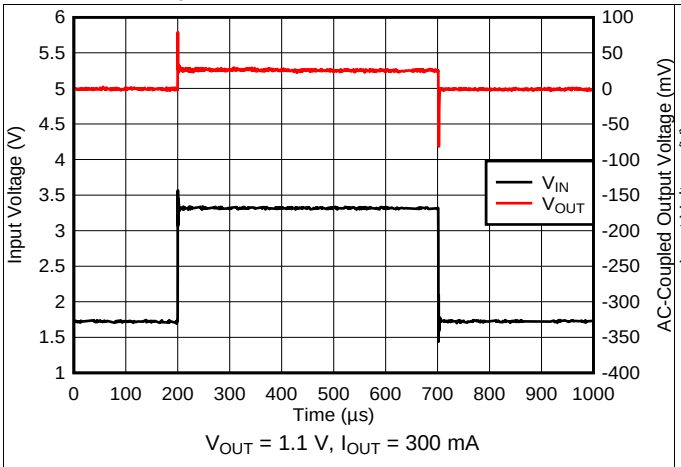


图 12. I_{OUT} Transient

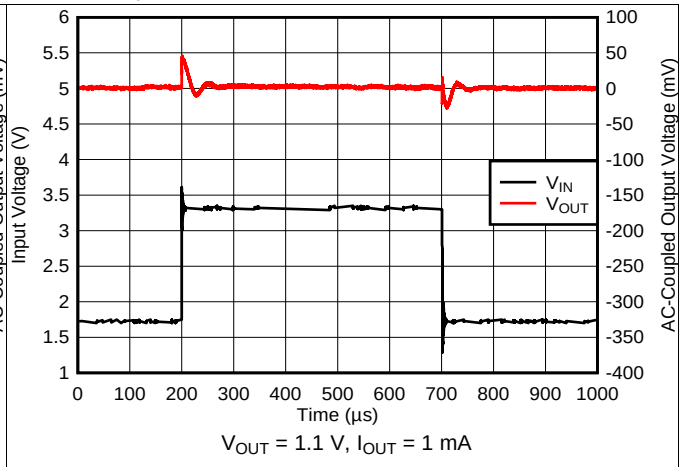
Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



V_{OUT} = 1.1 V, I_{OUT} = 300 mA

图 13. V_{IN} Transient



V_{OUT} = 1.1 V, I_{OUT} = 1 mA

图 14. V_{IN} Transient

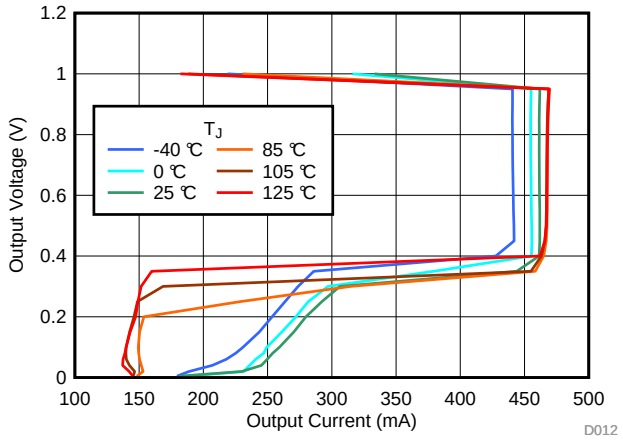
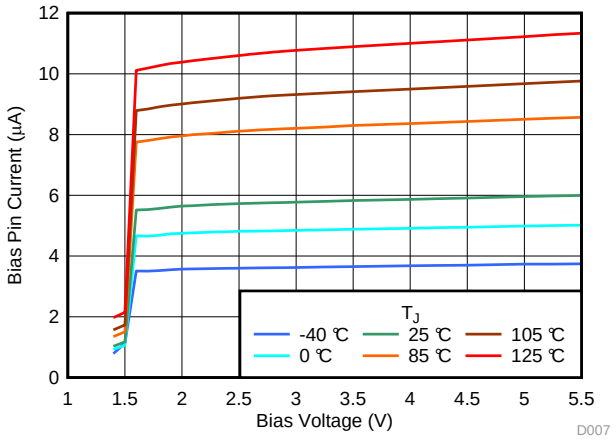
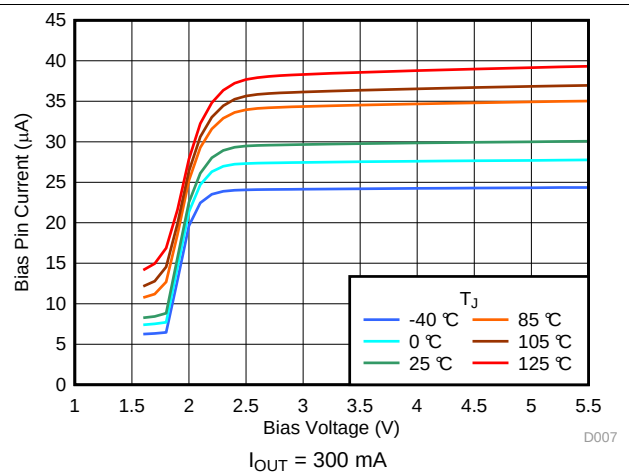


图 15. Foldback Current Limit Over Temperature



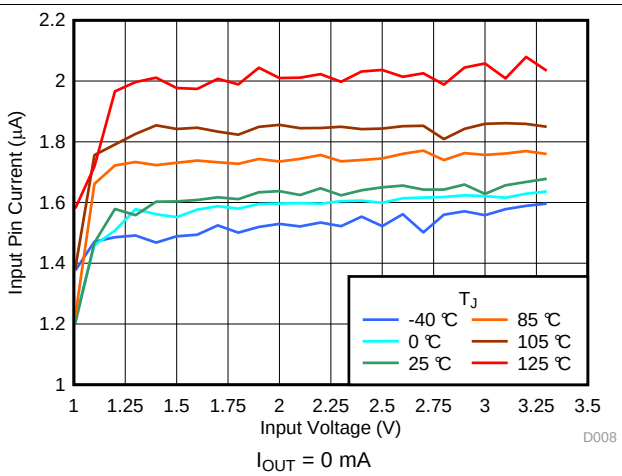
I_{OUT} = 0 mA

图 16. I_Q (V_{BIAS}) Over Temperature



I_{OUT} = 300 mA

图 17. I_Q (V_{BIAS}) Over Temperature

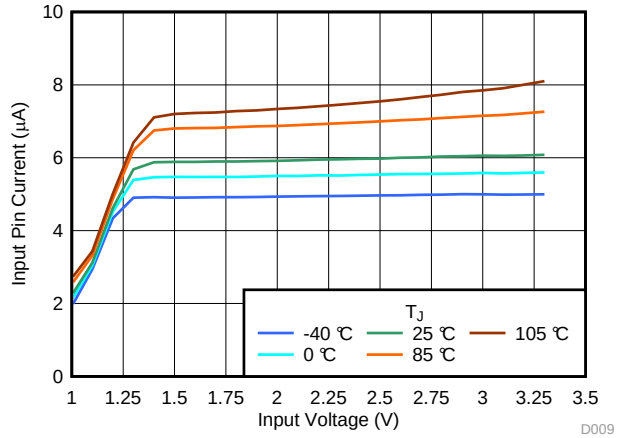


I_{OUT} = 0 mA

图 18. I_Q (V_{IN}) Over Temperature

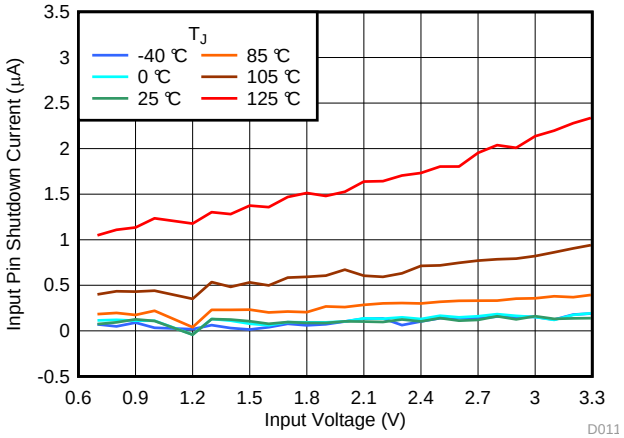
Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



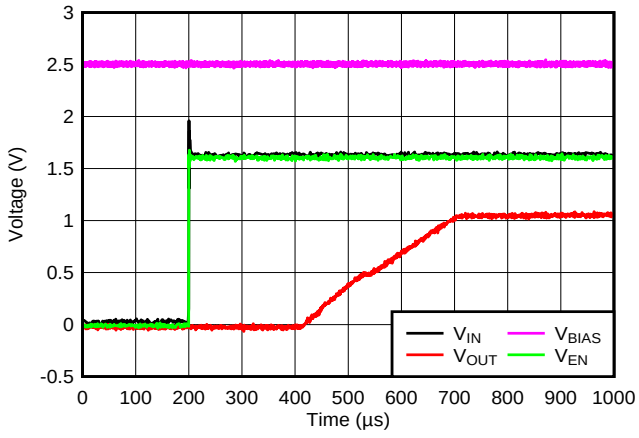
I_{OUT} = 300 mA

图 19. I_Q (V_{IN}) Over Temperature



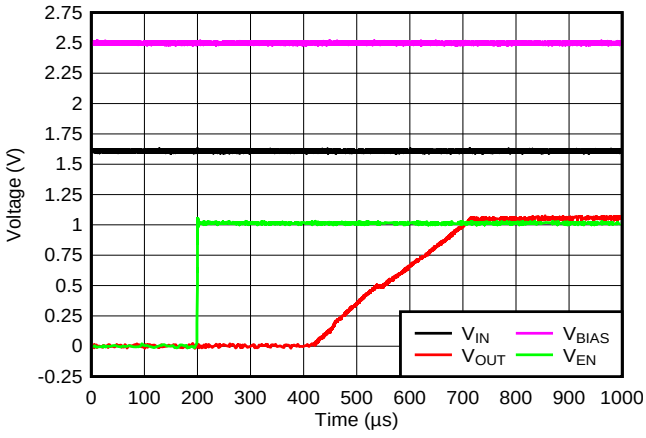
V_{OUT} = 1.0 V, V_{EN} < 0.4 V

图 20. I_{SHDN} (V_{IN}) Over Temperature



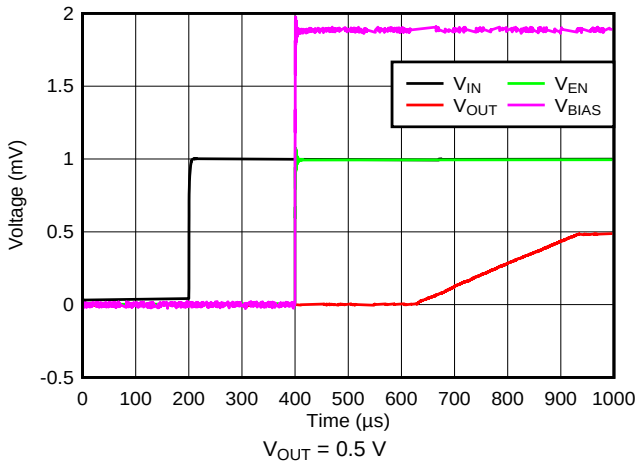
V_{OUT} = 1.1 V

图 21. Startup With V_{EN} = V_{IN}



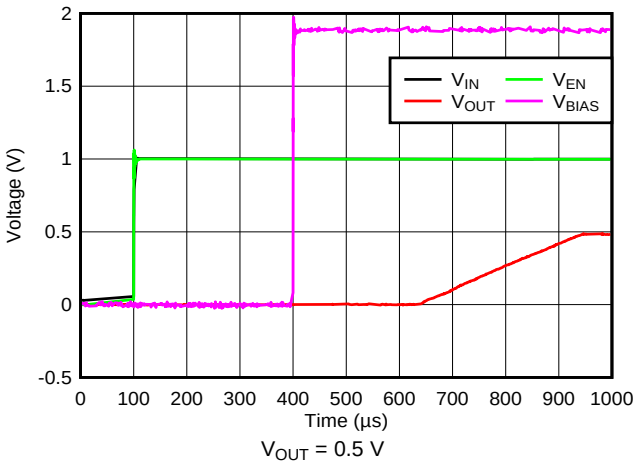
V_{OUT} = 1.1 V

图 22. Startup With Separated V_{EN}



V_{OUT} = 0.5 V

图 23. Startup With V_{EN} and V_{BIAS} Powering Up Simultaneously

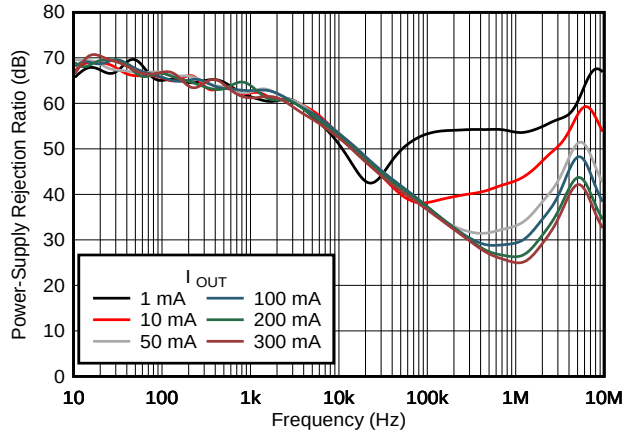


V_{OUT} = 0.5 V

图 24. Startup With V_{BIAS} Powering Up After V_{IN} and V_{EN}

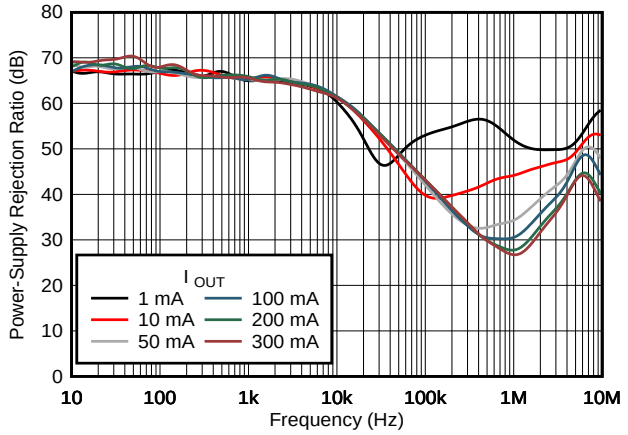
Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



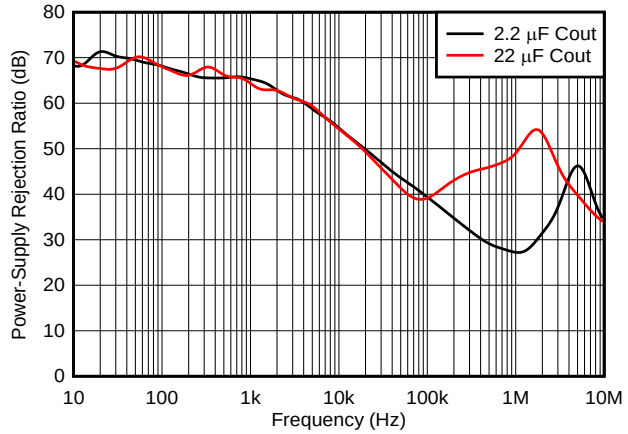
C_{IN} = 0 µF, V_{OUT} = 1.1 V, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

图 25. PSRR vs Frequency and I_{OUT}



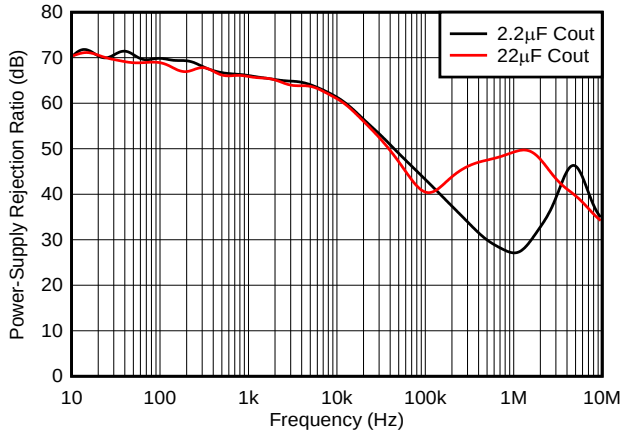
C_{IN} = 0 µF, V_{OUT} = 0.5 V, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

图 26. PSRR vs Frequency and I_{OUT}



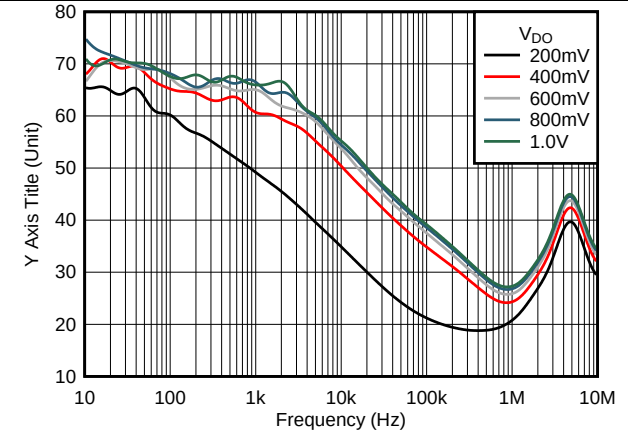
C_{IN} = 0 µF, V_{OUT} = 1.1 V, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

图 27. PSRR vs Frequency and C_{OUT}



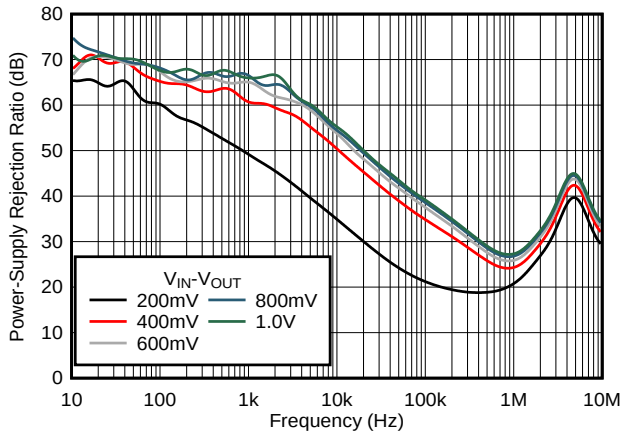
C_{IN} = 0 µF, V_{OUT} = 0.5 V, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

图 28. PSRR vs Frequency and C_{OUT}



C_{IN} = 0 µF, V_{OUT} = 1.1 V, I_{OUT} = 300 mA, V_{BIAS} = 2.5 V, C_{BIAS} = 0.1 µF

图 29. PSRR vs Frequency and V_{DO}

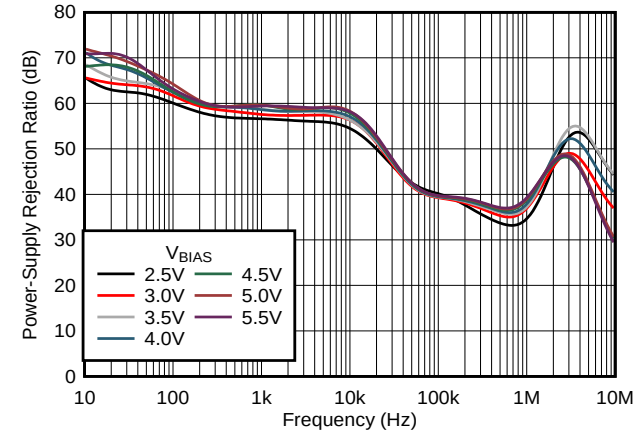


C_{IN} = 0 µF, V_{OUT} = 0.5 V, I_{OUT} = 300 mA, V_{BIAS} = 1.9 V, C_{BIAS} = 0.1 µF

图 30. PSRR vs Frequency and V_{DO}

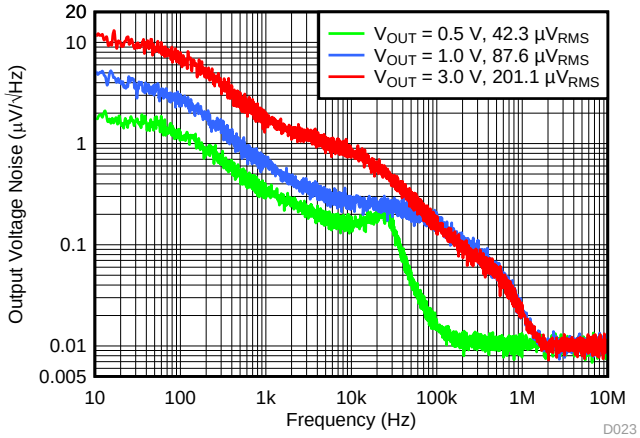
Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C



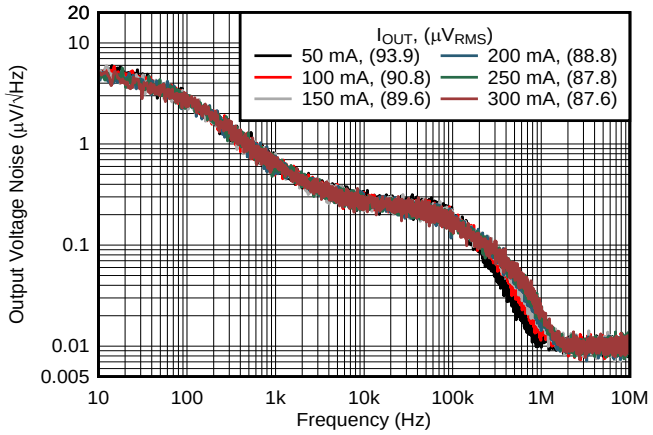
V_{OUT} = 1.1 V, I_{OUT} = 300 mA, C_{BIAS} = 0 µF

图 31. V_{BIAS} PSRR vs Frequency and V_{BIAS}



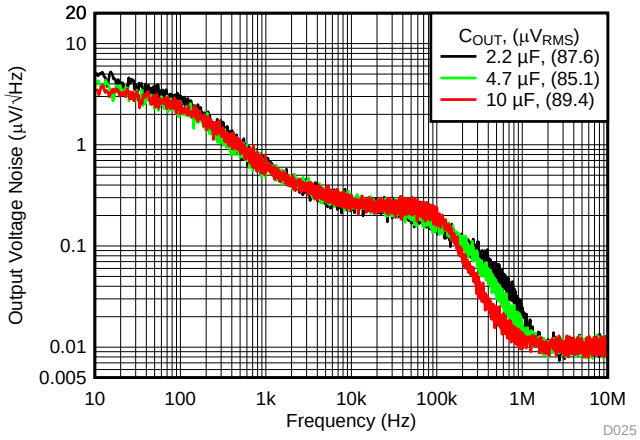
I_{OUT} = 300 mA

图 32. Output Noise vs Frequency and V_{OUT}



V_{OUT} = 1.0 V, V_{BIAS} = 2.5 V

图 33. Output Noise vs Frequency and I_{OUT}



V_{OUT} = 1.0 V, I_{OUT} = 300 mA

图 34. Output Noise vs Frequency and C_{OUT}

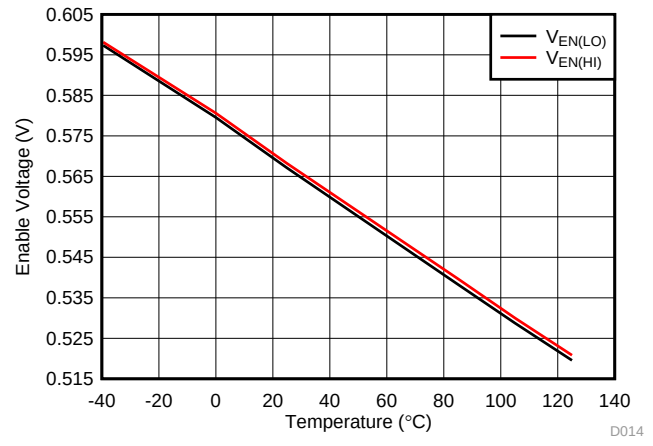


图 35. Enable High and Low Thresholds vs Temperature

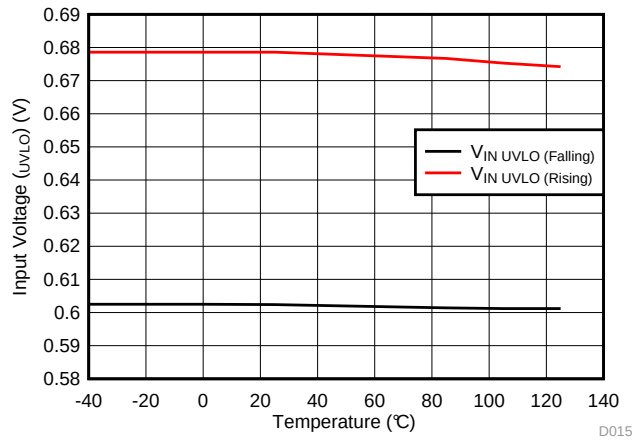


图 36. $V_{UVLO(IN)}$ Rising and Falling Thresholds vs Temperature

Typical Characteristics (接下页)

at T_J = –40 °C to +125 °C, V_{IN} = $V_{OUT(NOM)}$+ 0.5 V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and C_{BIAS} = 0.1 µF (unless otherwise noted); typical values are at T_J = 25°C

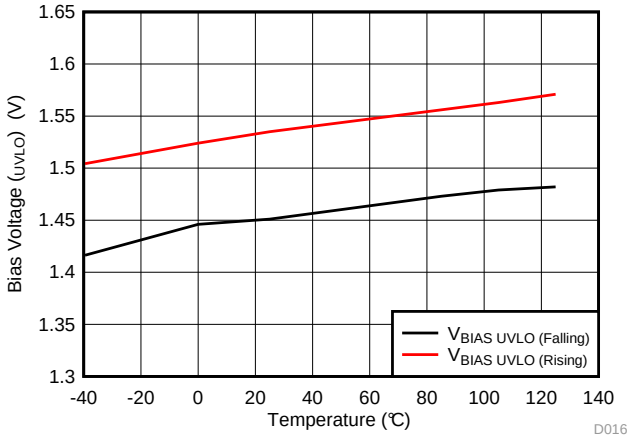


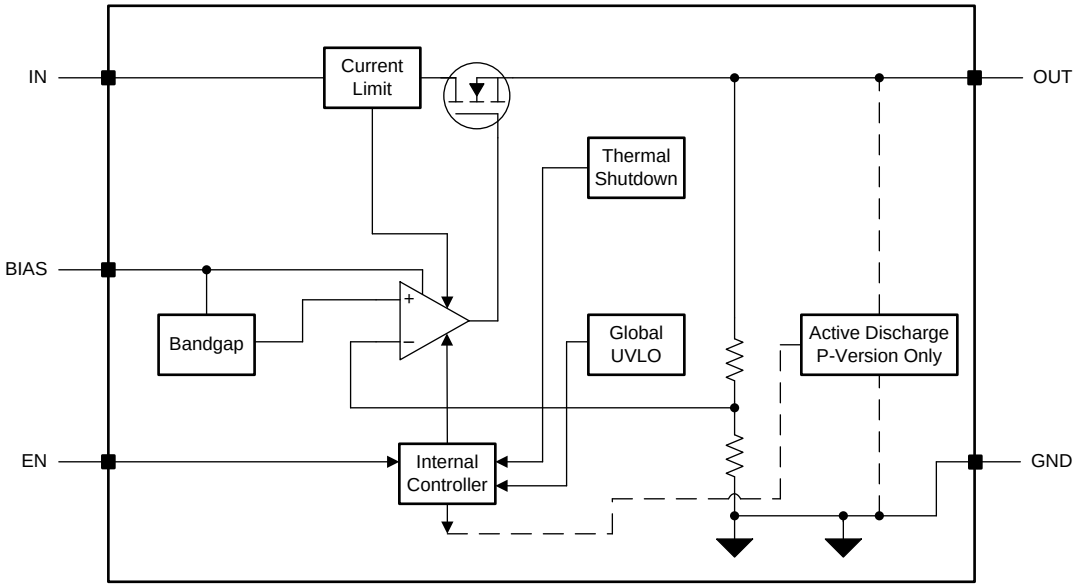
图 37. $V_{UVLO(BIAS)}$ Rising and Falling Thresholds vs Temperature

7 Detailed Description

7.1 Overview

The TPS7A10 is a low input, ultra-low dropout, and low quiescent current linear regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications. The implementation of the BIAS pin on the TPS7A10 vastly improves efficiency of low-voltage output applications by allowing the use of a preregulated, low-voltage input supply that offers sub-band-gap output voltages. The high power-supply rejection ratio (PSRR), low noise, low ground pin current, and ultra-small packaging make this device suitable for ultra-portable applications. This device also offers high output voltage accuracy of 1.5% over the recommended junction temperature range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excellent Transient Response

The TPS7A10 responds quickly to a transient on the input supply (line transient) or the output current (load transient) that results from the device high input impedance and low output impedance across frequency. This same capability also means that the device has a high power-supply rejection ratio (PSRR) and low internal noise floor (e_n). The low-dropout regulator (LDO) approximates an ideal power supply in ac (small-signal) and dc (large-signal) conditions.

The choice of external component values optimizes the small- and large-signal response; see the *Input and Output Capacitor Requirements* section for proper selection.

7.3.2 Global Undervoltage Lockout (UVLO)

The TPS7A10 uses two undervoltage lockout (UVLO) circuits: one on the BIAS pin and one on the IN pin to prevent the device from turning on before both V_{BIAS} and V_{IN} rise above their lockout voltages. The two UVLO signals are connected internally through an AND gate, as shown in 图 38. This internal connection allows the device to be turned off when either rail is below its lockout voltage.

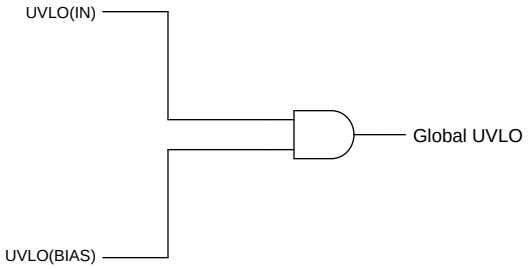


图 38. Global UVLO circuit

7.3.3 Active Discharge

The active discharge option (P version only) have internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled in order to actively discharge the output voltage. The active discharge circuit is activated by driving the enable pin to logic low to disable the device, or when the device is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. 公式 1 calculates the discharge time constant:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply collapses because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.4 Enable

The enable pin for this device is active high. The output of the device is turned on when the enable pin voltage is greater than the EN pin logic high voltage, and the output of the device is turned off when the enable pin voltage is less than the EN pin voltage logic low .

The EN pin can be tied to the IN pin, the BIAS pin, or can be driven separately to enable and disable the device; however, connecting the EN pin to the IN pin is only acceptable if the V_{IN} voltage is greater than 0.9 V.

Feature Description (接下页)

7.3.5 Sequencing Requirement

The V_{IN}, V_{BIAS}, and V_{EN} voltages can be sequenced in any order without causing damage to the device. The start up is always monotonic regardless of the sequencing order or the ramp rates of IN, BIAS, and EN pins. For optimum device performance, have V_{BIAS} present before enabling the device in any sequence order between V_{IN} and V_{EN} because the device internal circuitry is powered off the V_{BIAS}, refer to *Recommended Operating Conditions* for proper voltage ranges of V_{IN}, V_{BIAS}, and V_{EN}.

7.3.6 Internal Foldback Current Limit

The internal foldback current limit circuit is used to protect the LDO against high-load current faults or shorting events. The foldback mechanism lowers the current limit as the output voltage decreases, and limits power dissipation during short-circuit events while still allowing for the device to operate at the rated output current; see 图 15.

For example, when V_{OUT} is 90% of $V_{OUT(nom)}$, the current limit is I_{CL} (typical); however, if V_{OUT} is forced to 0 V, the current limit is I_{SC} (typical).

In many LDOs, the foldback current limit can prevent start up into a constant-current load or a negatively-biased output. A *brick-wall* current limit is when there is an abrupt current stop after the current limit is reached. The foldback mechanism for this device goes into a *brick-wall* current limit when V_{OUT} > 500 mV (typical), thus limiting current to I_{CL} (typical). When V_{OUT} is approximately 0 V, current is limited to I_{SC} (typical) in order to provide normal start up into a variety of loads.

Thermal shutdown can activate during a current-limit event because of the high power dissipation typically found in these conditions. To provide proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

7.3.7 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the thermal junction temperature (T_J) of the main pass-FET rises to the thermal shutdown temperature (T_{SD}) for shutdown listed in the *Electrical Characteristics*. Thermal shutdown hysteresis makes sure that the LDO resets again (turns on) when the temperature falls to the T_{SD} for reset.

The thermal time constant of the semiconductor die is fairly short, and thus the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced.

For reliable operation, limit the junction temperature to a maximum of 125°C. Operation above 125°C causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

A fast start up when T_J > the T_{SD} for reset causes the device thermal shutdown to assert at T_{SD} for reset, and prevents the device from turning on until the junction temperature is reduced below T_{SD} for reset.

7.4 Device Functional Modes

The device has the following modes of operation:

- Normal operation: The device regulates to the nominal output voltage.
- Dropout operation: The pass element operates as a resistor and the output voltage is set as $V_{IN} – V_{DO}$.
- Disabled: The output of the device is disabled and the discharge circuit is activated.

表 1 shows the conditions that lead to the different modes of operation.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{BIAS} > V_{OUT} + 1.05$ V	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{BIAS} < V_{OUT} + 1.05$ V	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J > T_{SD}$ for shutdown

7.4.1 Normal Mode

The device regulates the output to the nominal output voltage when all normal mode conditions in 表 1 are met.

7.4.2 Dropout Mode

The device is not in regulation, and the output voltage tracks the input voltage minus the voltage drop across the pass element of the device. In this mode, PSRR and the noise performance of the device are significantly degraded.

7.4.3 Disable Mode

In this mode, the pass element is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and the best implementation to achieve a reliable design.

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and BIAS pins. Multilayer ceramic capacitors are the industry standard for these types of applications, but must be used with good judgment. Ceramic capacitors that use X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. Avoid Y5V-rated capacitors because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, assume that effective capacitance decreases by as much as 50%. The input, output, and bias capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

A minimum 2.2-µF ceramic capacitor at the input is required for stability, A minimum 2.2-µF ceramic capacitor with a maximum ESR value of less than 250 mΩ at the output is also required for stability. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. A higher-value input capacitor may be necessary if large, fast rise-time load or line transients are anticipated, or if the device is located several inches from the input power source. Dynamic performance of the device is improved with the use of an output capacitor larger than the minimum value specified in the *Recommended Operating Conditions* table.

Although a bias capacitor is not required, connect a 0.1-µF ceramic capacitor from BIAS to GND for best analog design practice. This capacitor counteracts reactive bias sources if the source impedance is not sufficiently low.

Place the input, output, and bias capacitors as close as possible to the device to minimize traces parasitics.

Application Information (接下页)

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current while output voltage regulation is maintained. See 图 9, 图 10, 图 11, and 图 12 for typical load transient response. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions in 图 39 are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state operation.

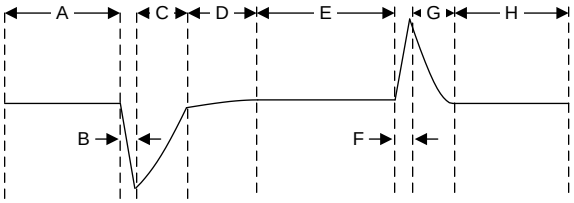


图 39. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient, but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered, and a higher current discharge path is provided for the output capacitor.

8.1.4 Dropout Voltage

Generally, dropout voltage refers to the minimum voltage difference between the input and output voltage (V_{DO} = V_{IN} – V_{OUT}) that is required for regulation. When V_{IN} – V_{OUT} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch.

Dropout voltage is affected by the drive strength of the pass-element gate. This drive strength is nonlinear with respect to V_{IN} on this device.

8.1.5 Behavior During Transition From Dropout Into Regulation

Some applications may have transients that place this device into dropout, especially when this device can be powered from a battery with relatively high ESR. The load transient saturates the output stage of the error amplifier when the pass element is driven fully on, making the pass element function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is limited because the error amplifier must first recover from saturation and then place the pass element back into active mode. During this time, V_{OUT} overshoots because the pass element is functioning as a resistor from V_{IN} to V_{OUT}.

When V_{IN} ramps up slowly for start-up, the slow ramp-up voltage may place the device in dropout. As with many other LDOs, the output can overshoot on recovery from this condition. However, this condition is easily avoided through the use of the enable signal.

If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot. These solutions provide a path to dissipate the excess charge.

Application Information (接下页)

8.1.6 Undervoltage Lockout Circuit Operation

The V_{IN} UVLO circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range. The V_{IN} UVLO circuit also makes sure that the device shuts down when the input supply collapses. Similarly, the V_{BIAS} UVLO circuit makes sure that the device stays disabled before the bias supply reaches the minimum operational voltage range. The V_{BIAS} UVLO circuit also makes sure that the device shuts down when the bias supply collapses.

图 40 depicts the UVLO circuit response to various input or bias voltage events. This figure can be separated into the following parts:

- Region A: The device does not start until the input or bias voltage reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation, but the device is still enabled.
- Region D: Normal operation, regulating device
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases, and the output falls as a result of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached, and a normal start-up follows.
- Region F: Normal operation followed by the input or bias falling to the UVLO falling threshold
- Region G: The device is disabled as the input or bias voltages fall below the UVLO falling threshold to 0 V. The output falls as a result of the load and active discharge circuit.

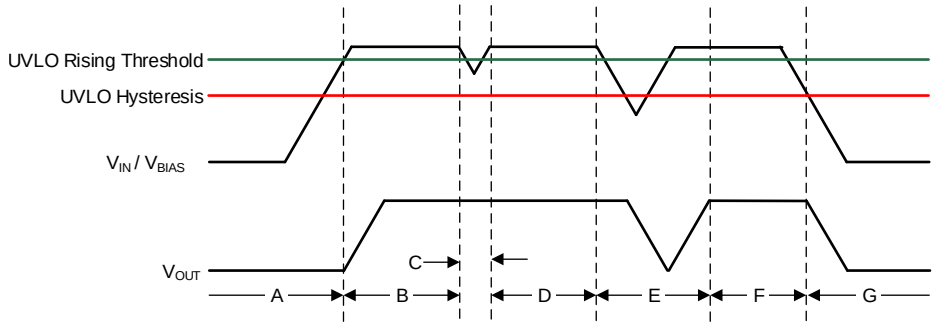


图 40. Typical V_{IN} or V_{BIAS} UVLO Circuit Operation

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

公式 2 calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = [(T_J - T_A) / R_{\theta JA}] \quad (2)$$

公式 3 represents the actual power being dissipated in the device:

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (3)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A10 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Application Information (接下页)

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 公式 4, maximum power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). The equation is rearranged in 公式 5 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (5)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance.

8.1.7.1 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 公式 6 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 公式 3
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

(6)

8.1.7.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is shown in 图 41, and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - 公式 5 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO, thus when $V_{IN} - V_{OUT}$ increases, the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

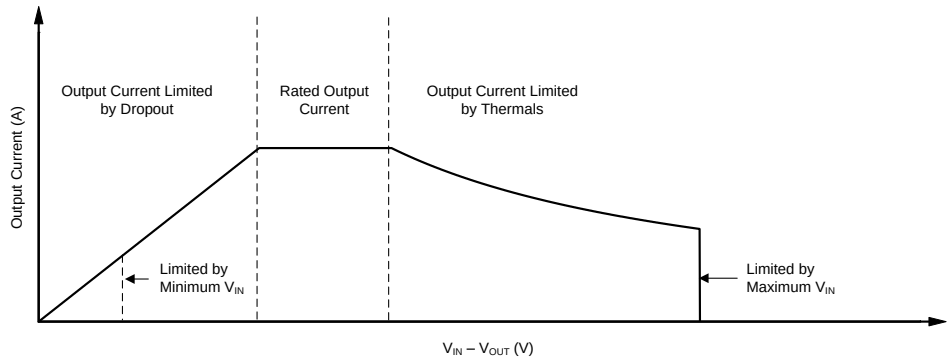


图 41. Region Description of Continuous Operation Regime

8.2 Typical Application

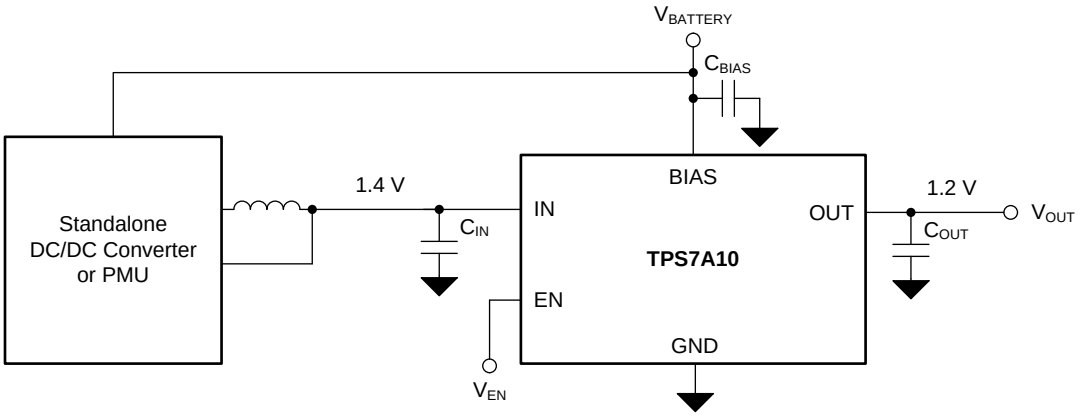


图 42. Supplying a Clean DC Voltage

8.2.1 Design Requirements

表 2 summarizes the design requirements for 图 42.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.4 V
V_{BIAS}	2.7 V
V_{OUT}	1.2 V
I_{OUT}	10-mA typical, 300-mA peak
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

For this design example, the 1.2-V, fixed-version TPS7A1012 device is selected. Use a 4.7-µF input capacitor to minimize transient currents drawn from the DC/DC convertor. Use a 4.7-µF output capacitor for optimized load transient response. The dropout voltage (V_{DO}) is kept within the TPS7A10 dropout voltage specification for the 1.2-V output voltage option inorder to keep the device in regulation under all load and temperature conditions for this design. The high-PSRR and low-noise measurements for this design example are given in the *Thermal Dissipation* section.

8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During startup, the input current is higher as a result of the inrush current charging the output capacitor. Use 公式 7 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (7)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use 公式 8 to calculate the power dissipation. As 公式 9 shows, multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A) to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (8)$$

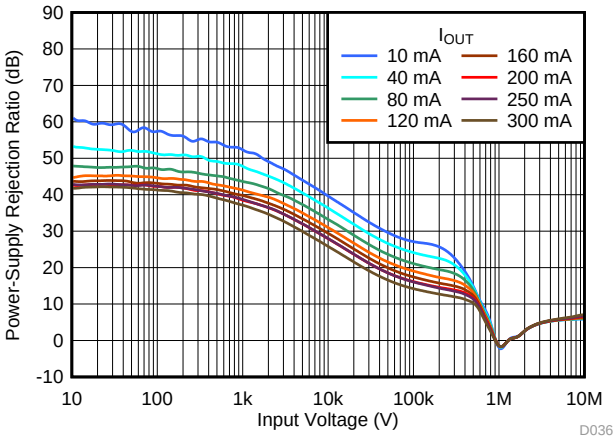
$$T_J = R_{\theta JA} \times P_D + T_A \quad (9)$$

If the ($T_{J(MAX)}$) value does not exceed 125°C, use 公式 10 to calculate the maximum ambient temperature. 公式 11 calculates the maximum ambient temperature with a value of 99.59°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (10)$$

$$T_{A(MAX)} = 125°C - 169.4 \times (1.4\ V - 1.2\ V) \times (0.3\ A) = 114.84°C \quad (11)$$

8.2.3 Application Curve



V_{IN} = 1.4 V, V_{OUT} = 1.2 V, V_{BIAS} = 2.7 V,
C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF, C_{BIAS} = 0.1 µF

图 43. PSRR vs Frequency and I_{OUT}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 0.75 V to 3.3 V, and a bias supply voltage range of 1.7 V to 5.5 V. The input and bias supplies must be well regulated and free of spurious noise. To make sure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V and V_{BIAS} = $V_{OUT(nom)}$ + 1.05 V.

10 Layout

10.1 Layout Guidelines

For correct printed circuit board (PCB) layout, follow these guidelines:

- Place input, output, and bias capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.

10.2 Layout Examples

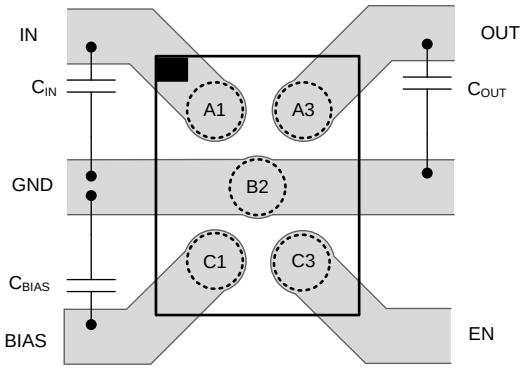


图 44. Recommended Layout for the YKA Package

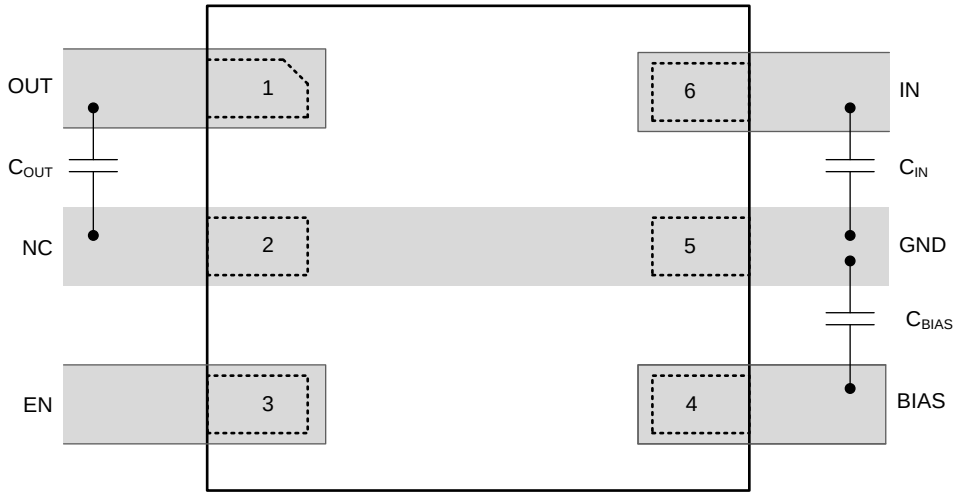


图 45. Recommended Layout for the DSE Package

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们为您提供了评估模块 (EVM)，可以借此来对使用 TPS7A10 时的电路性能进行初始评估。可通过德州仪器 (TI) 网站上的产品文件夹申请获取 *TPS7A10EVM*，也可以直接从 TI eStore 购买。

11.1.1.2 Spice 模型

可以通过 TPS7A10 产品文件夹的*工具与软件*选项卡获取该器件的 Spice 模型。

11.1.2 器件命名规则

表 **3.** 器件命名规则 **(1) (2)**

产品	V_{OUT}
TPS7A10**xx(x)yyyz**	**xx(x)** 为标称输出电压。对于分辨率为 50mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25 V）。 **yyy** 为封装标识符。 **z** 为封装数量。R 表示卷，T 表示带。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com.cn）。
(2) 可提供 0.5V 至 3.0V 的输出电压（以 50mV 为单位增量）。有关器件的详细信息和供货情况，请联系制造商。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TPS7A10EVM-004 评估模块》用户指南*
- 德州仪器 (TI)，*《使用新的热度量指标》应用报告*
- 德州仪器 (TI)，*《AN-1112 DSBGA 晶圆级芯片级封装》应用报告*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1006PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS7A1006PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	EF	Samples
TPS7A1006PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
TPS7A1008PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2	Samples
TPS7A1008PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E2	Samples
TPS7A1008PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A	Samples
TPS7A10105PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ	Samples
TPS7A10105PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DZ	Samples
TPS7A10105PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
TPS7A1010PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1	Samples
TPS7A1010PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	E1	Samples
TPS7A1010PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
TPS7A1011PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX	Samples
TPS7A1011PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DX	Samples
TPS7A1011PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
TPS7A1012PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW	Samples
TPS7A1012PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DW	Samples
TPS7A1012PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
TPS7A1015PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV	Samples
TPS7A1015PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1015PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	F	Samples
TPS7A1018PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU	Samples
TPS7A1018PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DU	Samples
TPS7A1018PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	G	Samples
TPS7A1025PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT	Samples
TPS7A1025PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DT	Samples
TPS7A1025PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H	Samples
TPS7A1028PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS	Samples
TPS7A1028PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DS	Samples
TPS7A1028PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	I	Samples
TPS7A1030PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR	Samples
TPS7A1030PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DR	Samples
TPS7A1030PYKAR	ACTIVE	DSBGA	YKA	5	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

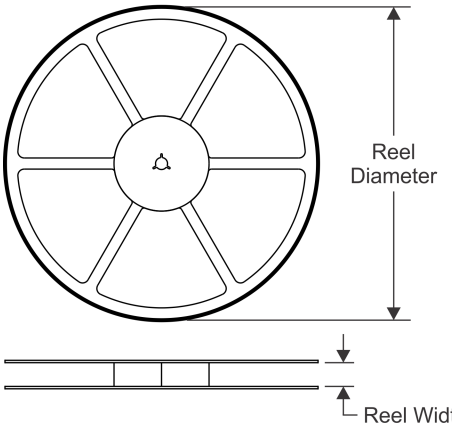
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

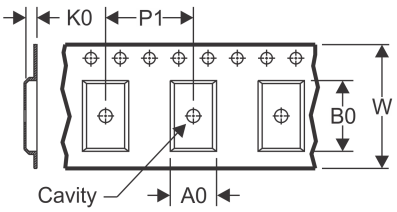
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

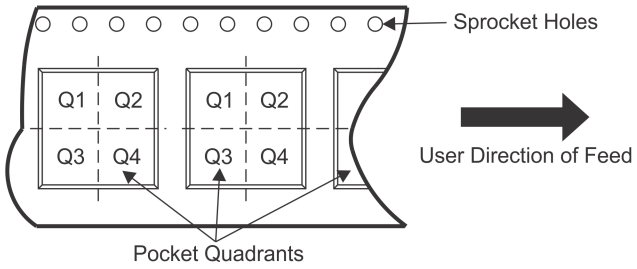


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

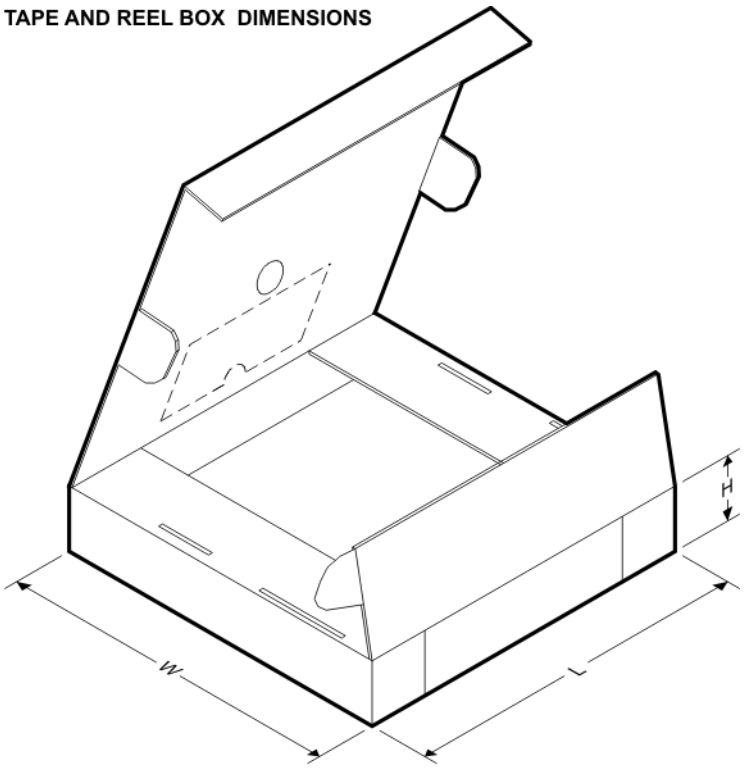


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1006PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1006PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1006PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1008PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1008PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1008PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A10105PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A10105PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A10105PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1010PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1010PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1010PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1011PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1011PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1011PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1012PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1012PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1012PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1015PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1015PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1015PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1018PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1018PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1018PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1025PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1025PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1025PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1028PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1028PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1028PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1
TPS7A1030PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1030PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS7A1030PYKAR	DSBGA	YKA	5	12000	180.0	8.4	0.9	1.25	0.48	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1006PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1006PDSET	WSON	DSE	6	250	183.0	183.0	20.0

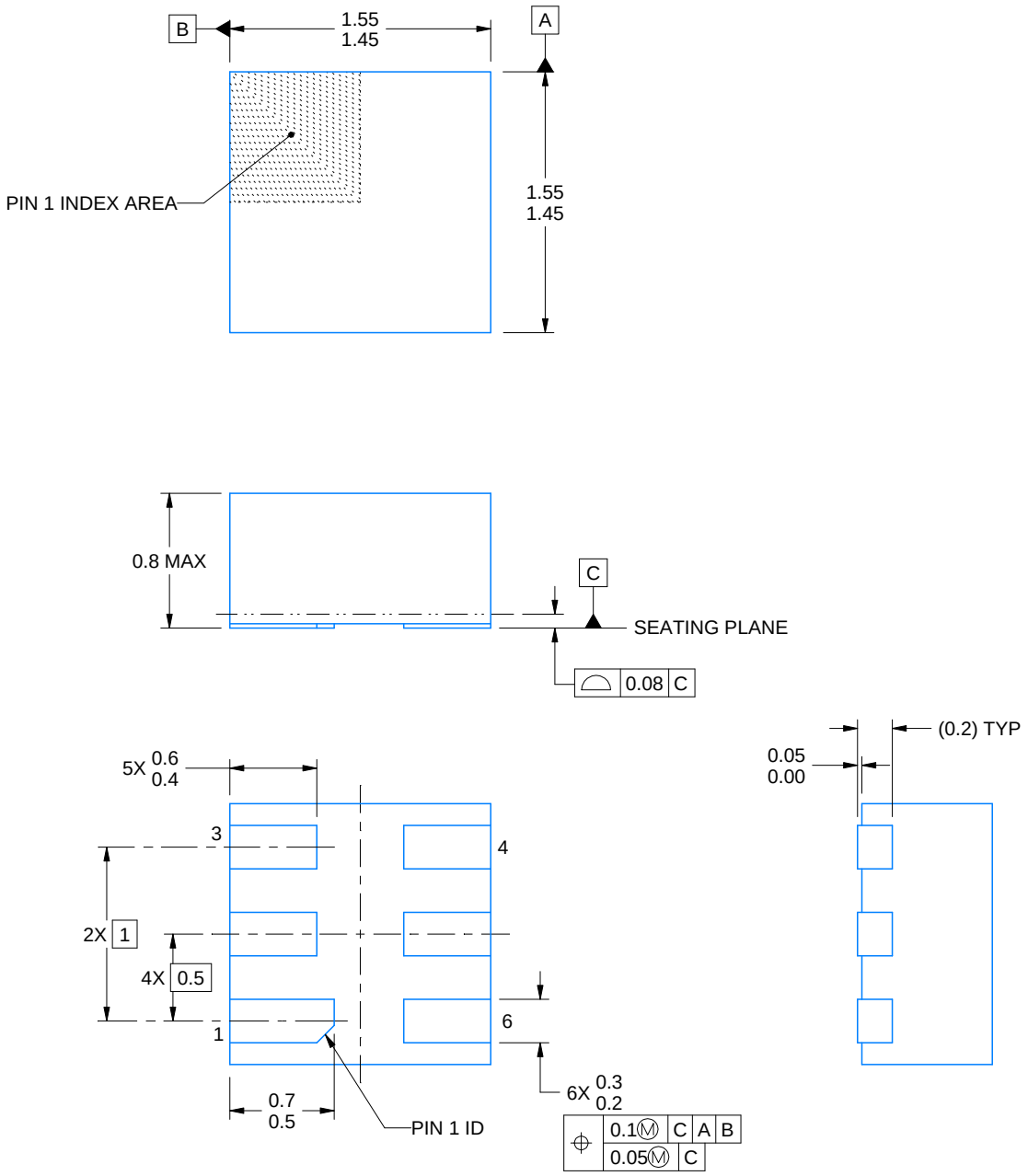
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1006PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1008PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1008PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1008PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A10105PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A10105PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A10105PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1010PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1010PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1010PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1011PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1011PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1011PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1012PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1012PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1012PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1015PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1015PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1015PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1018PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1018PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1018PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1025PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1025PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1025PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1028PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1028PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1028PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0
TPS7A1030PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TPS7A1030PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TPS7A1030PYKAR	DSBGA	YKA	5	12000	182.0	182.0	20.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

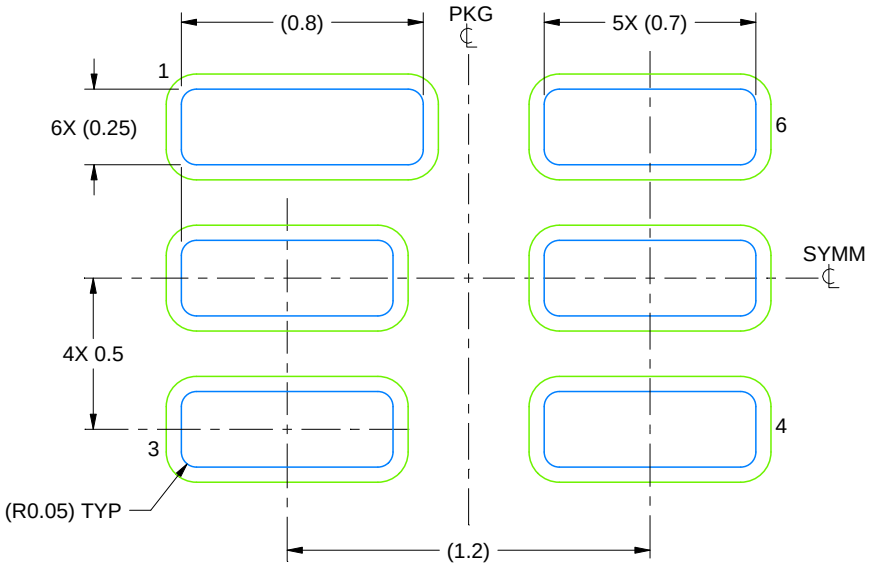
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

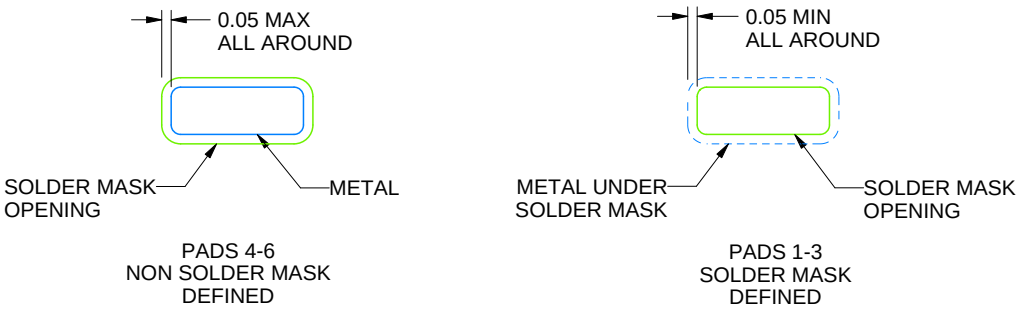
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

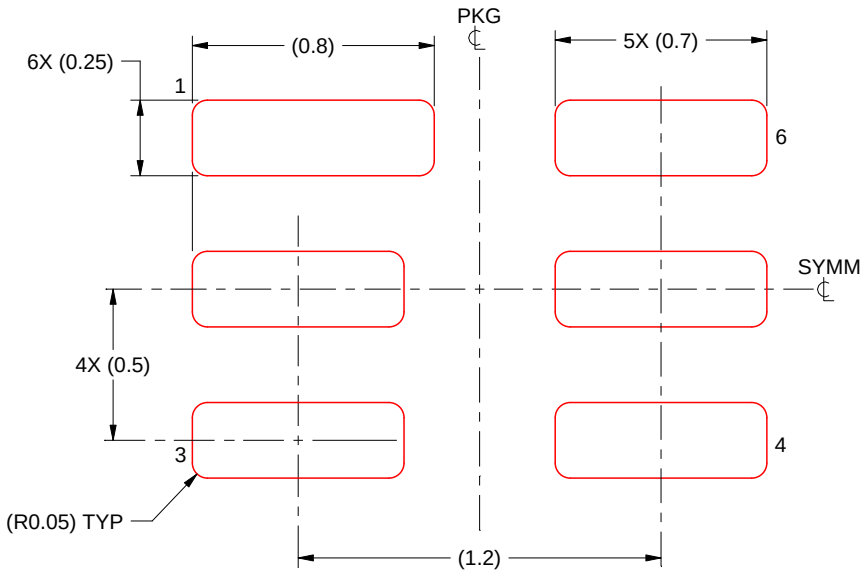
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

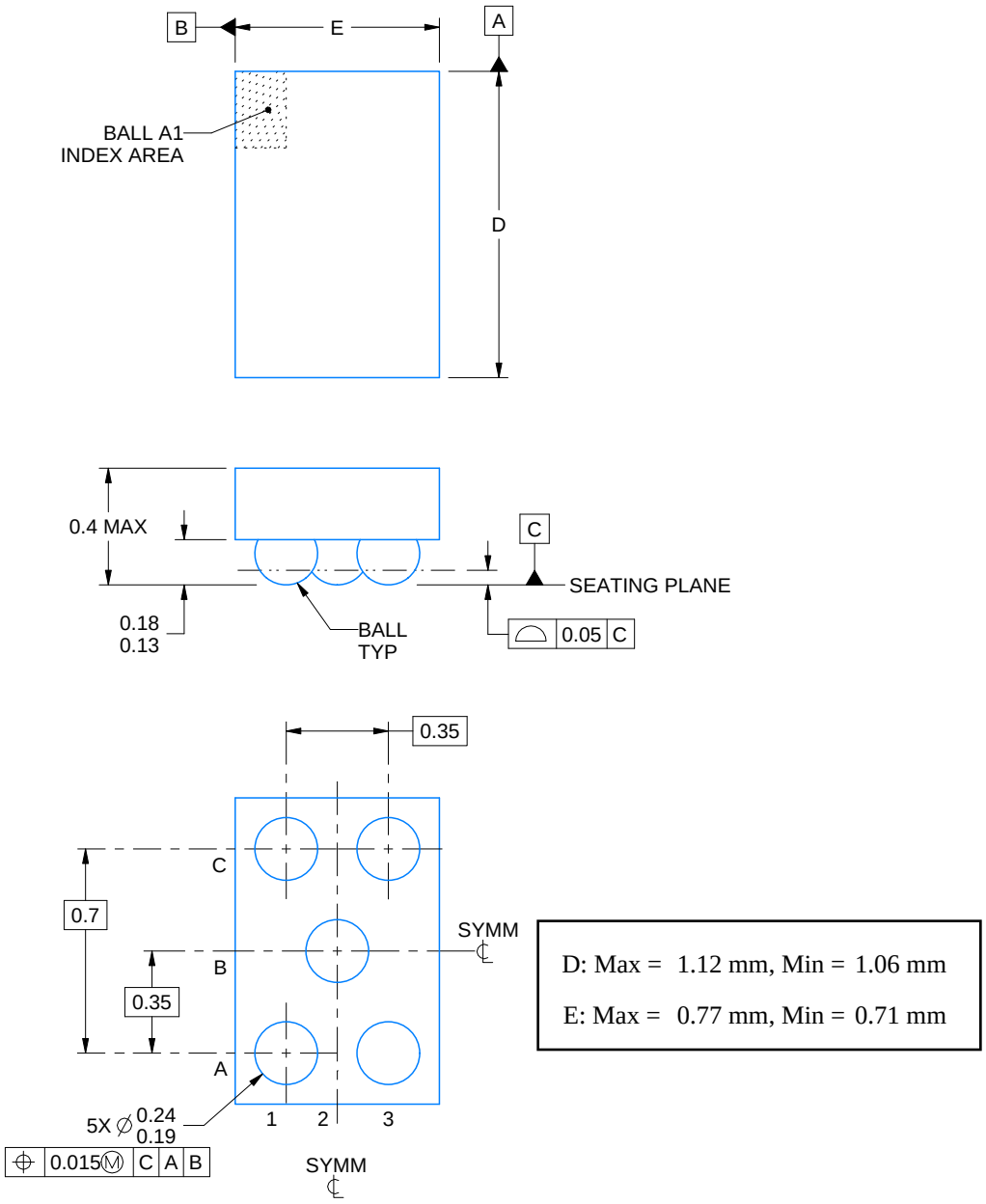
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YKA0005

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

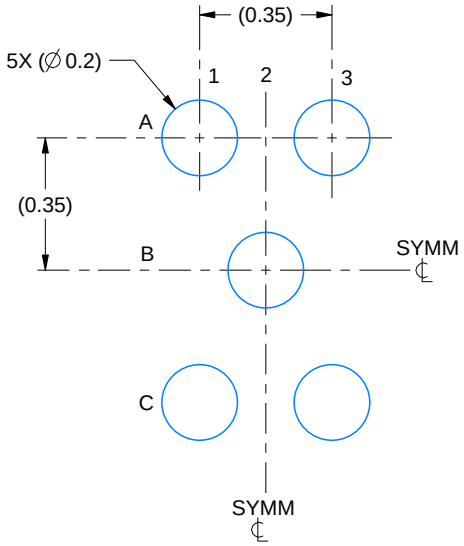


4223737/B 05/2017

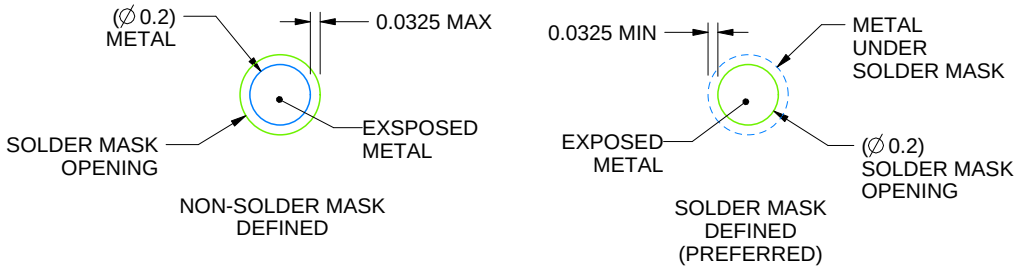
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223737/B 05/2017

NOTES: (continued)

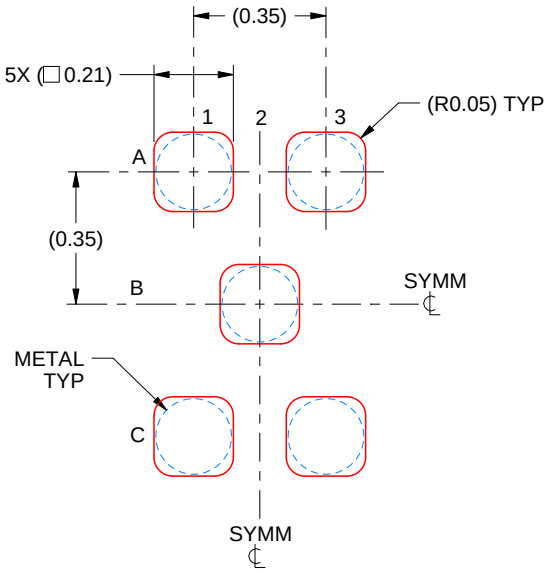
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0005

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

4223737/B 05/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265