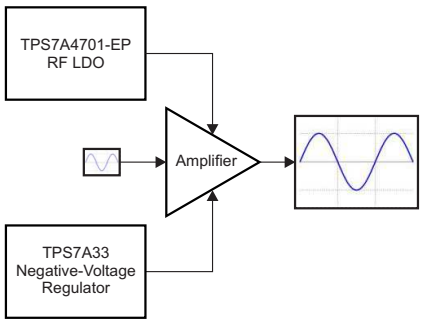
TPS7A4701-EP 36V、1A、4μV_{RMS}、射频 LDO 稳压器

1 特性

- 输入电压范围：3V 至 36V
- 输出电压噪声：
  4μV_{RMS}（10Hz、100kHz）
- 电源纹波抑制：
  - 82dB (100Hz)
  - ≥ 55dB (10Hz，10MHz)
- 两个输出电压模式：
  - ANY-OUT™版本（经由 PCB 布局进行配置的用户可编程输出）：
    - 无需外部反馈电阻器或者前馈电容器
    - 输出电压范围：1.4V 至 20.5V
  - 可调版本：
    - 输出电压范围：1.4V 至 34V
- 输出电流：1A
- 压降电压：1A 时为 307mV
- 与 CMOS 逻辑电平兼容的使能引脚
- 内置固定电流限制和热关断
- 采用高性能散热封装：5mm × 5mm QFN
- 工作温度范围：
  –55°C 至 125°C
- 支持国防、航天和医疗 应用：
  - 受控基线
  - 一个组装/测试场所
  - 一个制造场所
  - 在扩展温度范围（-55°C 至 125°C）内可用
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

简化原理图



2 应用

- 电压控制振荡器 (VCO)
- 频率合成器
- 测试和测量
- 仪器仪表、医疗和音频
- RX，TX，和 PA 电路
- 用于运算放大器，
  数模转换器 (DAC)，模数转换器 (ADC)，和其它高精度模拟电路的电源轨
- 后置 DC/DC 转换器稳压和
  纹波滤除
- 基站和电信基础设施
- 12V 和 24V 工业总线

3 说明

TPS7A4701-EP 是一款正电压 (36V)、超低噪声 (4μV_{RMS}) 低压降线性稳压器 (LDO)，具有 1A 负载电流灌入能力。

TPS7A4701-EP 输出电压可通过用户可编程的 PCB 布局进行配置（高达 20.5V），也可以使用外部反馈电阻器进行调节（高达 34V）。

TPS7A4701-EP 采用双极技术进行设计，主要用于高精度、高精密仪表 应用 ，在这些应用中干净的电压轨对于最大程度地提高系统性能而言至关重要。此特性使得该器件非常适合为运算放大器、模数转换器 (ADC)、数模转换器 (DAC) 以及重要 应用 （如医疗、射频 (RF) 和测试与测量）中的其他高性能模拟电路供电。

此外，TPS7A4701-EP 还非常适合用于后置直流/直流转换器稳压。通过滤除直流/直流开关转换所固有的输出电压纹波，可确保在灵敏仪器、测试与测量、音频和射频 应用中实现系统性能最大化。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A4701-EP	VQFN (20)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

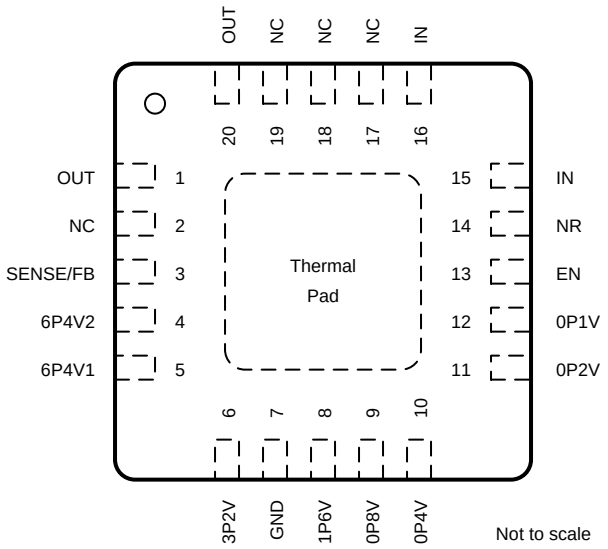
目录

4 修订历史记录

日期	修订版本	说明
2017 年2 月	*	初始发行版

5 Pin Configuration and Functions

RGW Package
20-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
0P1V	12	I	When connected to GND, this pin adds 0.1 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	I	When connected to GND, this pin adds 0.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	I	When connected to GND, this pin adds 0.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	I	When connected to GND, this pin adds 0.8 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	I	When connected to GND, this pin adds 1.6 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	I	When connected to GND, this pin adds 3.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	I	Enable pin. The device is enabled when the voltage on this pin exceeds the maximum enable voltage, $V_{EN(HI)}$. If enable is not required, tie EN to IN.
GND	7	—	Ground.
IN	15, 16	I	Input supply. A capacitor greater than or equal to 1 µF must be tied from this pin to ground to assure stability. A 10-µF capacitor is recommended to be connected from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NR	14	—	Noise reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1-µF capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise.
OUT	1, 20	O	Regulator output. A capacitor greater than or equal to 10 µF must be tied from this pin to ground to assure stability. A 47-µF ceramic output capacitor is highly recommended to be connected from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE/FB	3	I	Control-loop error amplifier input. This is the SENSE pin if the device output voltage is programmed using ANY-OUT (no external feedback resistors). This pin must be connected to OUT. Connect this pin to the point of load to maximize accuracy. This is the FB pin if the device output voltage is set using external resistors. See the *Adjustable Operation* section for more details.
SENSE	3	I	This is the SENSE pin of the device and must be connected to OUT. Connect this pin to the point of load to maximize accuracy.
Thermal Pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range, unless otherwise noted(1)

			MIN	MAX	UNIT
Voltage(2)		IN pin to GND pin	–0.4	36	V
		EN pin to GND pin	–0.4	36	V
		EN pin to IN pin	–36	0.4	V
		OUT pin to GND pin	–0.4	36	V
		NR pin to GND pin	–0.4	36	V
		SENSE/FB pin to GND pin	–0.4	36	V
		0P1V pin to GND pin	–0.4	36	V
		0P2V pin to GND pin	–0.4	36	V
		0P4V pin to GND pin	–0.4	36	V
		0P8V pin to GND pin	–0.4	36	V
		1P6V pin to GND pin	–0.4	36	V
		3P2V pin to GND pin	–0.4	36	V
		6P4V1 pin to GND pin	–0.4	36	V
		6P4V2 pin to GND pin	–0.4	36	V
	Current	Peak output	Internally limited		
T_J	Operating virtual junction		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2500	2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_I	3.0		35	V
V_O	1.4		34	V
V_{EN}	0		V_{IN}	V
I_O	0		1	A

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A4701-EP RGW 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At –55°C ≤ T_J ≤ 125°C; V_I = $V_{O(nom)}$ + 1 V or V_I = 3 V (whichever is greater); V_{EN} = V_I; I_O = 0 mA; C_{IN} = 10 µF; C_{OUT} = 10 µF; C_{NR} = 10 nF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			3		35	V
V_{UVLO}	Under-voltage lockout threshold	V_I rising			2.67		V
		V_I falling			2.5		
$V_{(REF)}$	Reference voltage	$V_{(REF)}$ = $V_{(FB)}$			1.4		V
$V_{UVLO(HYS)}$	Under-voltage lockout hysteresis				177		mV
V_{NR}	Noise reduction pin voltage	Using ANY-OUT option			V_{OUT}		V
		Using adjustable option			1.4		
V_O	Output voltage range	V_I ≥ $V_{O(nom)}$ + 1 V or 3 V (whichever is greater), C_{OUT} = 20 µF	Using ANY-OUT option	1.4		20.5	V
			Using adjustable option	1.4		34	
	Nominal accuracy	T_J = 25°C, C_{OUT} = 20 µF		–1		1	%V_O
	Overall accuracy	$V_{O(nom)}$ + 1 V ≤ V_I ≤ 35 V, 0 mA ≤ I_O ≤ 1 A, C_{OUT} = 20 µF		–3.5		3.5	
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{O(nom)}$ + 1 V ≤ V_I ≤ 35 V			0.092		%V_O
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_O ≤ 1 A			0.3		%V_O
$V_{(DO)}$	Dropout voltage	V_I = 95% $V_{O(nom)}$, I_O = 0.5 A			216		mV
		V_I = 95% $V_{O(nom)}$, I_O = 1 A			307	450	
$I_{(CL)}$	Current limit	V_O = 90% $V_{O(nom)}$		1	1.26		A
$I_{(GND)}$	Ground pin current	I_O = 0 mA			0.58	1	mA
		I_O = 1 A			6.1		
$I_{(EN)}$	Enable pin current	V_{EN} = V_I			0.78	2	µA
		V_I = V_{EN} = 35 V			0.81	2	
$I_{(SHDN)}$	Shutdown supply current	V_{EN} = 0.4 V			2.55	8	µA
		V_{EN} = 0.4 V, V_I = 35 V			3.04	60	
$V_{+EN(HI)}$	Enable high-level voltage			2		V_I	V
$V_{+EN(LO)}$	Enable low-level voltage			0		0.4	V
$I_{(FB)}$	Feedback pin current				350		nA
PSRR	Power-supply rejection ratio	V_I = 16 V, $V_{O(nom)}$ = 15 V, C_{OUT} = 50 µF, I_O = 500 mA, C_{NR} = 1 µF, f = 1 kHz			78		dB
V_n	Output noise voltage	V_I = 3 V, $V_{O(nom)}$ = 1.4 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz			4.17		µV_{RMS}
		V_{IN} = 6 V, $V_{O(nom)}$ = 5 V, C_{OUT} = 50 µF, C_{NR} = 1 µF, BW = 10 Hz to 100 kHz			4.67		
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			170		°C
		Reset, temperature decreasing			150		
T_J	Operating junction temperature			–55		125	°C

6.6 Typical Characteristics

At –55°C ≤ T_J ≤ 125°C; $V_I = V_{O(nom)}$ + 1 V or V_I = 3 V (whichever is greater); $V_{EN} = V_I$; I_O = 0 mA; C_{IN} = 10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

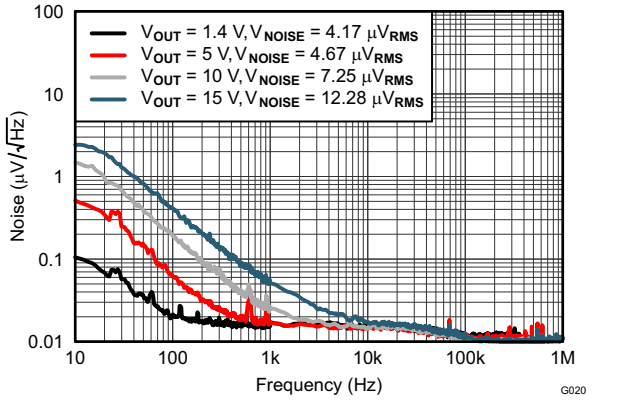


Figure 1. Noise vs Output Voltage

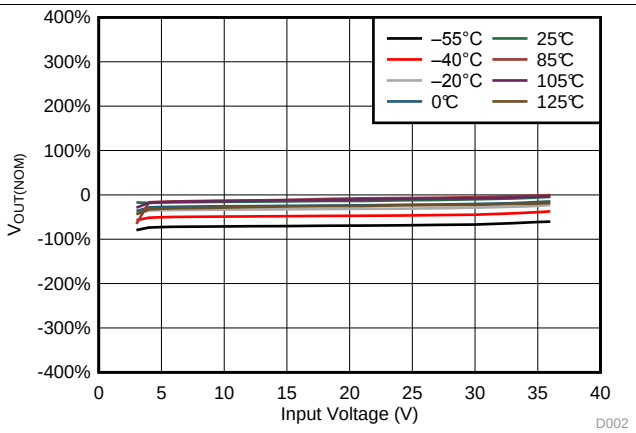


Figure 2. Line Regulation

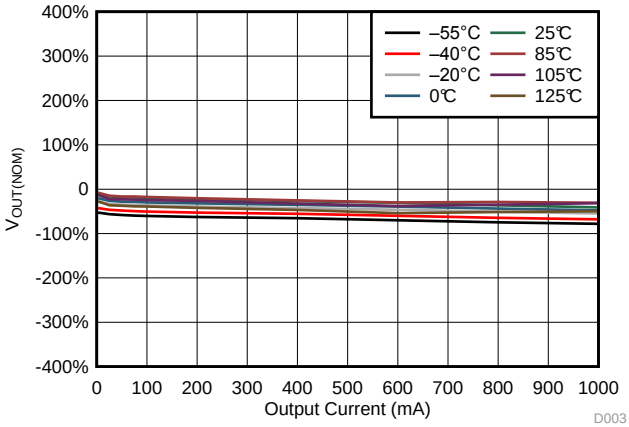


Figure 3. Load Regulation

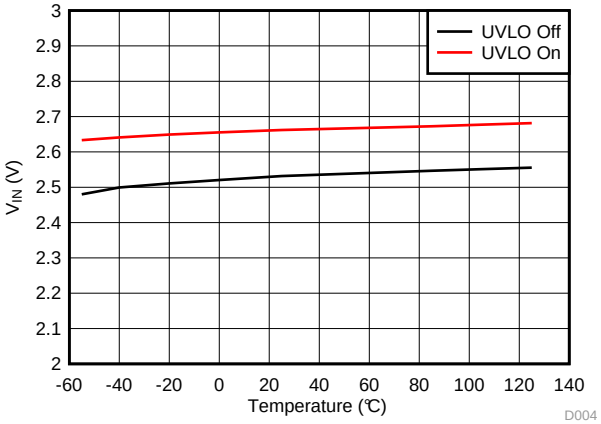


Figure 4. UVLO Threshold vs Temperature

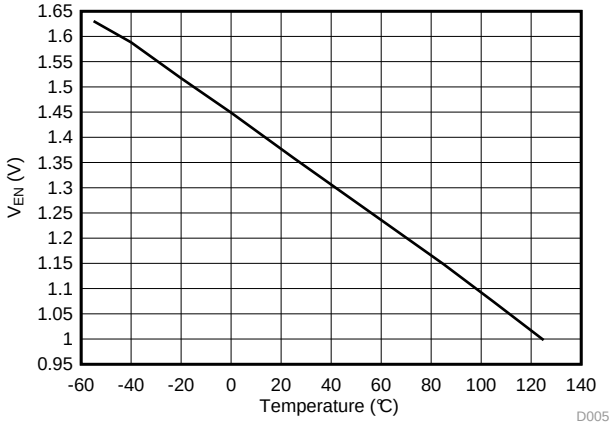


Figure 5. Enable Voltage Threshold vs Temperature

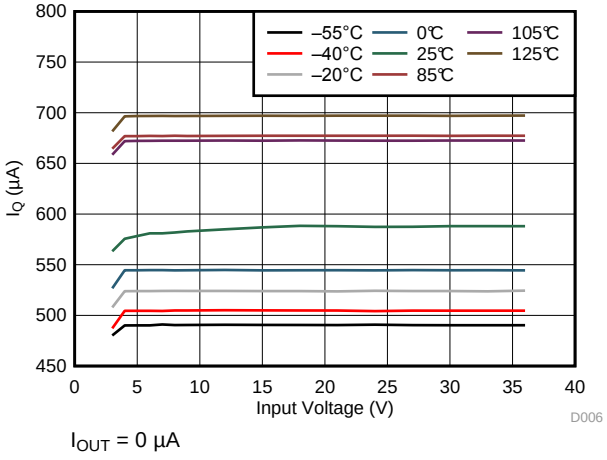


Figure 6. Quiescent Current vs Input Voltage

Typical Characteristics (continued)

At –55°C ≤ T_J ≤ 125°C; $V_I = V_{O(nom)}$ + 1 V or V_I = 3 V (whichever is greater); $V_{EN} = V_I$; I_O = 0 mA; C_{IN} = 10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.

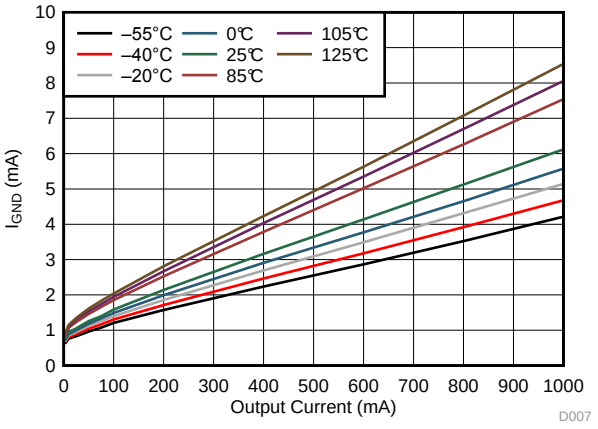


Figure 7. Ground Current vs Output Current

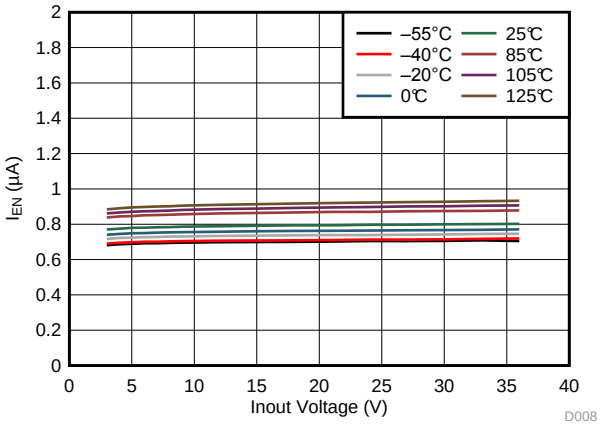


Figure 8. Enable Current vs Input Voltage

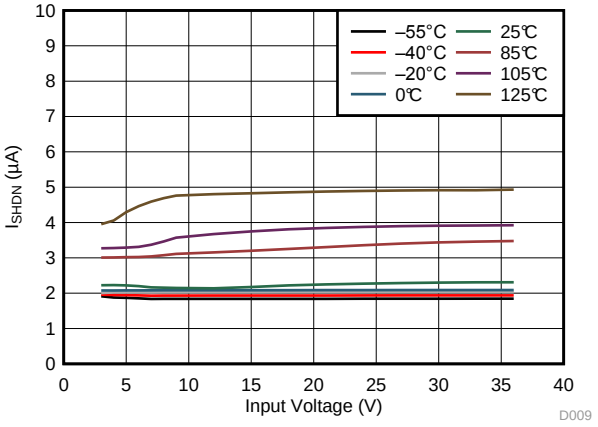


Figure 9. Shutdown Current vs Input Voltage

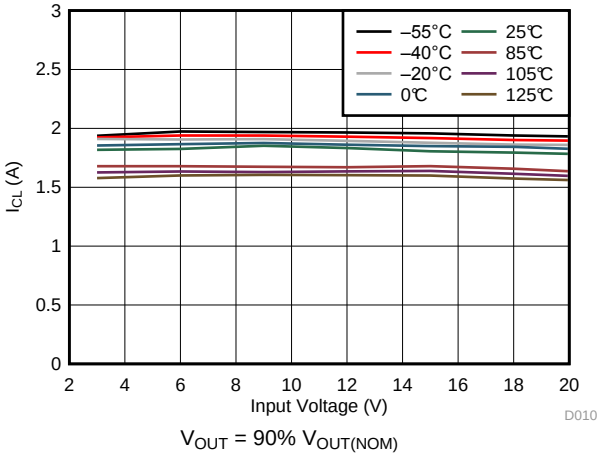


Figure 10. Current Limit vs Input Voltage

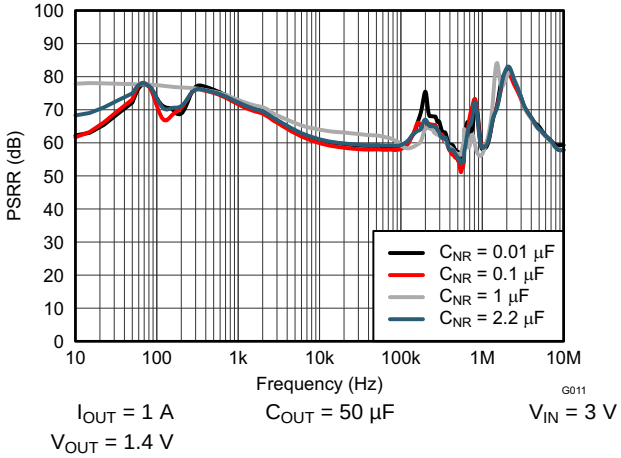


Figure 11. Power-Supply Rejection Ratio vs C_{NR}

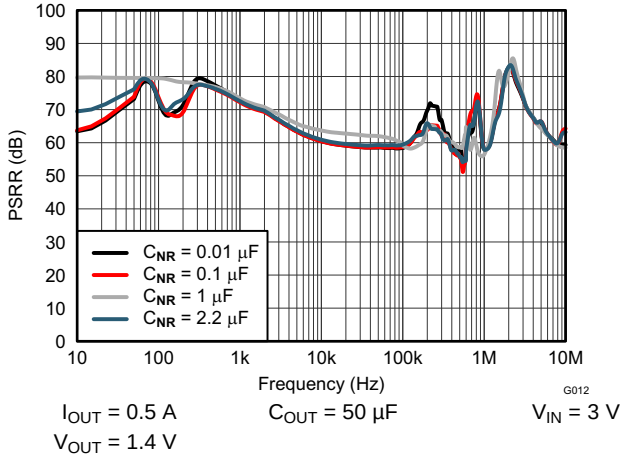
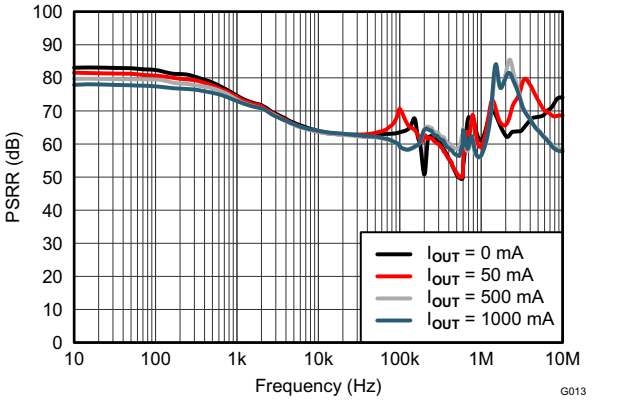


Figure 12. Power-Supply Rejection Ratio vs C_{NR}

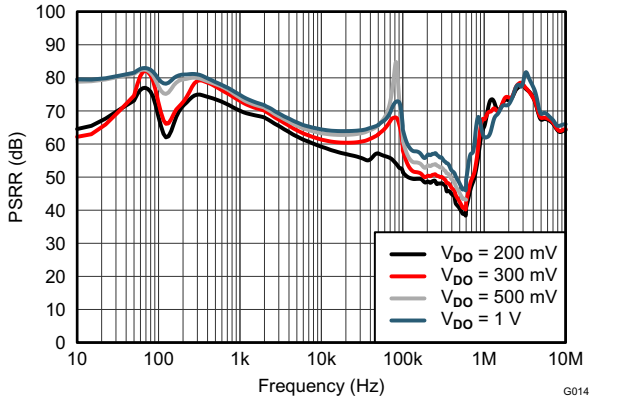
Typical Characteristics (continued)

At –55°C ≤ T_J ≤ 125°C; $V_I = V_{O(nom)}$ + 1 V or V_I = 3 V (whichever is greater); $V_{EN} = V_I$; I_O = 0 mA; C_{IN} = 10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.



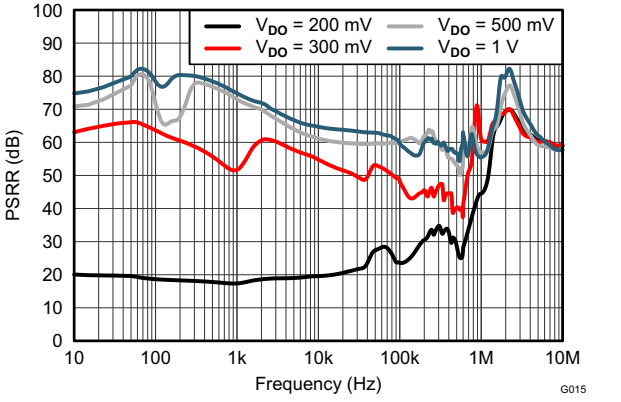
C_{NR} = 1 µF C_{OUT} = 50 µF V_{IN} = 3 V
V_{OUT} = 1.4 V

Figure 13. Power-Supply Rejection Ratio vs I_O



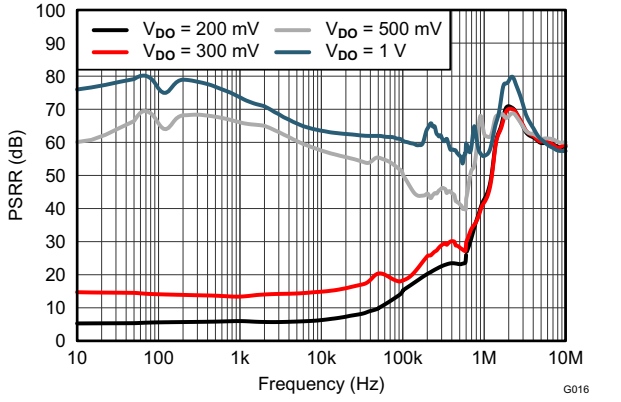
V_{OUT} = 3.3 V C_{NR} = 1 µF C_{OUT} = 50 µF
I_{OUT} = 50 mA

Figure 14. Power-Supply Rejection Ratio vs Dropout



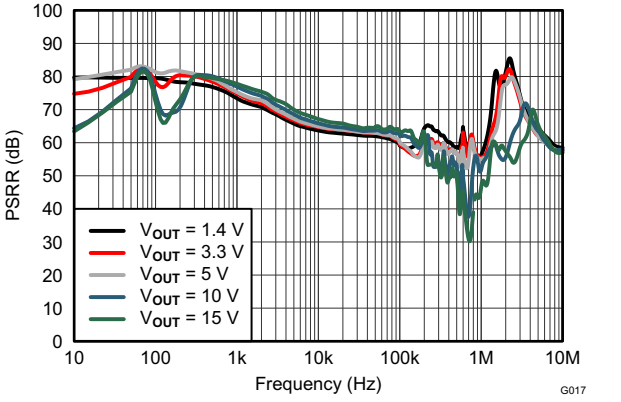
V_{OUT} = 3.3 V C_{NR} = 1 µF C_{OUT} = 50 µF
I_{OUT} = 500 mA

Figure 15. Power-Supply Rejection Ratio vs Dropout



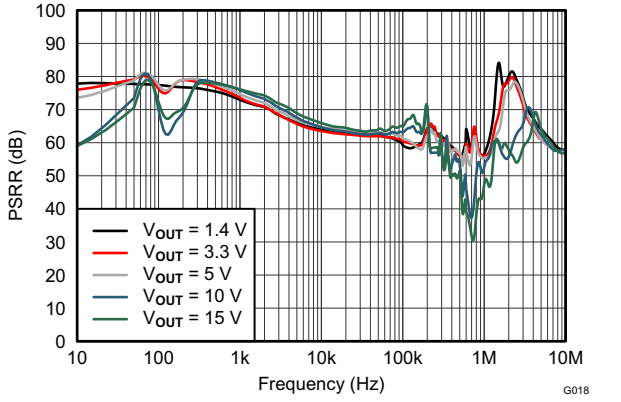
V_{OUT} = 3.3 V C_{NR} = 1 µF C_{OUT} = 50 µF
I_{OUT} = 1 A

Figure 16. Power-Supply Rejection Ratio vs Dropout



C_{NR} = 1 µF C_{OUT} = 50 µF I_{OUT} = 500 mA

Figure 17. Power-Supply Rejection Ratio vs Output Voltage

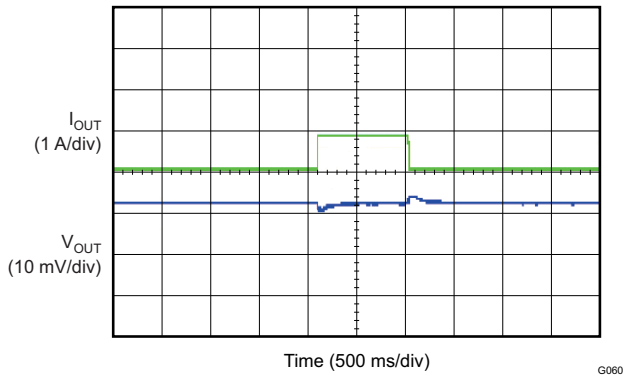


C_{NR} = 1 µF C_{OUT} = 50 µF I_{OUT} = 1000 mA

Figure 18. Power-Supply Rejection Ratio vs Output Voltage

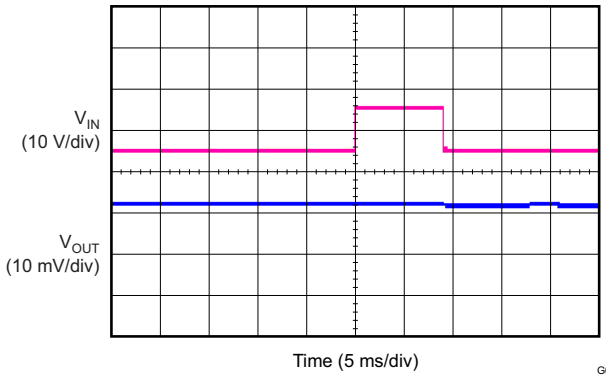
Typical Characteristics (continued)

At –55°C ≤ T_J ≤ 125°C; V_I = $V_{O(nom)}$ + 1 V or V_I = 3 V (whichever is greater); V_{EN} = V_I; I_O = 0 mA; C_{IN} = 10 µF; C_{OUT} = 10 µF; C_{NR} = 1 µF; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins OPEN, unless otherwise noted.



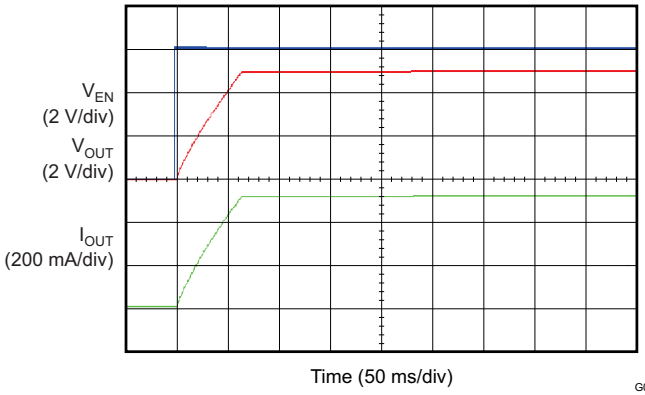
V_{IN} = 5 V V_{OUT} = 3.3 V I_{OUT} = 10 mA to 845 mA

Figure 19. Load Transient



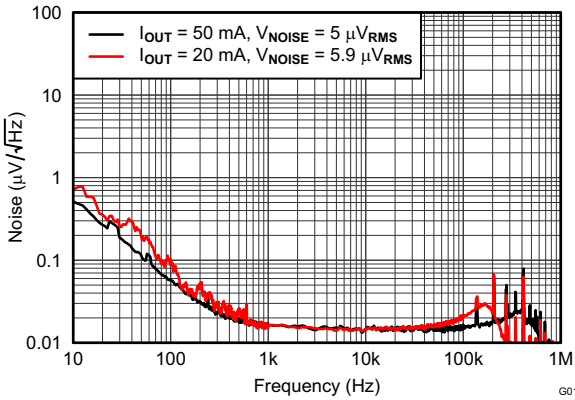
V_{IN} = 5 V to 15 V V_{OUT} = 3.3 V I_{OUT} = 845 mA

Figure 20. Line Transient



Startup Time = 65 ms V_{IN} = 6 V V_{OUT} = 5 V
I_{OUT} = 500 mA C_{IN} = 10 µF C_{OUT} = 50 µF

Figure 21. Startup



V_{OUT} = 4.7 V C_{OUT} = 10 µF C_{NR} = 1 µF
$BW_{RMSNOISE}$ (10 Hz, 100 kHz)

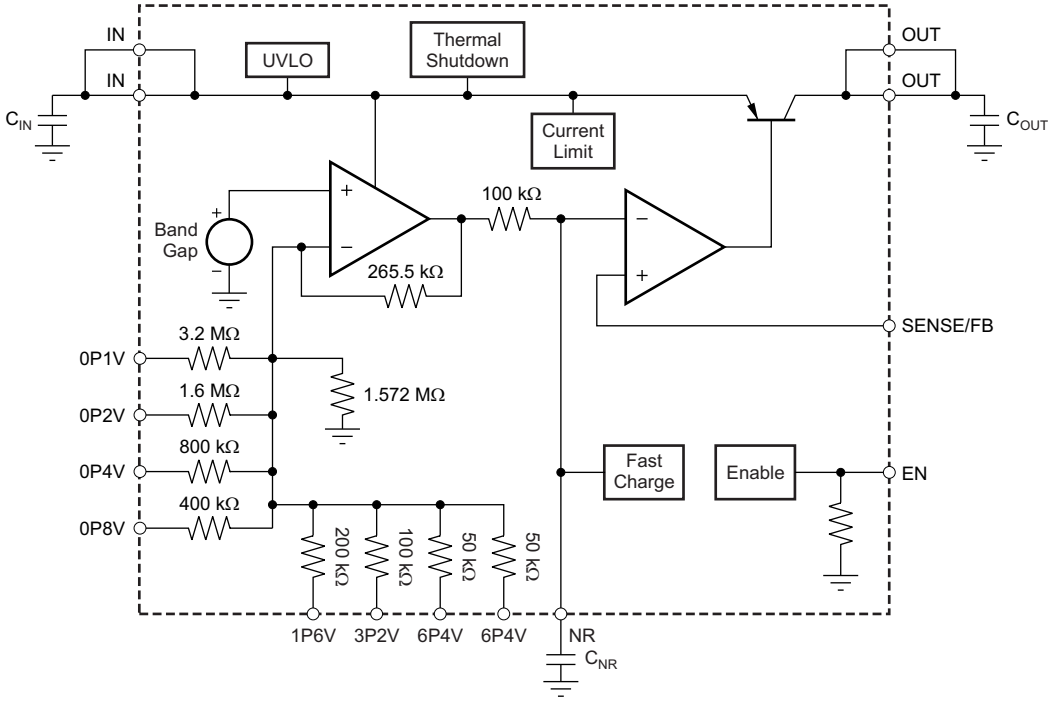
Figure 22. Noise vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A4701-EP is a positive voltage (36 V), ultra-low-noise (4 μV_{RMS}) LDOs capable of sourcing a 1-A load. The TPS7A4701-EP is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit (I_{CL})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate at a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls while load impedance decreases. Note also that when a current limit occurs while the resulting output voltage is low, excessive power is dissipated across the LDO, which results in a thermal shutdown of the output.

7.3.2 Enable (EN) And Under-Voltage Lockout (UVLO)

The TPS7A4701-EP only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input voltage (V_I) to prevent device turnon before V_I rises above the lockout voltage. The UVLO circuit also causes a shutdown when V_I falls below lockout. The EN signal allows independent logic-level turnon and shutdown of the LDO when the input voltage is present. EN can be connected directly to V_I if independent turnon is not needed.

Feature Description (continued)

7.3.3 Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turnon after EN and UVLO have achieved threshold voltage. The noise reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turnon.

Inrush current is defined as the current through the LDO from IN to OUT during the time of the turnon ramp up. Inrush current then consists primarily of the sum of load and charge current to the output capacitor. Inrush current can be estimated by Equation 1:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (1)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turnon ramp,
- $dV_{OUT}(t)/dt$ is the slope of the V_O ramp, and
- R_{LOAD} is the resistive load impedance

7.4 Device Functional Modes

The TPS7A4701-EP has the following functional modes:

1. **Enabled:** When EN goes above $V_{+EN(HI)}$, the device is enabled.
2. **Disabled:** When EN goes below $V_{+EN(LO)}$, the device is disabled. During this time, OUT is high impedance, and the current into IN does not exceed $I_{(SHDN)}$.

7.5 Programming

7.5.1 ANY-OUT Programmable Output Voltage

TPS7A4701-EP can be used in ANY-OUT mode. For ANY-OUT operation, the device does not use external resistors to set the output voltage, but uses device pins 4, 5, 6, 8, 9, 10, 11, and 12 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set by Equation 2 as the sum of the internal reference voltage ($V_{(REF)}$ = 1.4 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 100 mV (pin 12), 200 mV (pin 11), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to $V_{(REF)}$.

$$V_{OUT} = V_{REF} + (\Sigma \text{ ANY-OUT Pins to Ground}) \quad (2)$$

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 4 (6P4V2)	6.4 V
Pin 5 (6P4V1)	6.4 V
Pin 6 (3P2)	3.2 V
Pin 8 (1P6)	1.6 V
Pin 9 (0P8)	800 mV
Pin 10 (0P4)	400 mV
Pin 11 (0P2)	200 mV
Pin 12 (0P1)	100 mV

Table 2 shows a list of the most common output voltages and the corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 1.4 V to 20.5 V in 100-mV steps.

Table 2. Common Output Voltages and Corresponding Pin Settings

V_O (V)	PIN NAMES AND VOLTAGE PER PIN							
	0P1V 100 mV	0P2V 200 mV	0P4V 400 mV	0P8V 800 mV	1P6V 1.6 V	3P2V 3.2 V	6P4V1 6.4 V	6P4V2 6.4 V
1.4	Open	Open	Open	Open	Open	Open	Open	Open
1.5	GND	Open	Open	Open	Open	Open	Open	Open
1.8	Open	Open	GND	Open	Open	Open	Open	Open
2.5	GND	GND	Open	GND	Open	Open	Open	Open
3	Open	Open	Open	Open	GND	Open	Open	Open
3.3	GND	GND	Open	Open	GND	Open	Open	Open
4.5	GND	GND	GND	GND	GND	Open	Open	Open
5	Open	Open	GND	Open	Open	GND	Open	Open
10	Open	GND	GND	Open	GND	Open	GND	Open
12	Open	GND	Open	GND	Open	GND	GND	Open
15	Open	Open	Open	GND	Open	Open	GND	GND
18	Open	GND	GND	Open	Open	GND	GND	GND
20.5	GND	GND	GND	GND	GND	GND	GND	GND

7.5.2 Adjustable Operation

The TPS7A4701-EP has an output voltage range of 1.4 V to 34 V. For adjustable operation, set the nominal output voltage of the device using two external resistors, as shown in Figure 23.

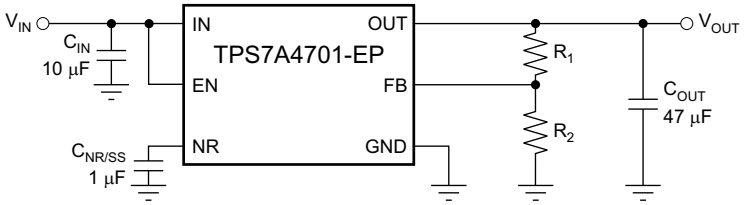


Figure 23. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage within the operational range. The current through feedback resistor R_2 must be at least 5 µA to ensure stability. Additionally, the current into the FB pin ($I_{(FB)}$, typically 350 nA) creates an additional output voltage offset that depends on the resistance of R_1. For high-accuracy applications, select R_2 such that the current through R_2 is at least 35 µA to minimize any effects of $I_{(FB)}$ variation on the output voltage; 10 kΩ is recommended. R_1 can be calculated using Equation 3.

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_{FB} + \frac{V_{REF}}{R_2}} \quad (3)$$

where

- V_{REF} = 1.4 V
- I_{FB} = 350 nA

Use 0.1% tolerance resistors to minimize the effects of resistor inaccuracy on the output voltage.

Table 3 shows the resistor combinations to achieve some standard rail voltages with commercially-available 1% tolerance resistors. The resulting output voltages yield a nominal error of < 0.5%.

Table 3. Suggested Resistors for Common Voltage Rails

V_{OUT}	R_1, Calculated	R_1, Closest 1% Value	R_2
1.4 V	0 Ω	0 Ω	∞
1.8 V	2.782 kΩ	2.8 kΩ	9.76 kΩ
3.3 V	13.213 kΩ	13.3 kΩ	9.76 kΩ
5 V	25.650 kΩ	25.5 kΩ	10 kΩ
12 V	77.032 kΩ	76.8 kΩ	10.2 kΩ
15 V	101.733 kΩ	102 kΩ	10.5 kΩ
18 V	118.276 kΩ	118 kΩ	10 kΩ
24 V	164.238 kΩ	165 kΩ	10.2 kΩ

To achieve higher nominal accuracy, two resistors can be used in the place of R_1. Select the two resistor values such that the sum results in a value as close as possible to the calculated R_1 value.

There are several alternative ways to set the output voltage. The program pins can be pulled low using external general-purpose input/output pins (GPIOs), or can be hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. The TPS7A4701 evaluation module (EVM), available for purchase from the TI eStore, allows the output voltage to be programmed using jumpers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A740x is a high-voltage, low-noise, 1-A LDO. Low-noise performance makes this LDO ideal for providing rail voltages to noise-sensitive loads, such as PLLs, oscillators, and high-speed ADCs.

8.2 Typical Application

Output voltage is set by grounding the appropriate control pins, as shown in Figure 24. When grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{(REF)}$ = 1.4 V). For example, when grounding pins 0P1V, 0P2V, and 1P6V, the voltage values 0.1 V, 0.2 V, and 1.6 V are added to the 1.4-V internal reference voltage for $V_{O(nom)}$ equal to 3.3 V, as described in the *Programming* section.

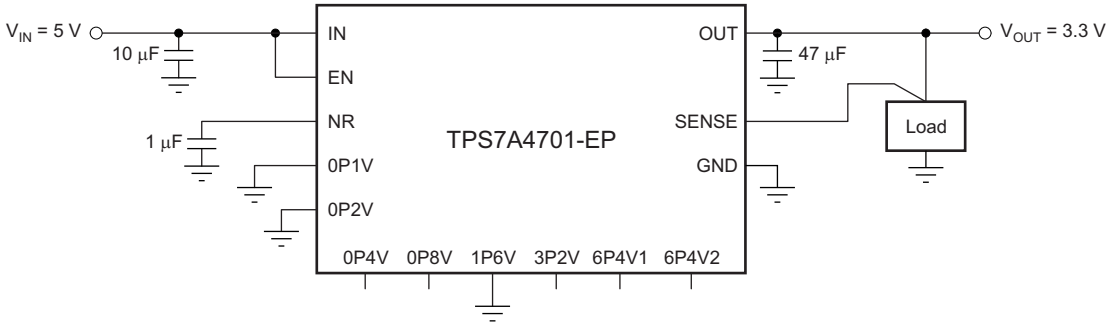


Figure 24. Typical Application, V_{OUT} = 3.3 V

8.2.1 Design Requirements

Table 4. Design Requirements Table

PARAMETER	DESIGN REQUIREMENT
Input Voltage	5 V, ±10%
Output Voltage	3.3 V, ±3%
Output Current	500 mA
Peak-to-Peak Noise, 10 Hz to 100 kHz	50 µVp-p

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Recommendations

These LDOs are designed to be stable using low equivalent series resistance (ESR), ceramic capacitors at the input, output, and at the noise reduction pin (NR, pin 14). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended here, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, but the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and the design engineer must be aware of these characteristics. It is recommended to apply a 50% derating of the nominal capacitance in the design.

Attention must be given to the input capacitance to minimize transient input droop during load current steps because the TPS7A4701-EP has a very fast load transient response. Large input capacitors are necessary for good transient load response, and have no detrimental influence on the stability of the device. Note, however, that using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor, in combination with the wire lead inductance, creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10-µF input capacitor form an LC filter with a resonance frequency of 712 kHz at the edge of the control loop bandwidth. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

8.2.2.1.1 Input and Output Capacitor Requirements

The TPS7A4701-EP is designed and characterized for operation with ceramic capacitors of 10 µF or greater at the input and output. Optimal noise performance is characterized using a total output capacitor value of 50 µF. Note especially that input and output capacitances must be located as near as practical to the respective input and output pins.

8.2.2.1.2 Noise Reduction Capacitor (C_{NR})

The noise reduction capacitor, connected to the NR pin of the LDO, forms an RC filter for filtering out noise that might ordinarily be amplified by the control loop and appear on the output voltage. Larger capacitances, up to 1 µF, affect noise reduction at lower frequencies while also tending to further reduce noise at higher frequencies. Note that C_{NR} also serves a secondary purpose in programming the turnon rise time of the output voltage and thereby controls the turnon surge current.

8.2.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{(DO)} = V_I – V_O$). However, in the *Electrical Characteristics* $V_{(DO)}$ is defined as the $V_I – V_O$ voltage at the rated current ($I_{(RATED)}$), where the main current pass-FET is fully on in the Ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. $V_{(DO)}$ indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this $V_{(DO)}$ limit ($V_I < V_O + V_{(DO)}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, the $V_{(DO)}$ is directly proportional to the output current and can be reduced by the same factor. The $R_{DS(on)}$ for the TPS7A4701-EP can be calculated using Equation 4:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{4}$$

8.2.2.3 Output Voltage Accuracy

The output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error typically includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the *Electrical Characteristics*. Output voltage accuracy also accounts for all variations between manufacturing lots.

8.2.2.4 Startup

The startup time for the TPS7A4701-EP depends on the output voltage and the capacitance of the C_{NR} capacitor. Equation 5 calculates the startup time for a typical device.

$$t_{SS} = 100{,}000 \bullet C_{NR} \bullet \ln\left(\frac{V_R + 5}{5}\right) \tag{5}$$

where

- C_{NR} = capacitance of the C_{NR} capacitor
- $V_R = V_O$ voltage if using the ANY-OUT configuration, or 1.4 V if using the adjustable configuration

8.2.2.5 AC Performance

AC performance of the LDO is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

8.2.2.5.1 Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the DC output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Equation 6 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{S(IN)}(f)$] and output noise voltage [$V_{S(OUT)}(f)$] are understood to be purely ac signals.

$$\text{PSRR (dB)} = 20\ \text{Log}_{10}\left(\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)}\right) \tag{6}$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for optimal PSRR.

The LDO is often employed not only as a DC-DC regulator, but also to provide exceptionally clean power-supply voltages that are free of noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A4701-EP.

8.2.2.5.2 Load Step Transient Response

The load step transient response is the output voltage response by the LDO to a step change in load current whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 1 A (at 1 A per microsecond) and shows a classic, critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers as the control loop adjusts itself. The depth of the charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, the speed of recovery is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case, off-loading step characterization occurs when the current step transitions from 1 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. Because the LDO cannot sink charge current, the control loop must turn off the main pass-FET to wait for the charge to deplete, thus giving the off-load step its typical monotonic decay (which appears triangular in shape).

8.2.2.5.3 Noise

The TPS7A4701-EP is designed, in particular, for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits for instance, where minimum phase noise is all important, or in-test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy. Because the TPS7A4701-EP is also designed for higher voltage industrial applications, the noise characteristic is well designed to minimize any increase as a function of the output voltage.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu V/\sqrt{Hz}$). The RMS noise is then calculated in the usual manner as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

8.2.3 Application Curves

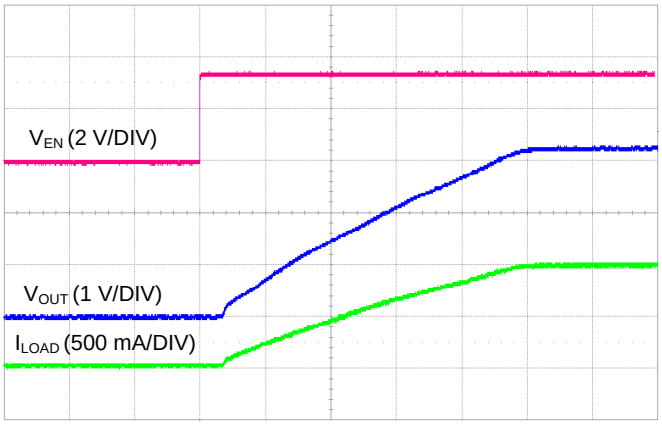


Figure 25. Startup with EN Pin rising (10 ms/DIV)

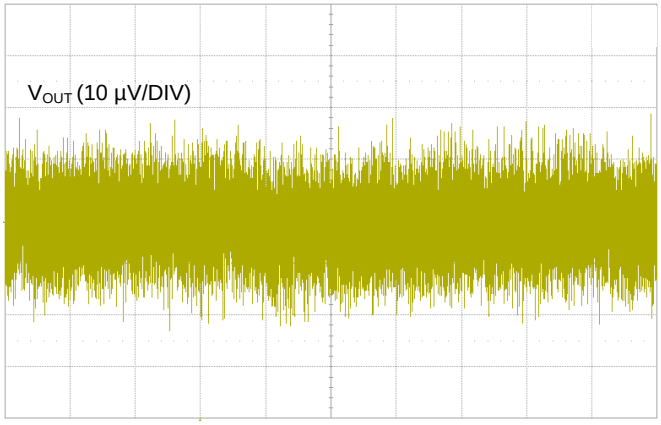


Figure 26. Output Noise Voltage, 10 Hz to 100 kHz (10 ms/DIV)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range of 3 V to 35 V. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9.1 Power Dissipation (P_D)

Power dissipation must be considered in the PCB design. In order to minimize risk of device operation above 125°C, use as much copper area as available for thermal dissipation. Do not locate other power-dissipating devices near the LDO.

Power dissipation in the regulator depends on the input to output voltage difference and load conditions. P_D can be calculated using Equation 7:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (7)$$

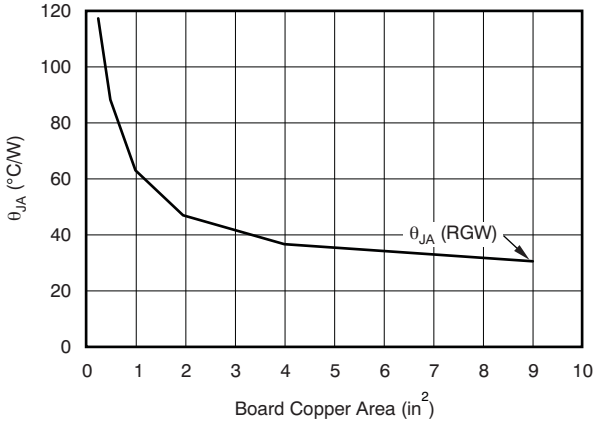
It is important to note that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the QFN (RGW) package is through the thermal pad to the PCB. The thermal pad must be soldered to a copper pad area under the device. Thermal vias are recommended to improve the thermal conduction to other layers of the PCB.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 8.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (8)$$

Unfortunately, this thermal resistance (θ_{JA}) depends primarily on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the spreading planes. The θ_{JA} recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area and is to be used only as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the QFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. By knowing θ_{JCbot}, the minimum amount of appropriate heat sinking can be used to estimate θ_{JA} with Figure 27. θ_{JCbot} can be found in the *Thermal Information* table.



NOTE: θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 27. Θ_{JA} vs Board Size

10 Layout

10.1 Layout Guidelines

For best overall performance, all circuit components are recommended to be located on the same side of the circuit board and as near as practical to the respective LDO pin connections. Ground return connections to the input and output capacitor, and to the LDO ground pin, must also be as close to each other as possible and connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

Use the TPS7A4701 evaluation module (EVM), available for purchase from the TI eStore, as a reference for layout and application design.

10.2 Layout Example

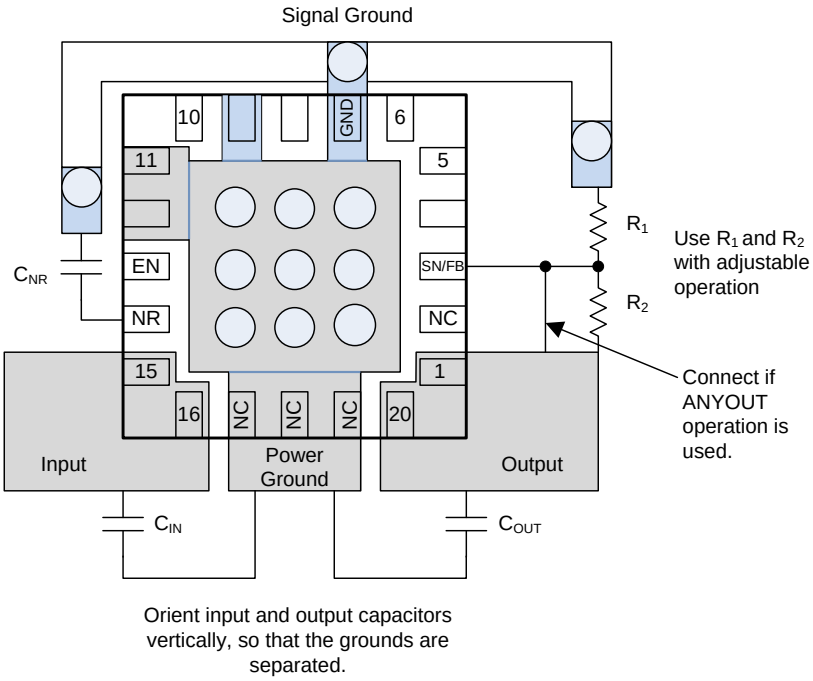


Figure 28. Layout Example

10.3 Thermal Protection

The TPS7A4701-EP contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 170°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 150°C (typical). Because the TPS7A4701-EP is capable of supporting high input voltages, a great deal of power can be expected to be dissipated across the device at low output voltages, which causes a thermal shutdown. The thermal time-constant of the semiconductor die is fairly short, and thus the output oscillates on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, the junction temperature must be limited to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown must be designed to occur at least 45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4701-EP is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A4701-EP into thermal shutdown degrades device reliability.

10.4 Estimating Junction Temperature

JEDEC standards now recommend the use of PSI thermal metrics to estimate the junction temperatures of the LDO while in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These PSI metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 9.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (9)$$

where:

- P_D is the power dissipated as explained in Equation 7,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《TPS7A47XXEVM-094 评估模块》*
- *《使用前馈电容器和低压降稳压器的优缺点》*

11.2 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

ANY-OUT, PowerPAD, E2E are trademarks of Texas Instruments.
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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4701MRGWREP	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7A4701M	Samples
V62/17601-01XE	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7A4701M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

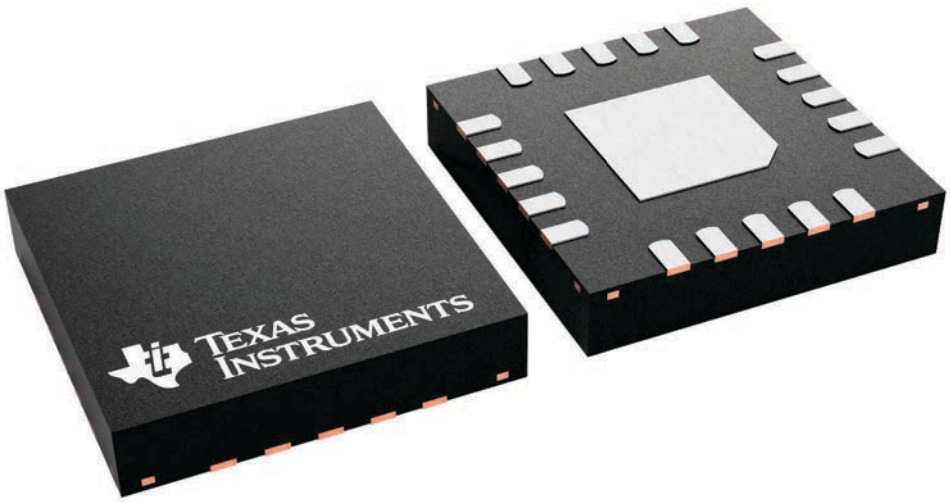
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



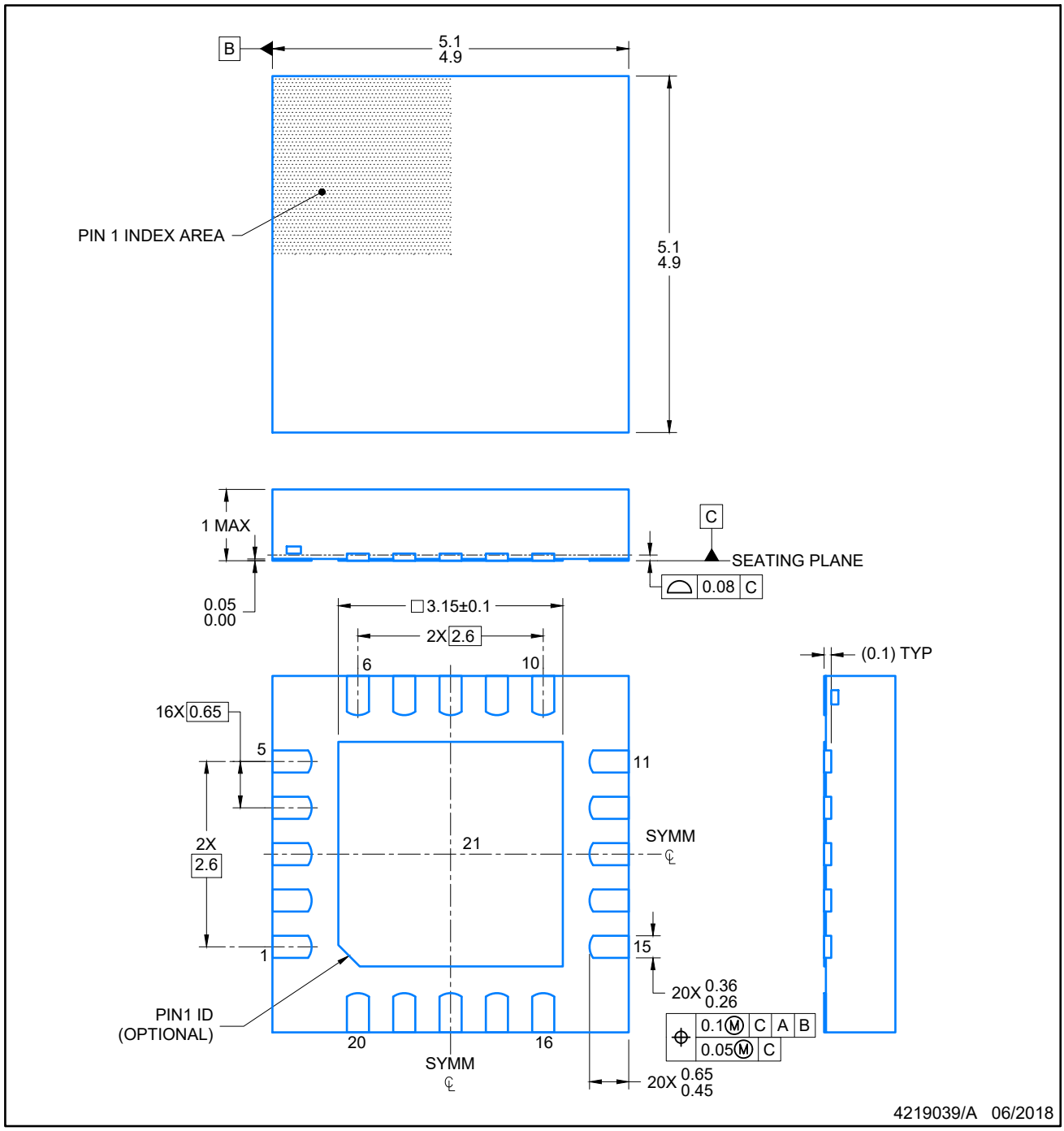
4227157/A

PACKAGE OUTLINE

RGW0020A

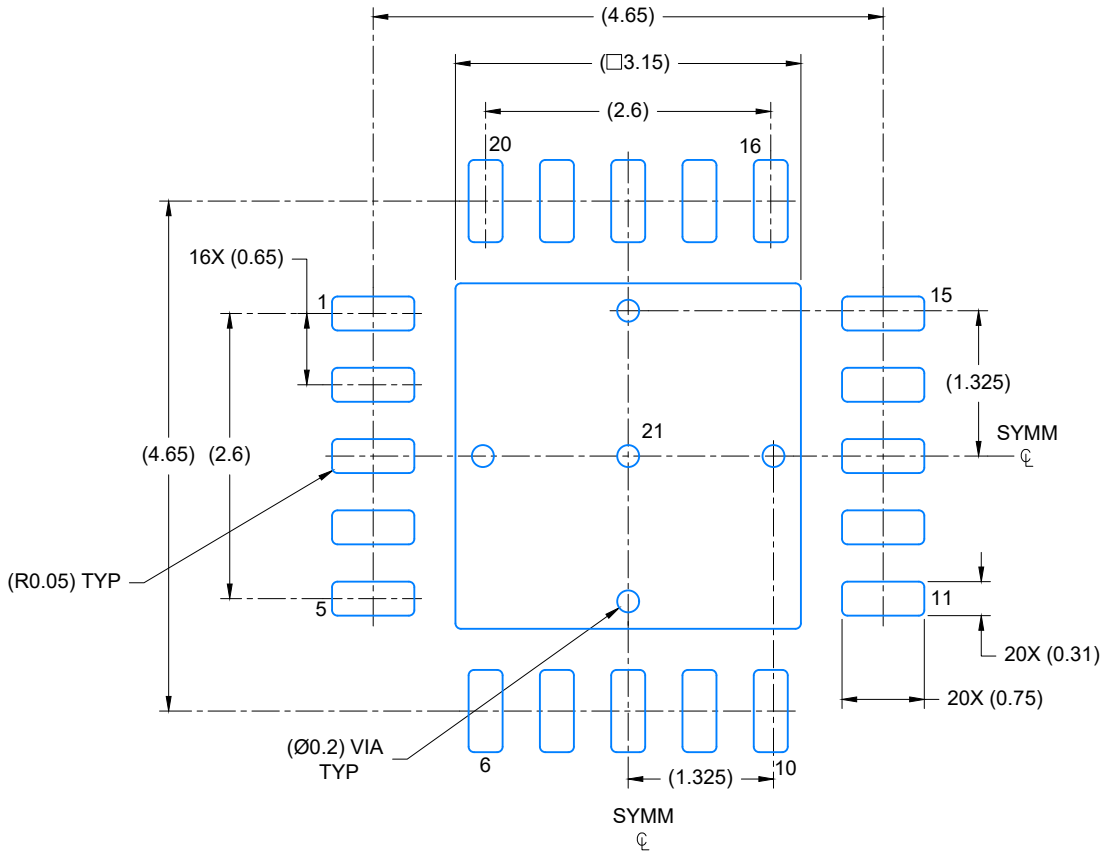
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



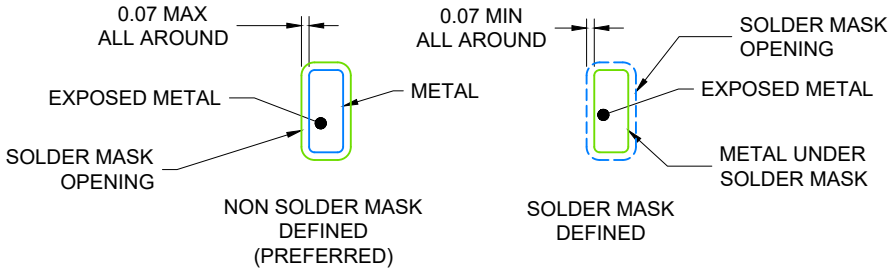
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X



SOLDER MASK DETAILS

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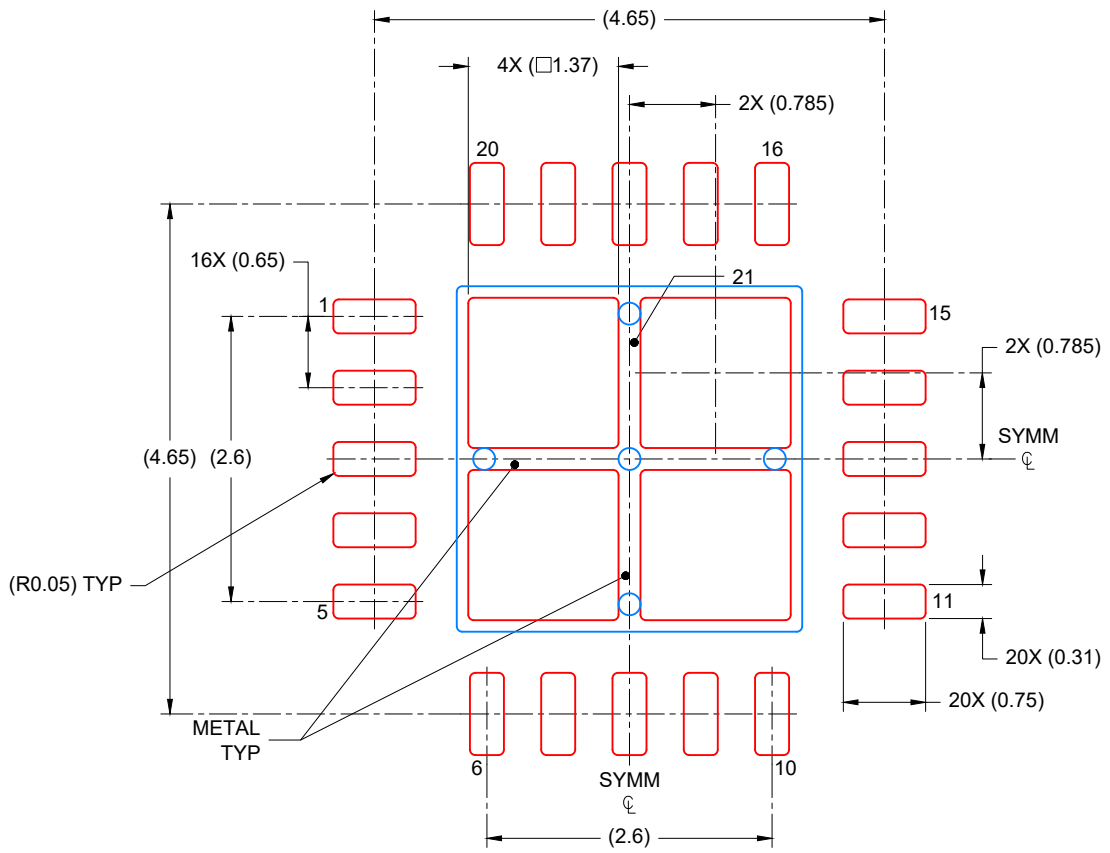
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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