Texas Instruments
TPS7B4255-Q1
ZHCSOZ7A – JUNE 2022 – REVISED AUGUST 2023

TPS7B4255-Q1
具有 5mV 跟踪容差的汽车类 70mA、40V 电压跟踪 LDO

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 结温：–40°C 至 +150°C，T_J
- 宽输入工作电压范围（3V 至 40V）：
  - 最大绝对输入电压范围：-40V 至 +45V
- 宽输出电压范围：2V 至 40V
- 最大输出电流：70mA
- 非常严格的输出跟踪容差：5mV（最大值）
- 低压降：70mA 时为 500mV（最大值）
- 组合基准和使能功能
- 轻负载时低静态电流：35μA
- 宽 C_{OUT} 和 ESR 范围：
  - 与 ESR（1mΩ 至 3Ω）陶瓷输出电容器（1μF 至 200μF）搭配使用时可保持稳定
- 集成保护特性：
  - 反向电流保护
  - 反极性保护
  - 过热保护
  - 接地输出短路和电源输出短路保护
- 采用两种 5 引脚 SOT-23 封装：
  - 标准 SOT-23 (DBV) 封装
  - 热增强型 SOT-23 (DYB) 封装

2 应用

- 动力总成压力传感器
- 动力总成温度传感器
- 动力总成排气传感器
- 动力总成油液浓度传感器
- 车身控制模块 (BCM)

3 说明

TPS7B4255-Q1 是一款低压差 (LDO) 电压跟踪稳压器，具有高跟踪精度以及出色的负载和线路瞬态响应。该器件采用两种 5 引脚 SOT-23 封装（DBV 和 DYB）。TPS7B4255-Q1 旨在为动力总成系统等汽车应用中的非板载传感器供电。由于提供非板载电源的电缆发生故障的风险较高，因此器件配备了集成保护功能，可应对反向电流（电池短路）、反极性、输出接地短路（电流限制）和过热（热关断）等故障情况。该器件可承受 45V（绝对最大值）输入电压，并能经受住汽车负载突降瞬态条件的考验。

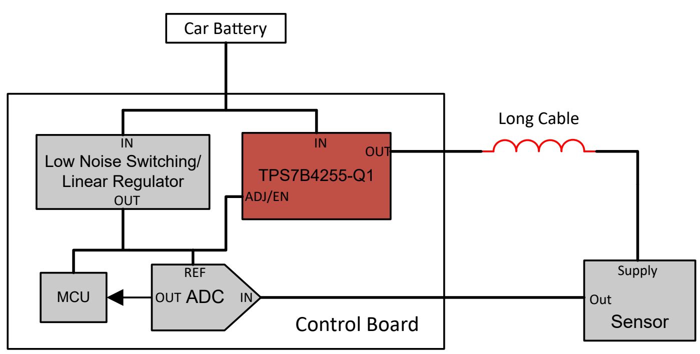
负载高达 70mA、容差非常小的 OUT 引脚可对 ADJ/EN 引脚上施加的基准电压进行有效跟踪。因此，TPS7B4255-Q1 可为高精度非板载传感器提供电源电压，这有助于利用比例式传感器提高测量的可靠性和精度。

通过将 ADJ/EN 输入引脚置于低电平，TPS7B4255-Q1 可切换至待机模式，从而将 LDO 的静态电流降至 3.25μA 以下。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS7B4255-Q1	DBV（SOT-23，5)	2.9mm × 2.8mm
	DYB（SOT-23，5）	2.93mm x 2.7mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用

English Data Sheet: SBVS392

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2022) to Revision A (August 2023)	**Page**
• 将文档状态从 *预告信息* 更改为 *量产数据*	1

5 Pin Configuration and Functions

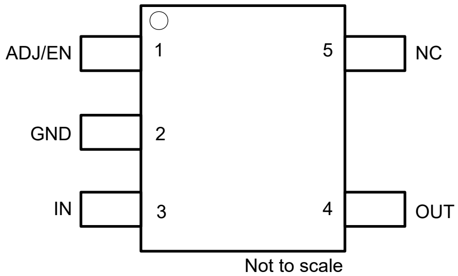


图 5-1. DBV Package, 5-Pin SOT-23 (Top View)

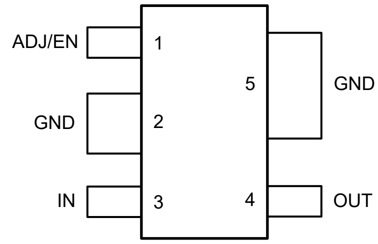


图 5-2. DYB Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBV	DYB		
ADJ/EN	1	1	I	Adjustable or enable input pin. Connect the external reference voltage to this pin. This pin connects to the error amplifier internally. A low signal below V_{IL} disables the device, and a high signal above V_{IH} enables the device. Connect the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, place a 0.1-µF capacitor close to this pin.
GND	2	2, 5	G	Ground pin.
IN	3	3	I	Input power-supply voltage pin. This pin is the device supply. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible to compensate for line influences.
NC	5	—	—	NC pin. This pin is not internally connected. This pin can either be left floating or connected to GND for improved thermal performance.
OUT	4	4	O	Tracker output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table. Place the output capacitor as close to output of the device as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	–40	45	V
V_{OUT}	Tracker output voltage	–5	45	V
$V_{ADJ/EN}$	Adjustable reference and enable input voltage	–0.3	45	V
V_{IN} - V_{OUT}	Input output voltage difference	–40	40	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect the device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Unregulated input voltage	3		40	V
V_{OUT}	Regulated output voltage	2		40	V
V_{ADJ}	Adjust pin voltage	2		40	V
I_{OUT}	Output current	0		70	mA
C_{IN}	Input capacitor[1]	0	1		μF
C_{OUT}	Output capacitor[2]	1		200	μF
ESR	Output capacitor ESR requirements	0.001		3	Ω
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance recommended is 500 nF.
(2) Effective output capacitance of 500 nF minimum required for stability.

6.4 Thermal Information

THERMAL METRIC[1] [2]		TPS7B4255-Q1		UNIT
		DBV (SOT-23)	DYB (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.3	127.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.6	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	16.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.9	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.1	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7, two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated
(2) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 1 µF, 1 mΩ ≤ C_{OUT} ESR ≤ 3 Ω, C_{IN} = 1 µF, and V_{ADJ} = 5 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tracking accuracy	V_{IN} = V_{OUT} + 600 mV to 40 V, I_{OUT} = 100 µA to 70 mA	–5		5	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 600 mV to 40 V			0.5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 600 mV, I_{OUT} = 100 µA to 70 mA [(1)]			0.6	mV
I_Q	Quiescent current	V_{IN} = 5.6 V to 40 V, I_{OUT} = 100 µA, T_J = 25ºC		35	40	µA
		V_{IN} = 5.6 V to 40 V, I_{OUT} = 100 µA, -40ºC < T_J < 85ºC			45	
		V_{IN} = 5.6 V to 40 V, I_{OUT} = 100 µA			50	
I_{GND}	Ground current	V_{IN} = 5.6 V to 40 V, I_{OUT} = 70 mA, T_J = 25ºC			470	
		V_{IN} = 5.6 V to 40 V, I_{OUT} = 70 mA			550	
V_{DO}	Dropout voltage	I_{OUT} = 70 mA, V_{ADJ} ≥ 5 V, V_{IN} = V_{ADJ}			500	mV
		I_{OUT} = 50 mA, V_{ADJ} ≥ 5 V, V_{IN} = V_{ADJ}			365	
$I_{SHUTDOWN}$	Shutdown supply current (I_{GND})	$V_{ADJ/EN}$ = 0 V			3.25	µA
$I_{ADJ/EN}$	ADJ/EN pin current				0.3	
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising	2.6	2.7	2.81	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling	2.3	2.4	2.5	
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis			300		mV
V_{IL}	Adjustable and enable logic input low level				0.85	V
V_{IH}	Adjustable and enable logic input high level		1.75			
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1 V, V_{OUT} short to 90% x V_{ADJ}	75	105	130	mA
PSRR	Power-supply ripple rejection	V_{IN} - V_{OUT} = 1 V, frequency = 100 Hz, I_{OUT} = 70 mA		80		dB
V_n	Output noise voltage	V_{OUT} = 3.3 V, I_{OUT} = 1 mA, BW = 10 Hz to 100 kHz, a 5 µV_{RMS} reference is used for this measurement		150		µV_{RMS}
I_{REV}	Reverse current at V_{IN}	V_{IN} = 0 V, V_{OUT} = 20 V, V_{ADJ} = 5 V	-0.25		0.25	µA
$I_{REV\text{-}N1}$	Reverse current at negative V_{IN}	V_{IN} = –20 V, V_{OUT} = 20 V, V_{ADJ} = 5 V	-0.5		0.5	
$I_{REV\text{-}N2}$	Reverse current at negative V_{IN}	V_{IN} = –20 V, V_{OUT} = 0 V, V_{ADJ} = 5 V	-0.5		0.5	
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			15		°C

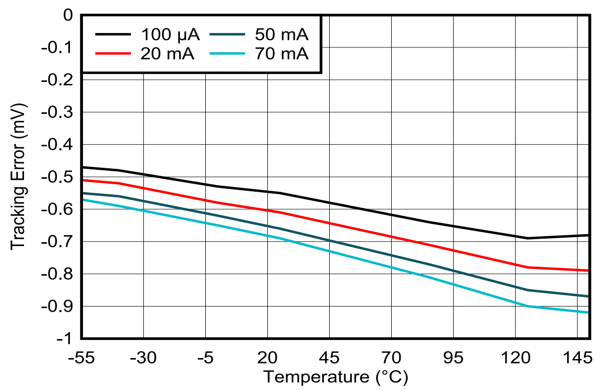
(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. Please see the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150℃.

6.6 Timing Characteristics

specified at V_{IN} = 13.5 V, I_{OUT} = 100 µA, C_{OUT} = 1 µF, C_{IN} = 1 µF, and V_{ADJ} = 5 V (unless otherwise noted), and V_{ADJ} = 5 V (unless otherwise noted); typical values are at T_J = 25°C

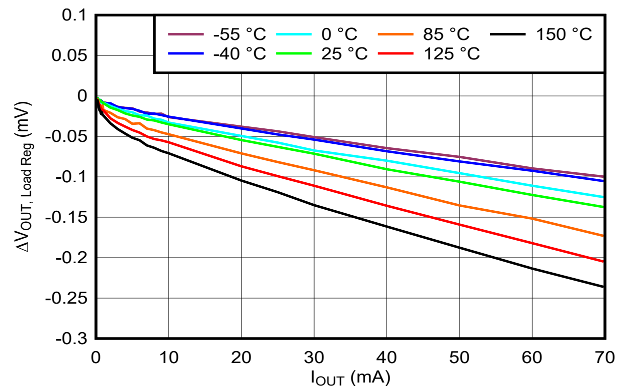
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing Characteristics						
$t_{startup}$	Start-up time	Time from EN high to V_{OUT} = 95% × V_{ADJ}		255		µs

6.7 Typical Characteristics



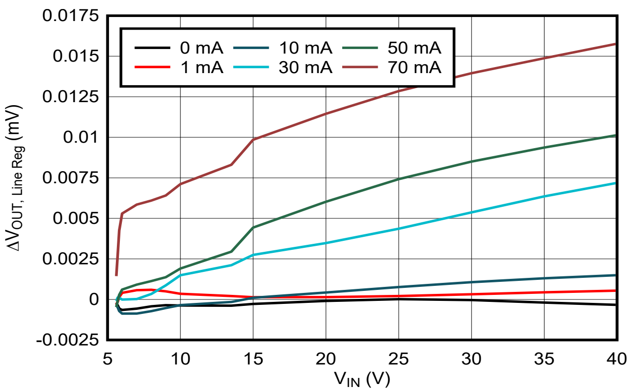
V_{IN} = 13.5 V, V_{ADJ} = 5 V

图 6-1. Tracking Error vs Ambient Temperature



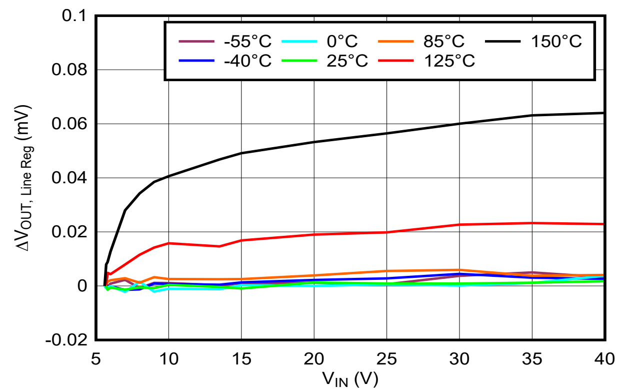
V_{IN} = 13.5 V, V_{ADJ} = 5 V

图 6-2. Load Regulation



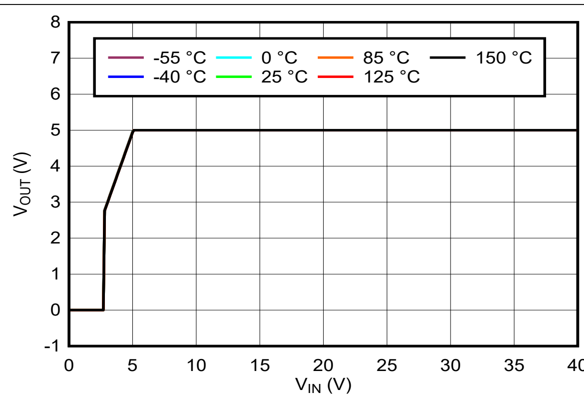
V_{ADJ} = 5 V, T_{AMB} = 25°C

图 6-3. Line Regulation



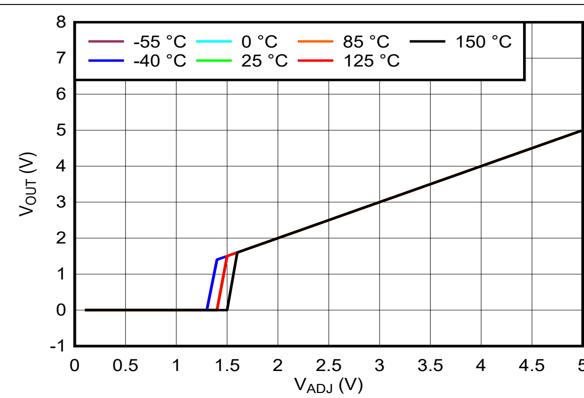
V_{ADJ} = 5 V, I_{OUT} = 10 mA

图 6-4. Line Regulation



V_{ADJ} = 5 V, I_{OUT} = 10 mA

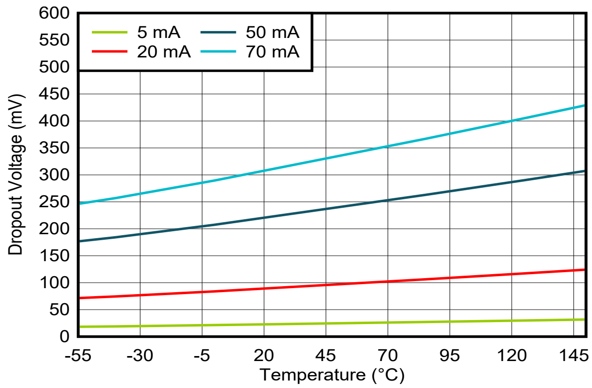
图 6-5. Output Voltage vs Input Voltage



V_{IN} = 13.5 V, I_{OUT} = 10 mA

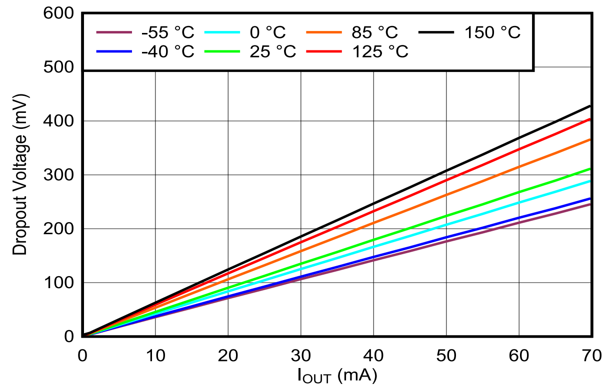
图 6-6. Output Voltage vs Adjustable Reference Voltage

6.7 Typical Characteristics (continued)



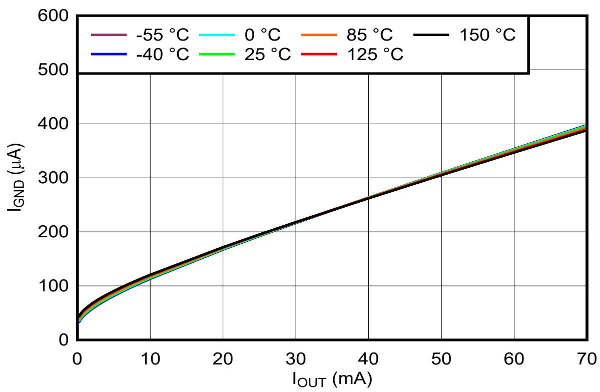
V_{IN} = 5 V, V_{ADJ} = 5 V

图 6-7. Dropout Voltage vs Ambient Temperature



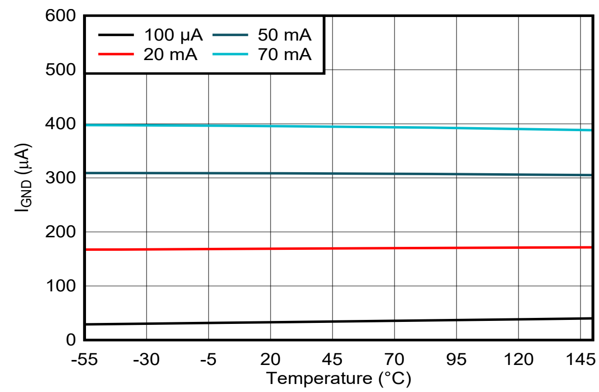
V_{IN} = 5 V, V_{ADJ} = 5 V

图 6-8. Dropout Voltage vs Output Current



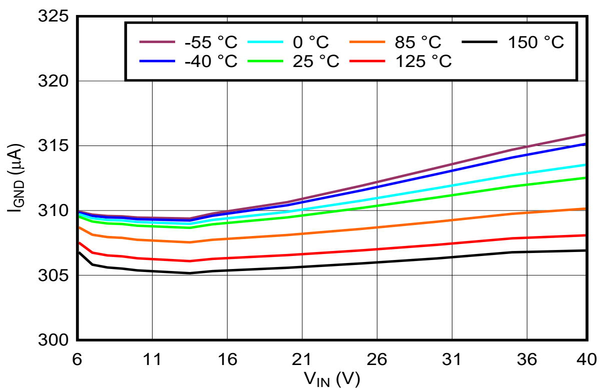
V_{IN} = 13.5 V, V_{ADJ} = 5 V

图 6-9. Ground Current vs Output Current



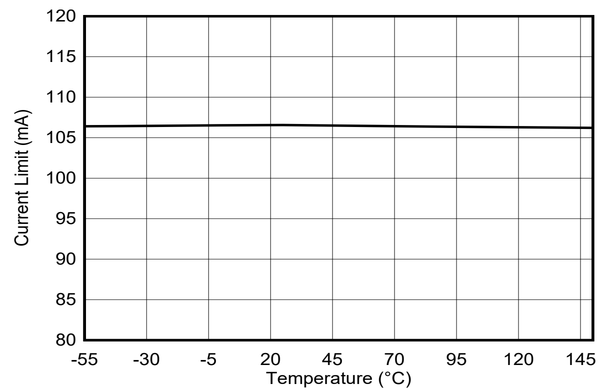
V_{IN} = 13.5 V, V_{ADJ} = 5 V

图 6-10. Ground Current vs Ambient Temperature



V_{ADJ} = 5 V, I_{OUT} = 50 mA

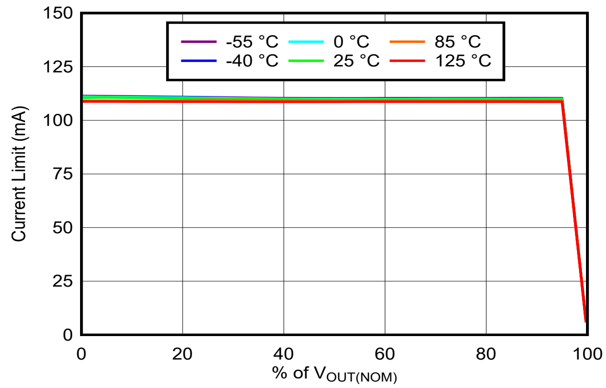
图 6-11. Ground Current vs Input Voltage



V_{IN} = 13.5 V, V_{ADJ} = 5 V

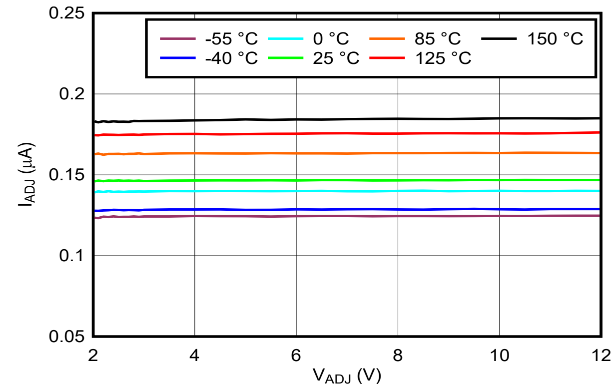
图 6-12. Current Limit vs Ambient Temperature

6.7 Typical Characteristics (continued)



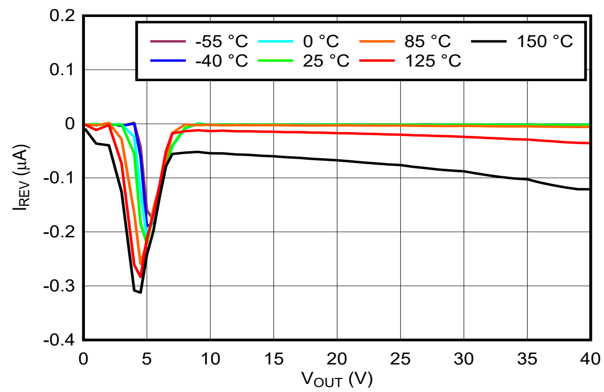
V_{IN} = 13.5 V, V_{ADJ} = 5 V

图 6-13. Current Limit Profile vs. Output Voltage



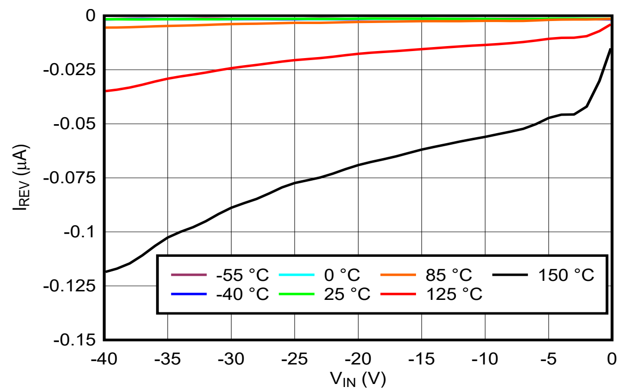
V_{IN} = 13.5 V, I_{OUT} = 0 mA

图 6-14. Adjustable Pin Current vs Adjustable Pin Voltage



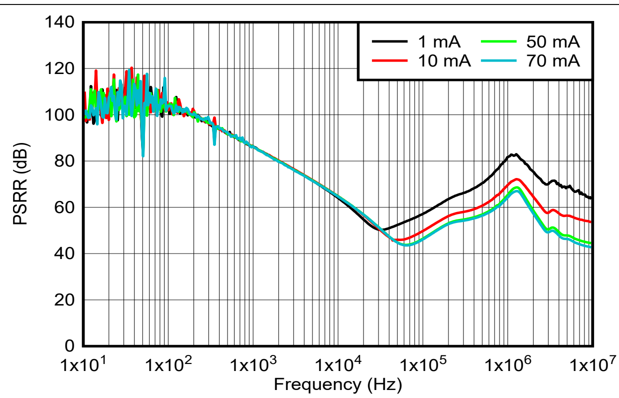
V_{IN} = 0 V, V_{ADJ} = 5 V

图 6-15. Reverse Current vs Output Voltage



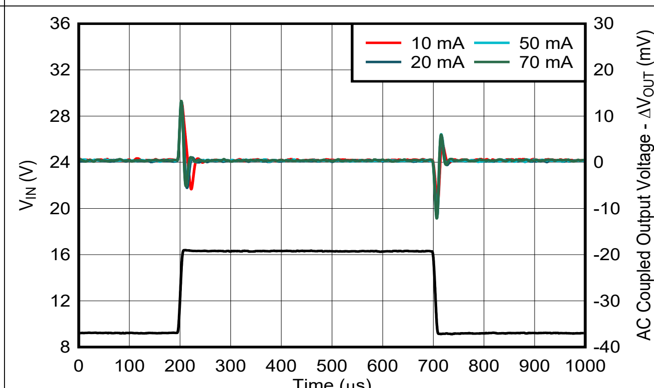
V_{OUT} = 0 V, V_{ADJ} = 5 V

图 6-16. Reverse Current vs Input Voltage



V_{IN} = 13.5 V, V_{ADJ} = 5 V, C_{OUT} = 10 µF, T_{AMB} = 25°C

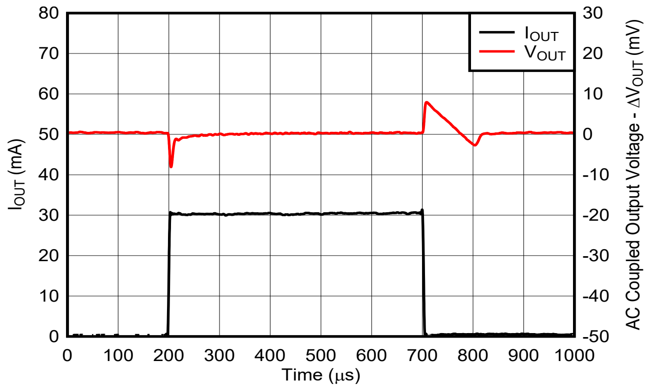
图 6-17. Power-Supply Rejection Ratio vs Frequency



V_{ADJ} = 5 V, C_{OUT} = 10 µF, V_{IN} = 9 V to 16 V,
V_{IN} ramp rate = 1 V/µs

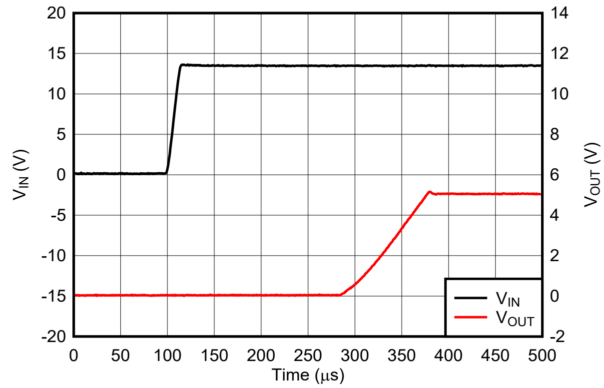
图 6-18. Line Transient

6.7 Typical Characteristics (continued)



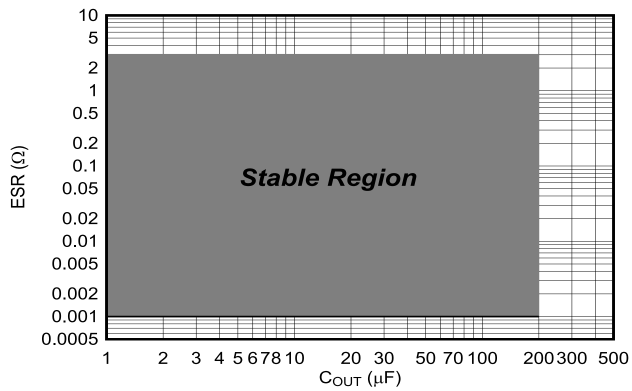
V_{IN} = 13.5 V, V_{ADJ} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 1 mA to 30 mA, I_{OUT} ramp rate = 1 A/µs

图 6-19. Load Transient



V_{IN} = 13.5 V, V_{ADJ} = 5 V, V_{IN} rate of rise = 1 V/µs, C_{OUT} = 1 µF

图 6-20. Start-Up Profile



1 mΩ ≤ ESR ≤ 3 Ω, 1 µF ≤ C_{OUT} ≤ 200 µF

图 6-21. ESR vs Load Capacitance

7 Detailed Description

7.1 Overview

The TPS7B4255-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering sensors off-board, multiple protection features are built into the LDO including short to battery, short to GND, and reverse current protection.

This device features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), reverse current, and reverse polarity protection.

7.2 Functional Block Diagram

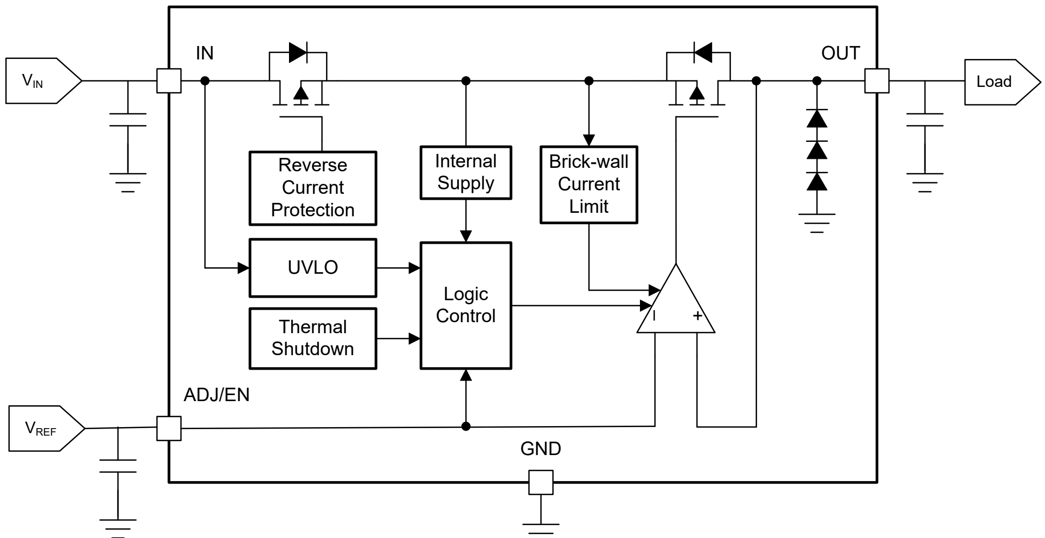


图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Tracker Output Voltage (V_{OUT})

This device is a tracking LDO; thus, with sufficient V_{IN} (⩾3 V) applied, the output voltage is determined by the voltage provided to the ADJ/EN pin. The LDO remains disabled as long as $V_{ADJ/EN}$ is less than V_{IL}. When $V_{ADJ/EN}$ exceeds V_{IH}, the output begins to rise to the voltage on the ADJ/EN pin. The output rises linearly as determined by the load, the output capacitor, and the current limit. When the voltage reaches the level on the ADJ/EN pin, the output voltage remains within 5 mV from the voltage set on the ADJ/EN pin over all specified operating conditions.

7.3.1.1 Output Voltage Equal to the Reference Voltage

As shown in 图 7-2, connect the external reference voltage directly to the ADJ/EN pin. When connected properly, and as given in 方程式 1, the LDO output voltage is equal to the reference voltage.

$$V_{OUT} = V_{REF} \tag{1}$$

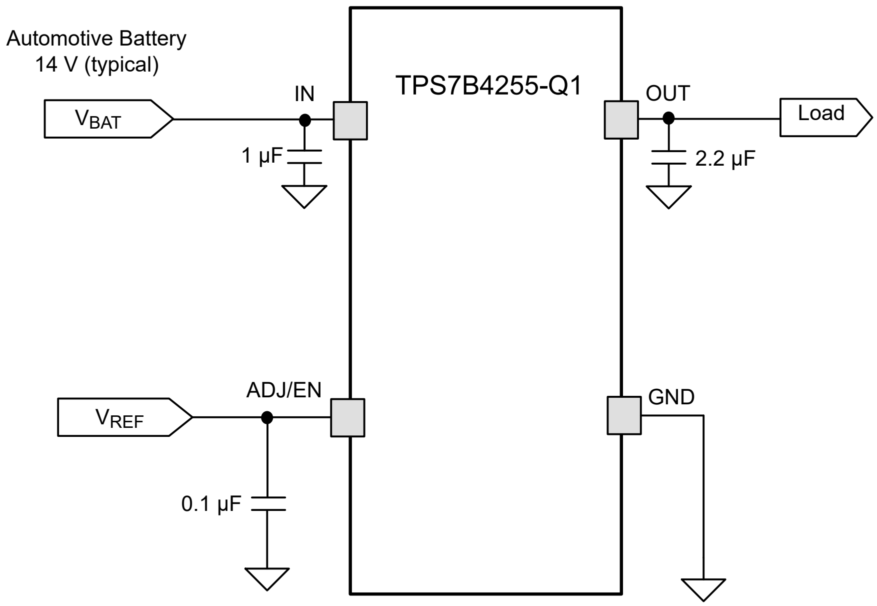


图 7-2. Tracker Output Voltage Equal to the Reference Voltage

7.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ/EN pin, as shown in 图 7-3, can help generate an output voltage that is lower than the reference voltage. Both the R_1 and R_2 resistors must be less than 100 kΩ in value. 方程式 2 calculates V_{OUT}.

$$V_{OUT} = \frac{V_{REF} {}^{*} R_2}{R_1 + R_2} \tag{2}$$

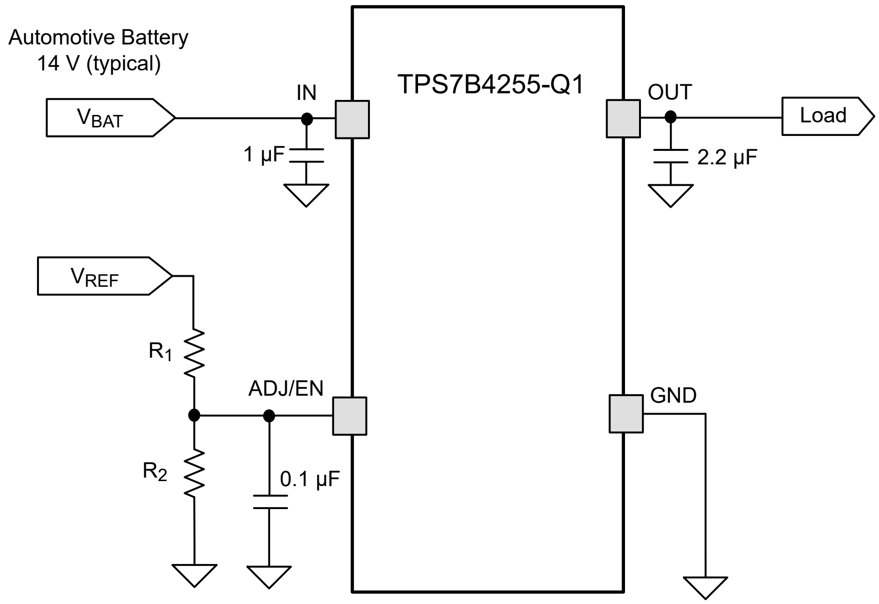


图 7-3. Tracker Output Voltage Lower Than the Reference Voltage

7.3.2 Reverse Current Protection

The TPS7B4255-Q1 incorporates a back-to-back PMOS topology that protects the device from damage against a fault condition, resulting in V_{OUT} being higher than V_{IN} and the subsequent flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the *Absolute Maximum Ratings* are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 1 µs, and along with the body diode of the blocking PMOS transistor, limits the reverse current to I_{REV}.

7.3.3 Undervoltage Lockout

The device has an internally fixed undervoltage lockout threshold. Undervoltage lockout activates when the input voltage V_{IN} drops below the undervoltage lockout (UVLO) level; see the $V_{UVLO(FALLING)}$ parameter in the *Electrical Characteristics* table. This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the *Electrical Characteristics* table).

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the excessive power dissipation condition is removed. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4255-Q1 is designed to protect against overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4255-Q1 into thermal shutdown degrades device reliability.

7.3.5 Current Limit

The device has an internal current limit circuit to protect the device during overcurrent or shorting conditions. The current limit circuit, as shown in 图 7-4, is a brick-wall scheme. When the device is in current limit, the device sources I_{CL} and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

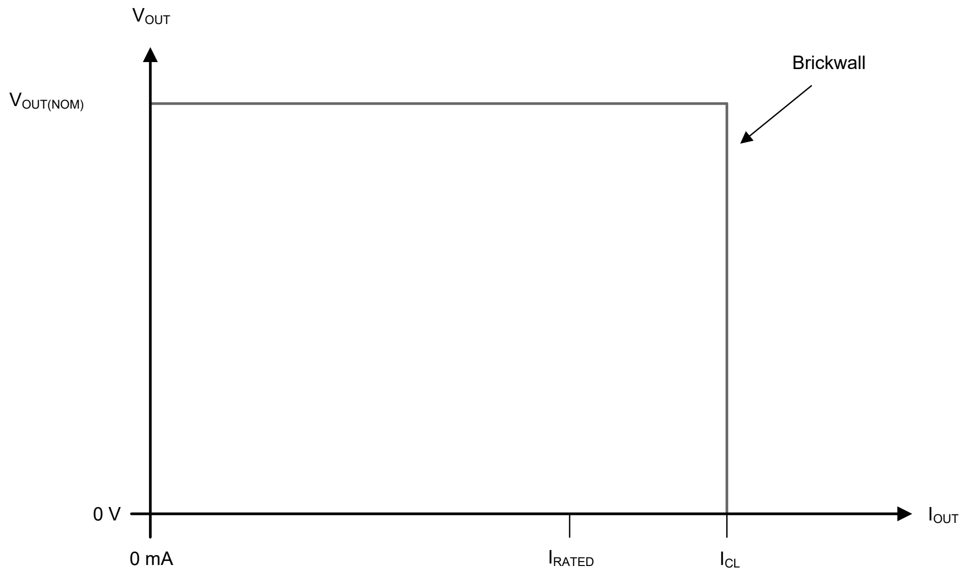


图 7-4. Current Limit: Brick-Wall Scheme

During a current limit event, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage (V_{IN} – V_{OUT}). If the device heats enough, the device can enter thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device can enter thermal shutdown again and continue this cycle until the current limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

7.3.6 Output Short to Battery

When the output is shorted to the supply (as shown in 图 7-5), the TPS7B4255-Q1 survives and no damage occurs to the device. As shown in 图 7-6, a short to the supply can also occur when the device is powered by an isolated supply at a lower voltage. In this example, the TPS7B4255-Q1 supply input voltage is set at 7 V when a short to the main supply (14 V typical) occurs on V_{OUT}, which typically runs at 5 V. The device survives without damage, and the back-to-back PMOS topology helps limit the continuous reverse current that flows out through V_{IN} to less than 0.25 µA.

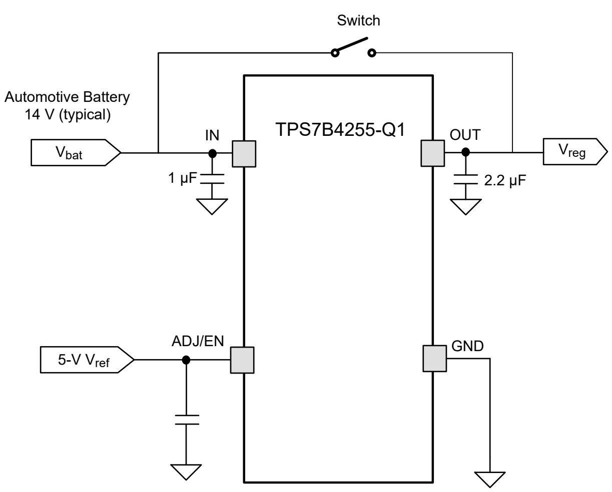


图 7-5. Output Voltage Short to Battery

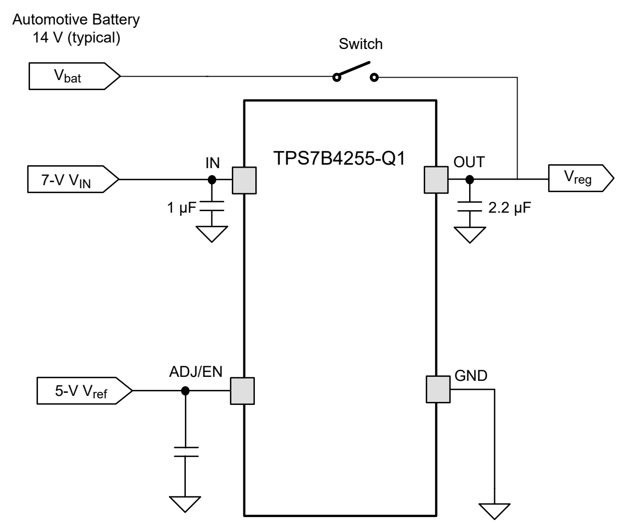


图 7-6. Output Voltage Higher Than the Input

7.3.7 Tracking Regulator With an Enable Circuit

Pulling the reference voltage below V_{IL} disables the device, and the device enters a sleep state where the device draws 3.25 μA (maximum) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur; the device can be configured as shown in 图 7-7 in this case. The TPS7B84-Q1 is a 150-mA LDO with ultra-low quiescent current that provides the reference voltage to both the TPS7B4255-Q1 and the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output (I/O).

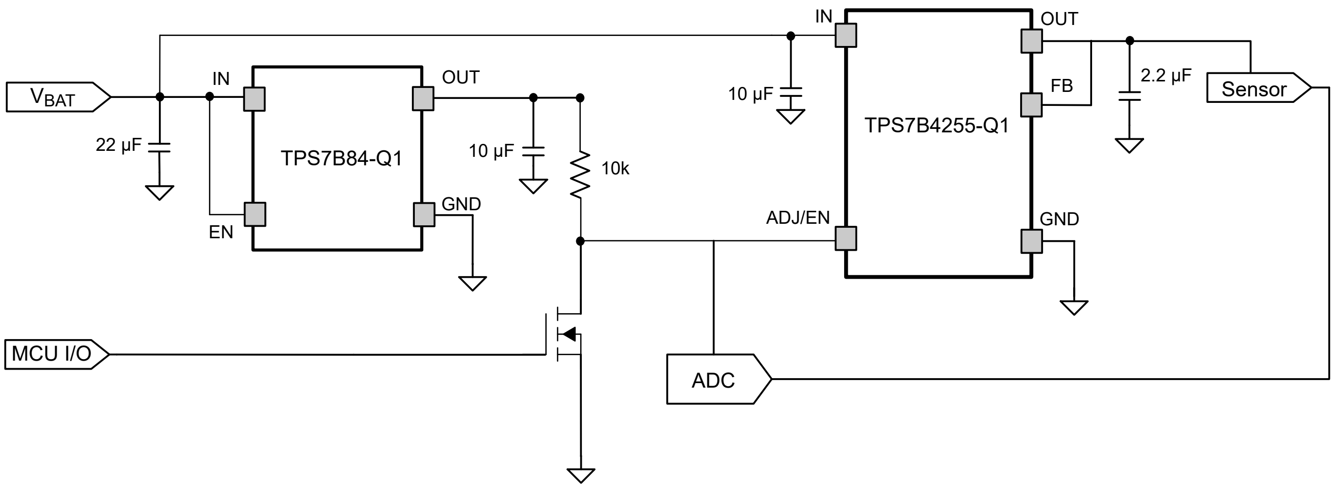


图 7-7. Tracking an LDO With an Enable Circuit

7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ADJ/EN}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(Nom)} + V_{DO}$ and $V_{IN} \geqslant V_{IN(min)}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leqslant I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leqslant I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ADJ/EN} < V_{IL}$	Not applicable	$T_J > T_{SD(shutdown)}$

The device turns on when V_{IN} is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than the enable rising threshold V_{IH}.

7.4.1 Normal Operation

The device output voltage $V_{OUT(Nom)}$ tracks the reference voltage $V_{ADJ/EN}$ when the following conditions are met:

- The input voltage is at least 3 V ($V_{IN(min)}$) and greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The reference voltage at the ADJ/EN pin is greater than the enable rising threshold V_{IH} and stays stable at $V_{OUT(Nom)}$
- The output current is less than $I_{OUT(max)}$ ($I_{OUT} \leqslant 70$ mA)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the saturation region.

7.4.3 Operation With V_{IN} < 3 V

For input voltages below 3 V and above $V_{UVLO(FALLING)}$, the LDO continues to operate but certain circuits can possibly not have the proper headroom to operate within specification. When the input voltage drops below $V_{UVLO(FALLING)}$ the device shuts off.

7.4.4 Disable With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. The output of the device can be shutdown by forcing $V_{ADJ/EN}$ less than V_{IL}. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) when the pass transistor is fully on. This condition arises when the input voltage falls to the point where the error amplifier must drive the gate of the pass transistor to the rail and has no remaining headroom for the control loop to operate. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage directly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage (V_{DO}).

In dropout mode, the output is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients can cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current (I_{RATED}, see the *Recommended Operating Conditions* table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)}=\frac{V_{DO}}{I_{RATED}} \tag{3}$$

8.1.2 Reverse Current

The TPS7B4255-Q1 incorporates reverse current protection that prevents damage from a fault condition, resulting in V_{OUT} being higher than V_{IN}. During such a fault condition, where the V_{IN} and V_{OUT} absolute maximum ratings are not violated and V_{OUT} – V_{IN} is less than 40 V, no damage occurs and less than 0.5 µA of reverse current flows through the LDO. The reverse current comparator typically responds to a reverse voltage condition and, along with the body diode of the blocking PMOS transistor, limits the reverse current in 1 µs.

8.2 Typical Application

图 8-1 shows a typical application circuit for the TPS7B4255-Q1.

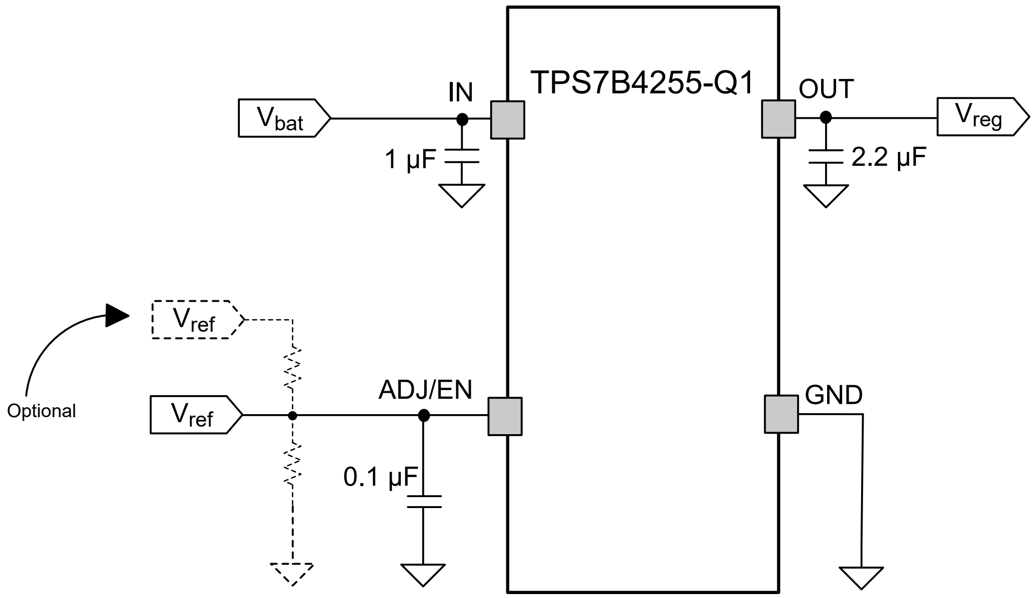


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

Use the parameters listed in 表 8-1 for this design example.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3 V to 40 V
ADJ/EN reference voltage	2 V to 40 V
Output voltage	2 V to 40 V
Output current rating	70 mA
Output capacitor range	1 µF to 200 µF
Output capacitor ESR range	1 mΩ to 3 Ω

8.2.2 Detailed Design Procedure

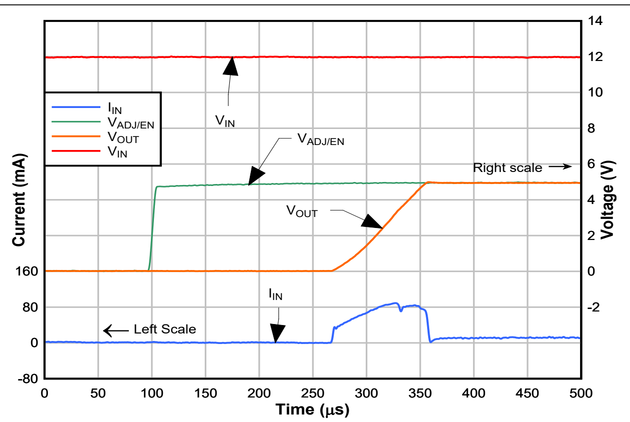
8.2.2.1 Input and Output Capacitor Selection

Depending on the end application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4255-Q1 requires an output capacitor of at least 1 µF (500 nF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 3 Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 200 µF.

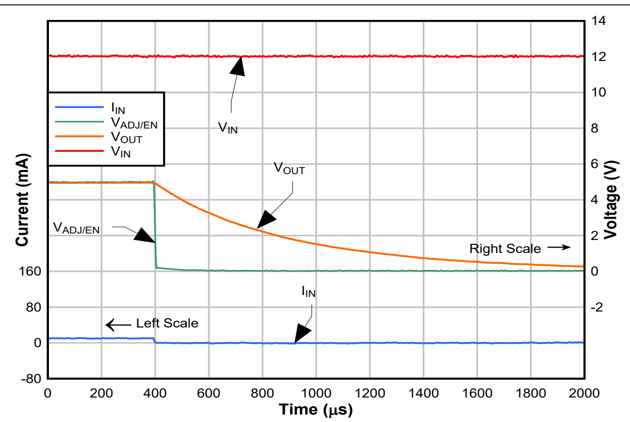
Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND, connected close to the device pins. Some input supplies have a high impedance; thus, placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.2.3 Application Curves



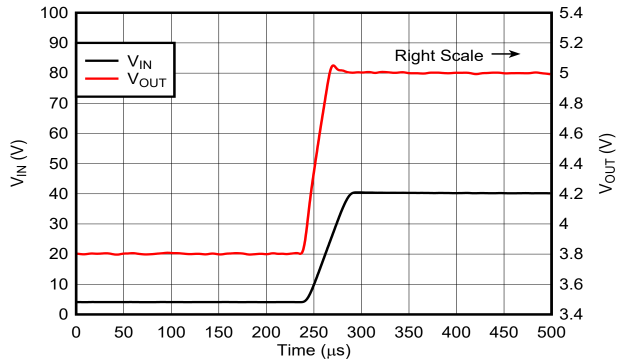
V_{IN} = 12 V, $V_{ADJ/EN}$ = 5 V, $V_{ADJ/EN}$ slew rate = 1 V/ μ s, C_{IN} = C_{OUT} = 1 μ F, R_{LOAD} = 470 Ω

图 8-2. Power-Up



V_{IN} = 12 V, $V_{ADJ/EN}$ = 5 V, $V_{ADJ/EN}$ slew rate = 1 V/ μ s, C_{IN} = C_{OUT} = 1 μ F, R_{LOAD} = 470 Ω

图 8-3. Power-Down



C_{OUT} = 1 µF, $V_{ADJ/EN}$ = 5 V, I_{OUT} = 70 mA, V_{IN} slew rate = 1 V/µs

图 8-4. Dropout Exit Recovery

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4255-Q1 are available at the end of this document and at www.ti.com.

TI's DYB package footprint can be used for both the DYB package as well as the DBV package for easy multisourcing.

8.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to make sure that the maximum performance is as denoted in this product data sheet, use the same layout pattern used for the TPS7B4255-Q1 evaluation board, available at www.ti.com.

8.4.1.3 Power Dissipation and Thermal Considerations

方程式 4 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (4)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT}, the term $I_Q \times V_{IN}$ in 方程式 4 can be ignored.

Calculate the junction temperature (T_J) with 方程式 5 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

方程式 6 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (6)$$

The maximum ambient air temperature (T_{AMAX}) at which the device can operate can be calculated with 方程式 7 for a given maximum junction temperature (T_{JMAX}).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \quad (7)$$

8.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (图 8-5), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

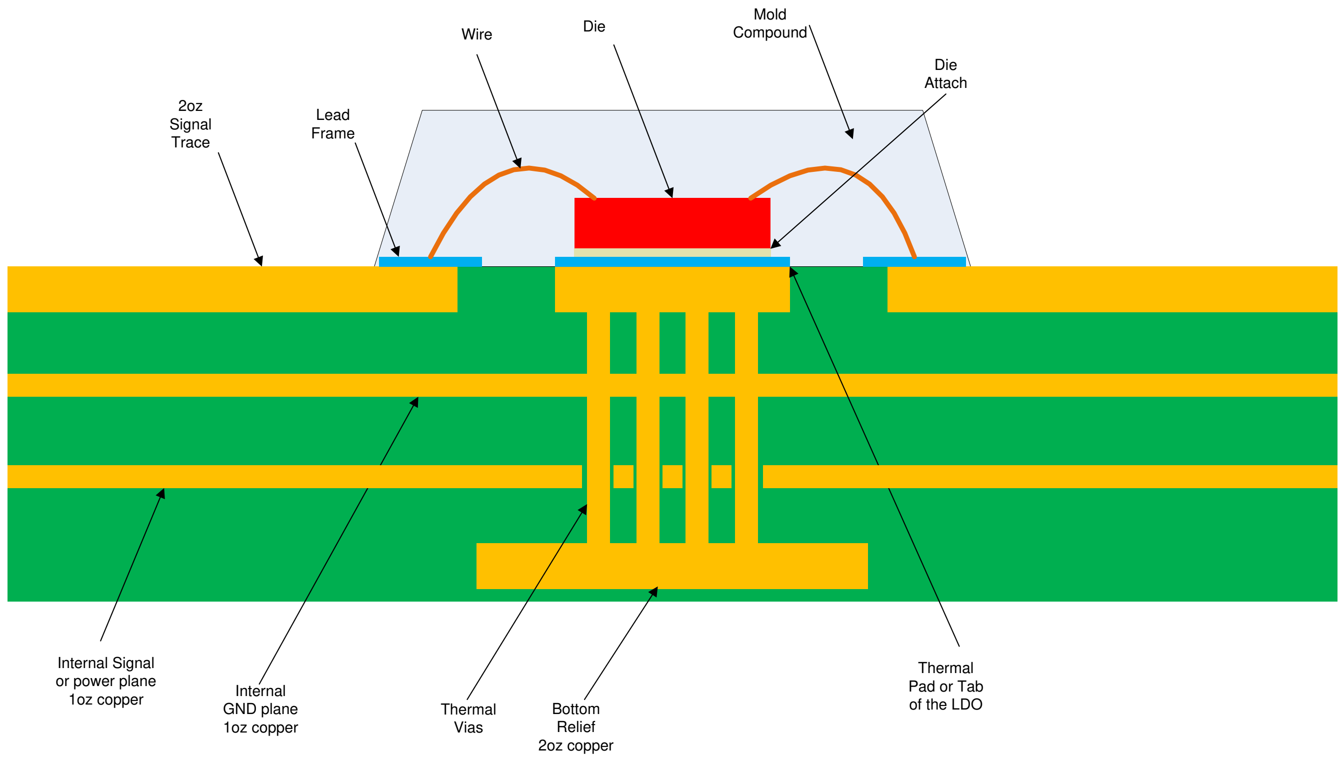


图 8-5. JEDEC Standard 2s2p PCB

图 8-6 through 图 8-9 illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness for the DBV package and DYB package. These plots are generated with a 101.6-mm × 101.6-mm × 1.6-mm PCB of two and four layers. For the 4-layer board, inner planes use 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 4 × 5 (DBV and DYB package) array of thermal vias with a 300-µm drill diameter and 25-µm copper plating is located as close as practical to the GND pin of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area. The *PowerPAD™ Thermally Enhanced Package* application note discusses the impact that thermal vias have on thermal performance.

As shown in 图 8-7, ψ_{JB} increases with additional connecting copper area. The reason for this increase is that the board temperature is measured at the copper near the GND pin, and because the GND pin is fused to the die pad, more heat escapes through the GND pin when more copper is connected to the pad, and thus the temperature at this point is higher. Consequently the ψ_{JB} increases. This increase does not imply that heat sinking for the device is reduced when more connecting copper is added. Increasing connecting copper area always increases board-level heat sinking for the device. Furthermore, the boards used for 图 8-7 have vias connecting to internal copper planes. Therefore, ψ_{JB} is much higher than what is specified in the *Thermal Information* table, which uses the high-K board layout specified in JESD51-7 that has no thermal vias.

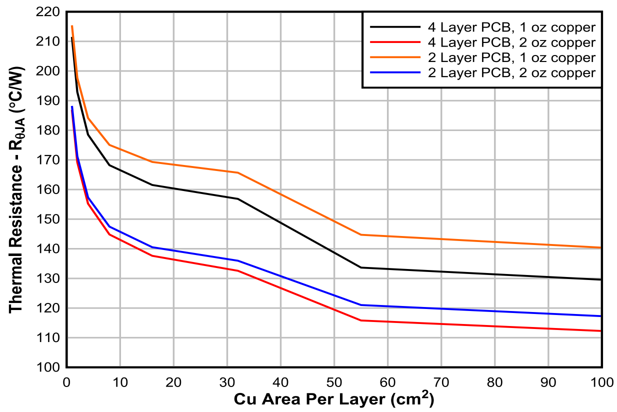


图 8-6. $R_{\theta JA}$ vs Copper Area (DBV Package)

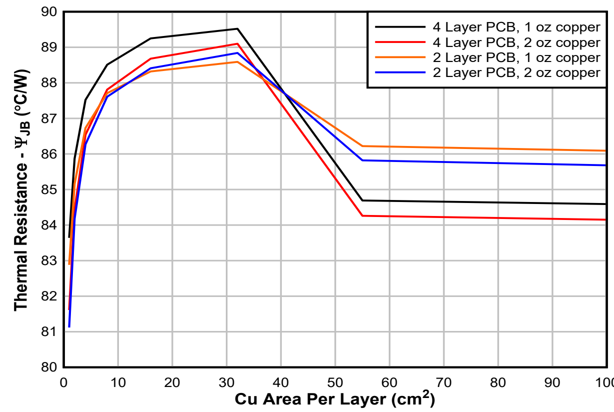


图 8-7. ψ_{JB} vs Copper Area (DBV Package)

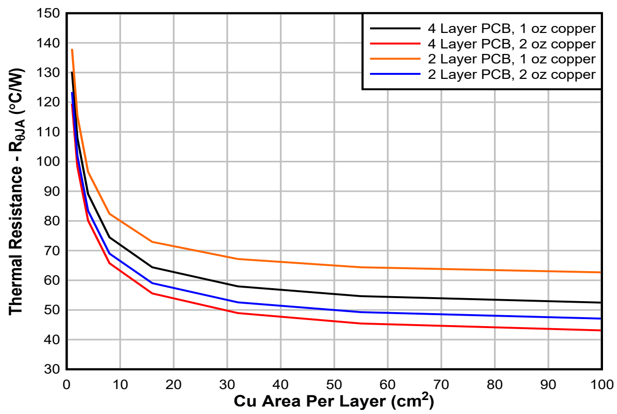


图 8-8. $R_{\theta JA}$ vs Copper Area (DYB Package)

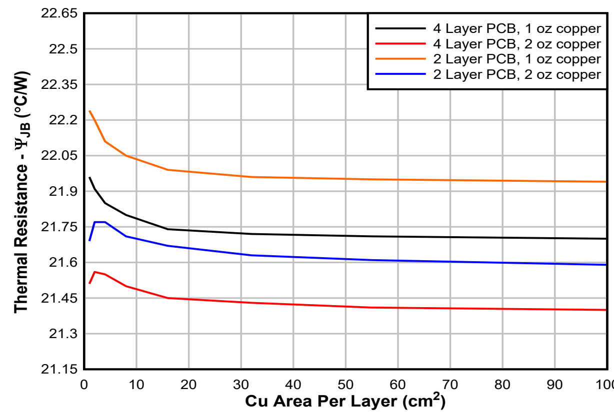
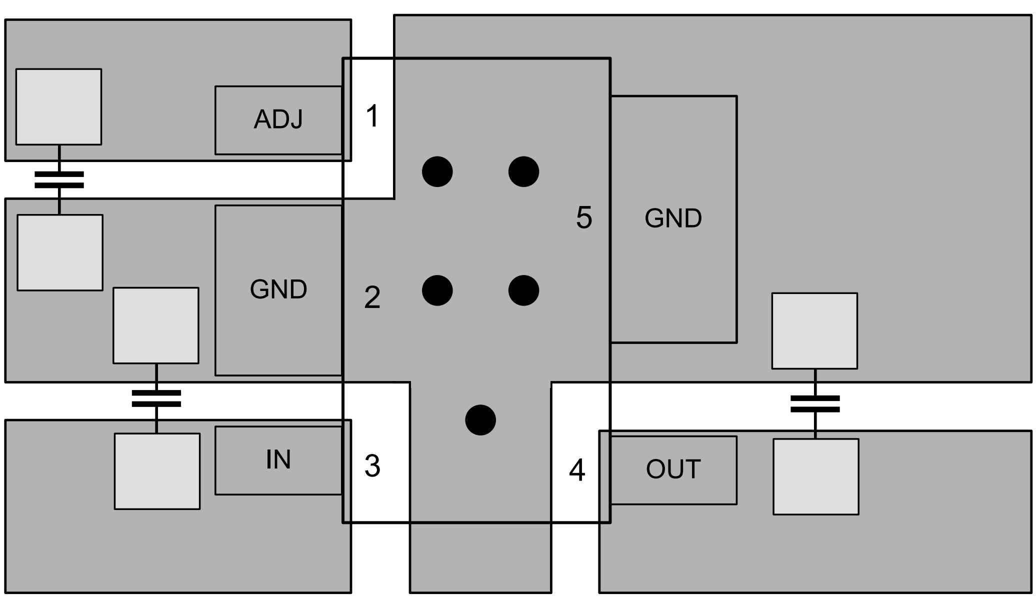


图 8-9. ψ_{JB} vs Copper Area (DYB Package)

8.4.2 Layout Examples



● Circles denote PCB via connections

图 8-10. DYB Package Layout Example

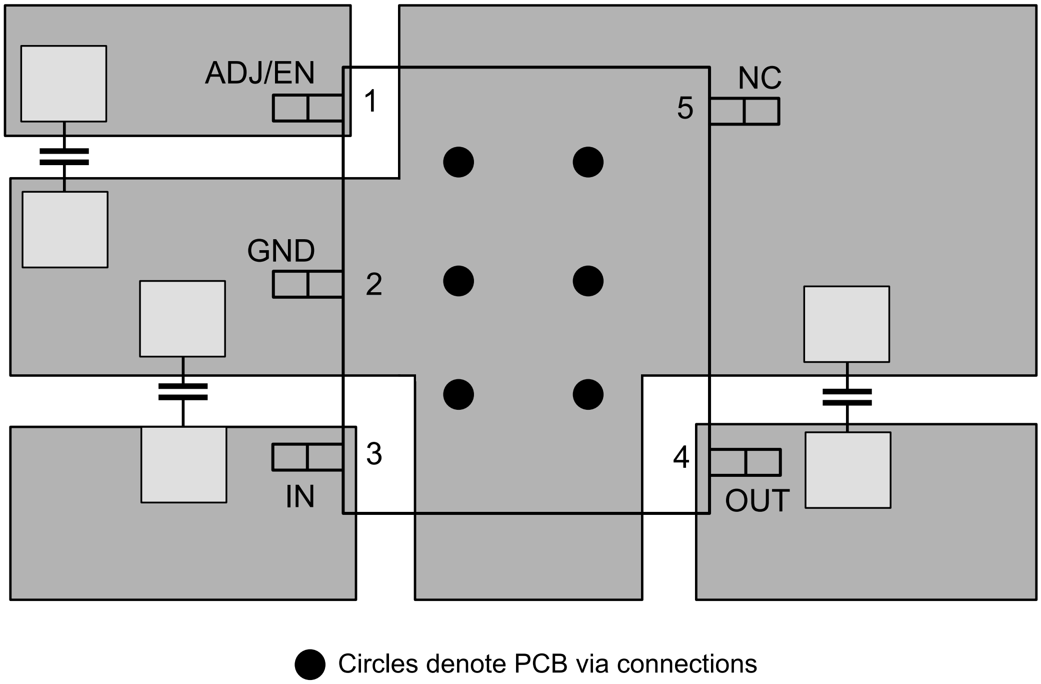


图 8-11. DBV Package Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

表 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7B4255**Q yyyR Q1**	**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **R** is the packaging quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

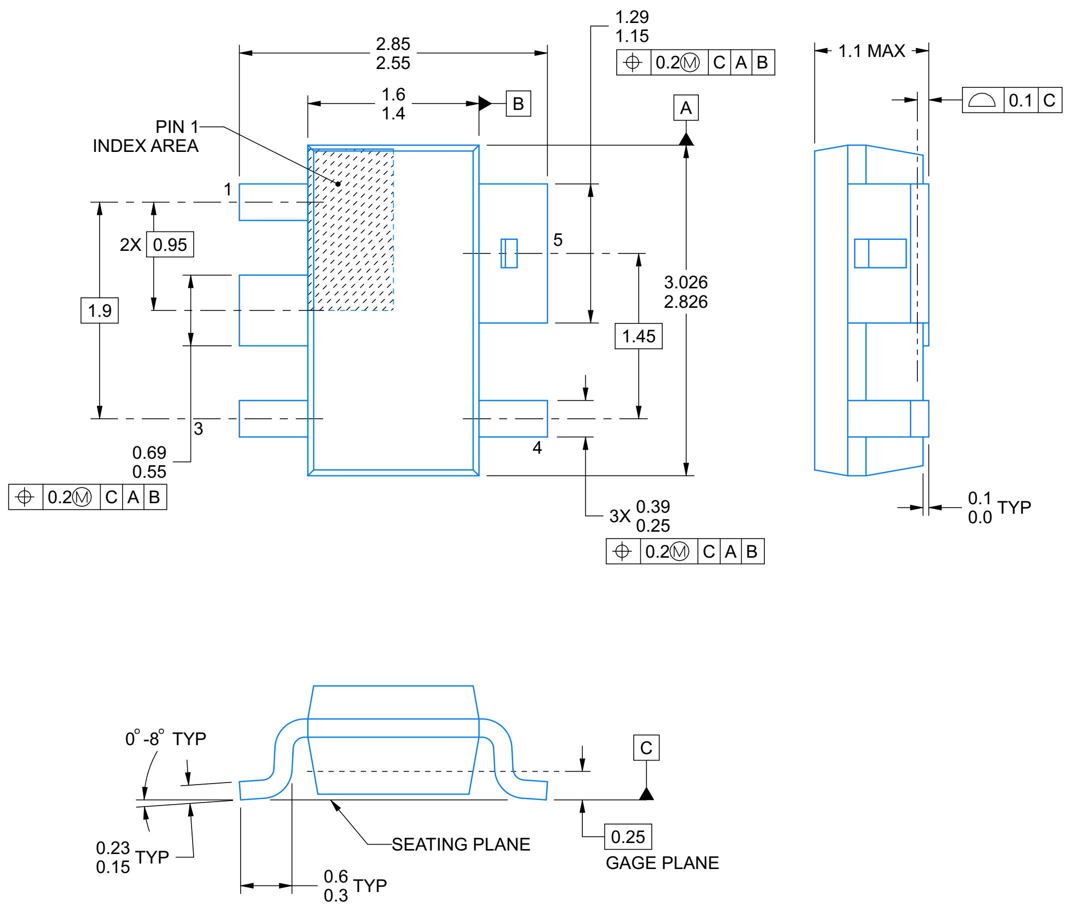
10.1 Mechanical Data

PACKAGE OUTLINE

DYB0005A

SOT - 1.1 max height

SOT



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NOTES:

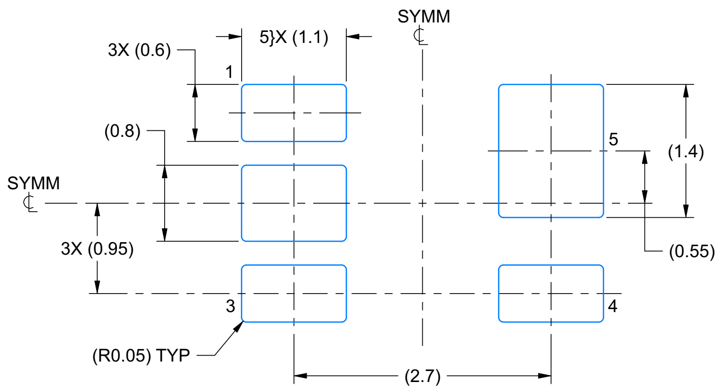
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No JEDEC reference as of August 2020.

www.ti.com

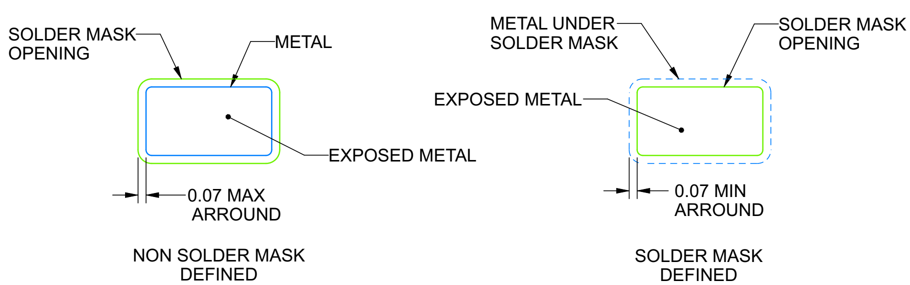
EXAMPLE BOARD LAYOUT

DYB0005A SOT - 1.1 max height

SOT



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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NOTES: (continued)

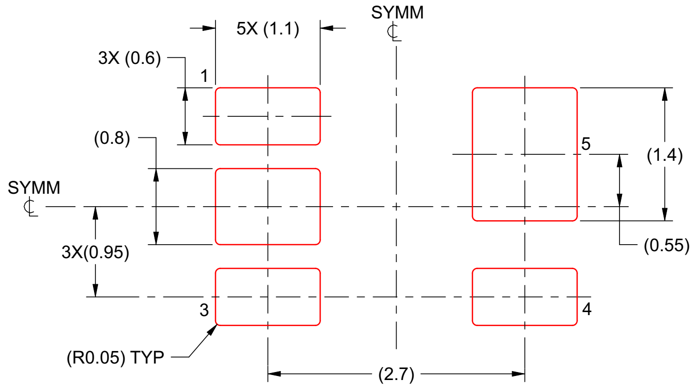
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

www.ti.com

EXAMPLE STENCIL DESIGN

DYB0005A SOT - 1.1 max height

SOT



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4226199/A 09/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B4255QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2Q5F
TPS7B4255QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2Q5F
TPS7B4255QDYBRQ1	Active	Production	SOT-23 (DYB) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q6T
TPS7B4255QDYBRQ1.A	Active	Production	SOT-23 (DYB) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q6T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

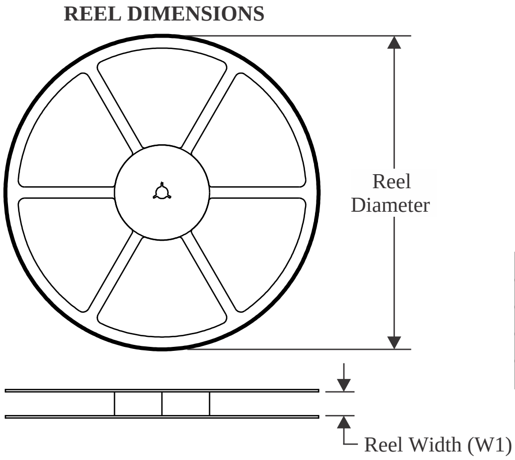
OTHER QUALIFIED VERSIONS OF TPS7B4255-Q1 :

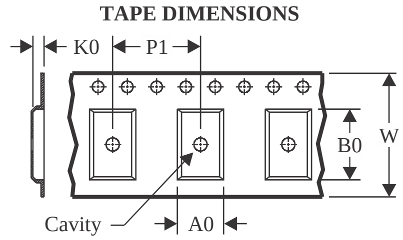
- Catalog : TPS7B4255

NOTE: Qualified Version Definitions:

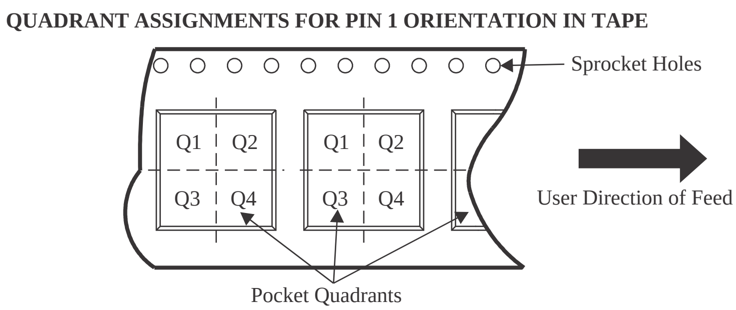
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





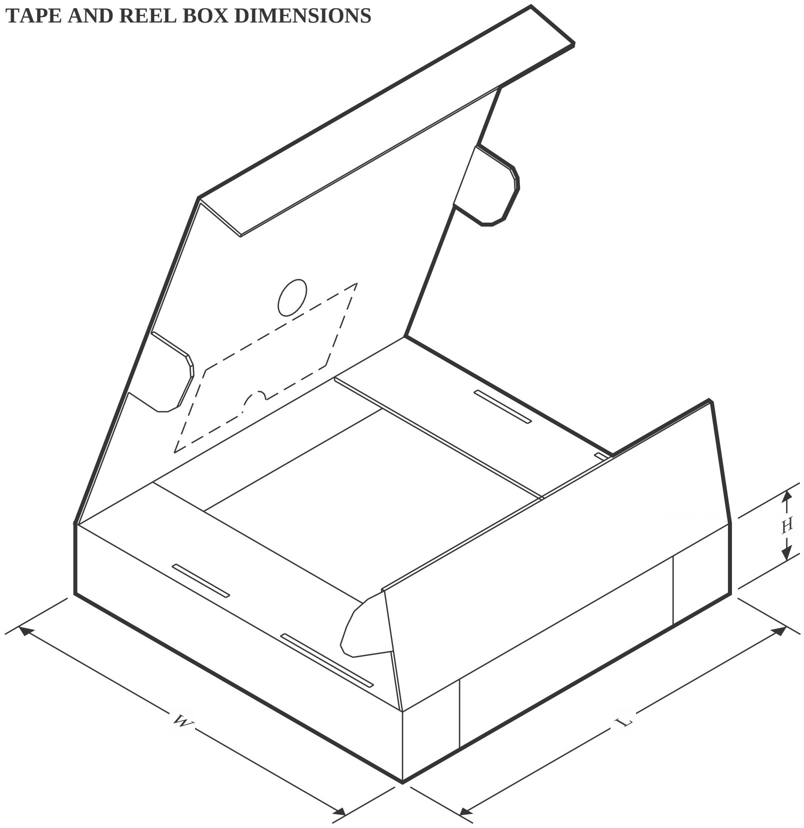
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

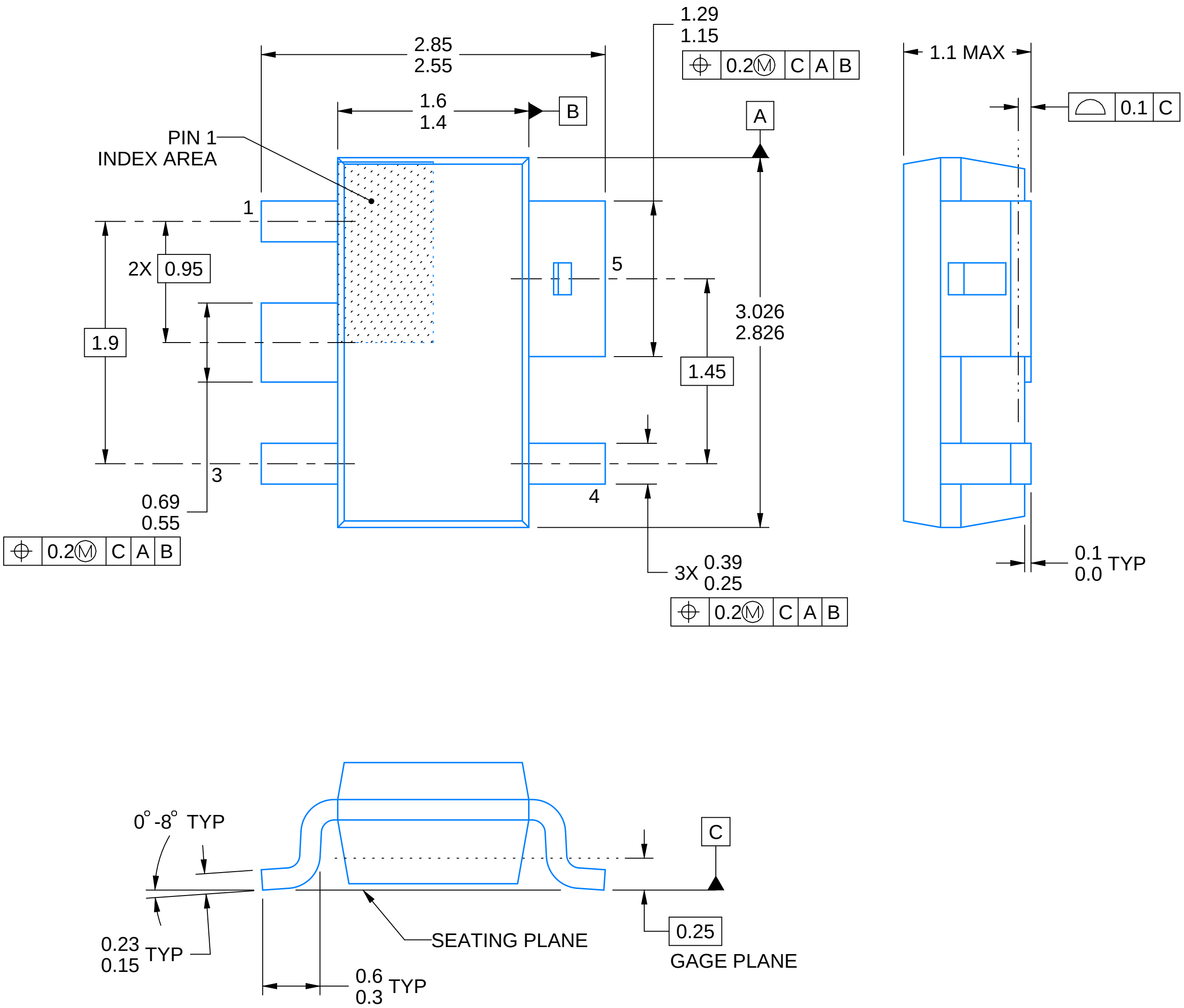
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4255QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7B4255QDYBRQ1	SOT-23	DYB	5	3000	178.0	9.0	3.2	3.05	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

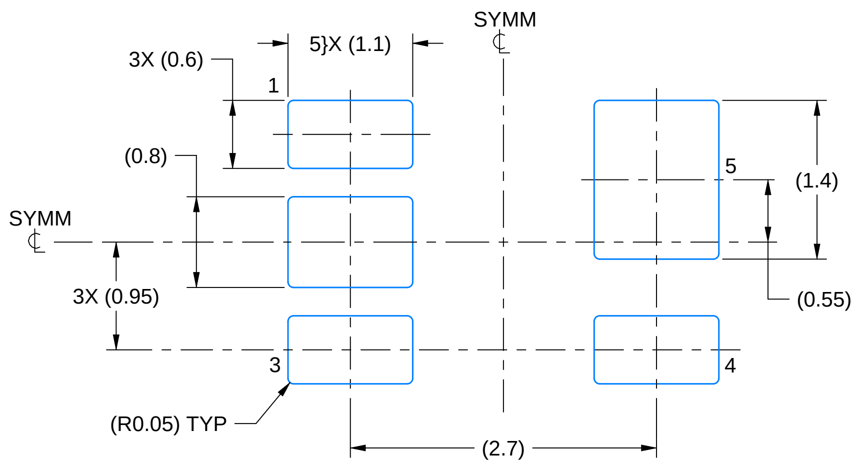
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4255QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7B4255QDYBRQ1	SOT-23	DYB	5	3000	180.0	180.0	18.0



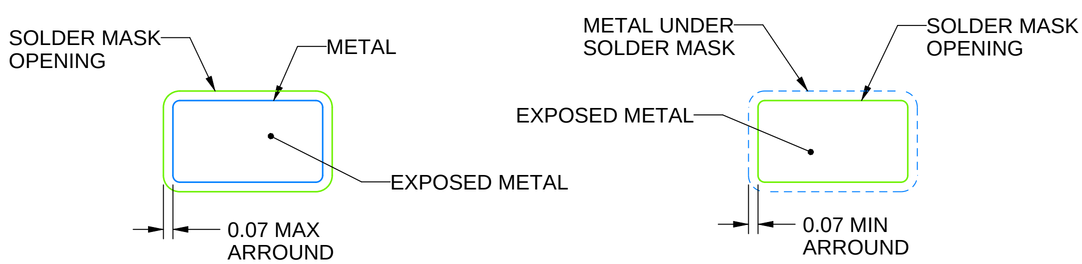
4226199/A 09/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No JEDEC reference as of August 2020.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED

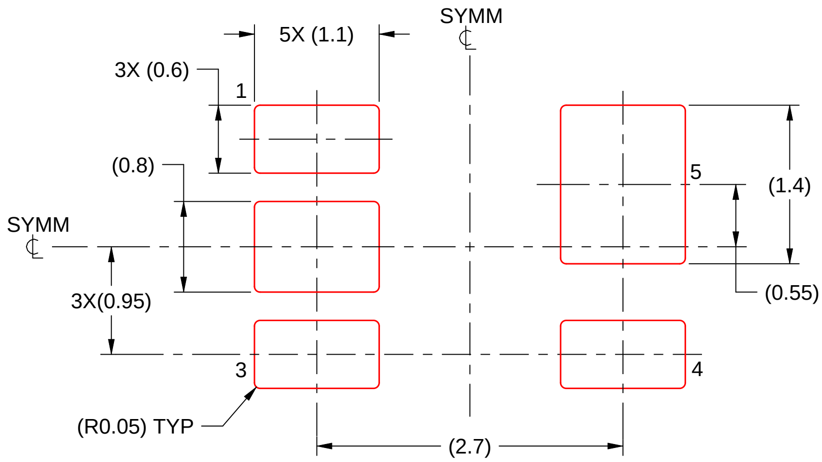
SOLDER MASK DEFINED

SOLDERMASK DETAILS

4226199/A 09/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

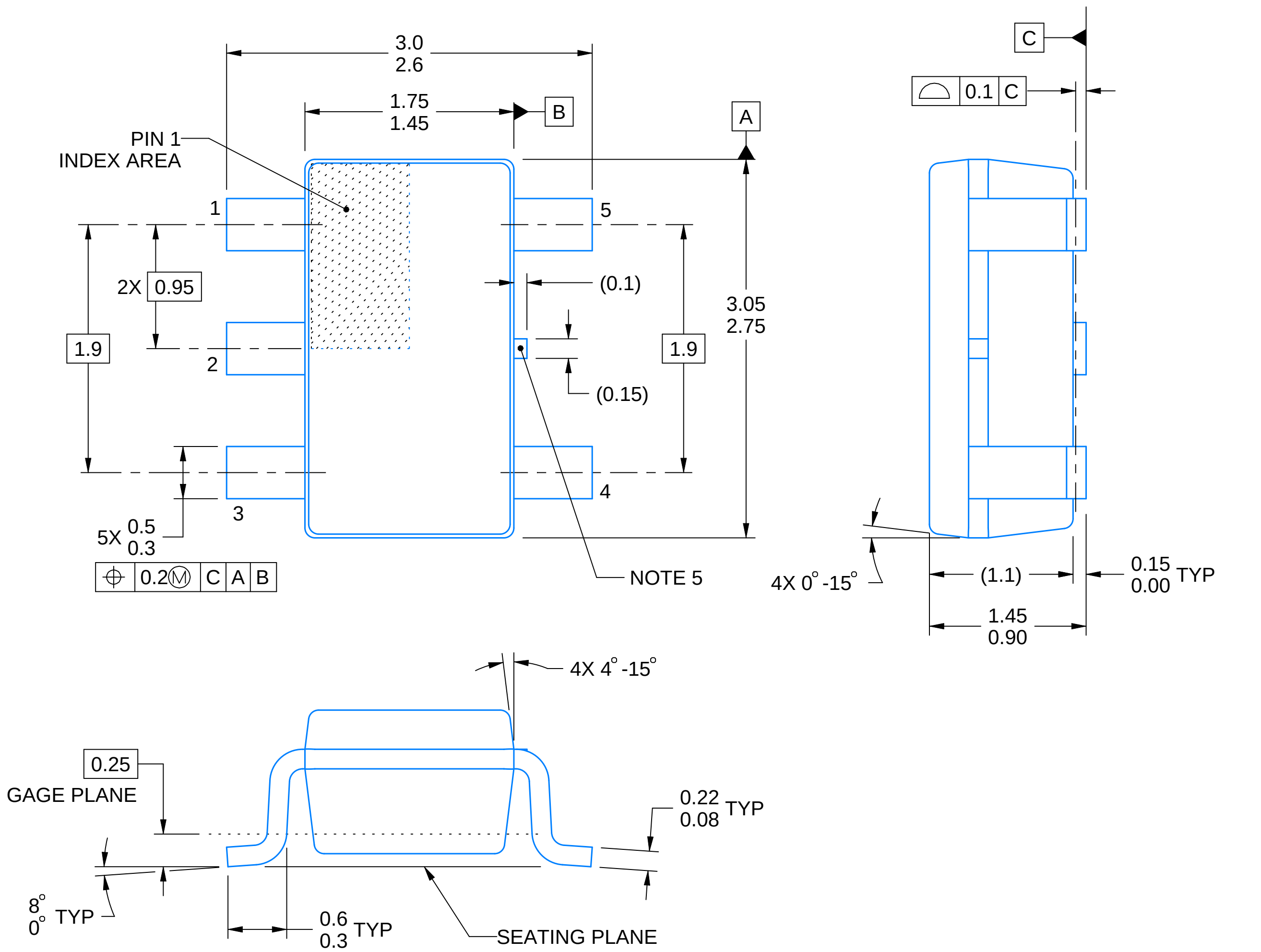


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4226199/A 09/2020

NOTES: (continued)

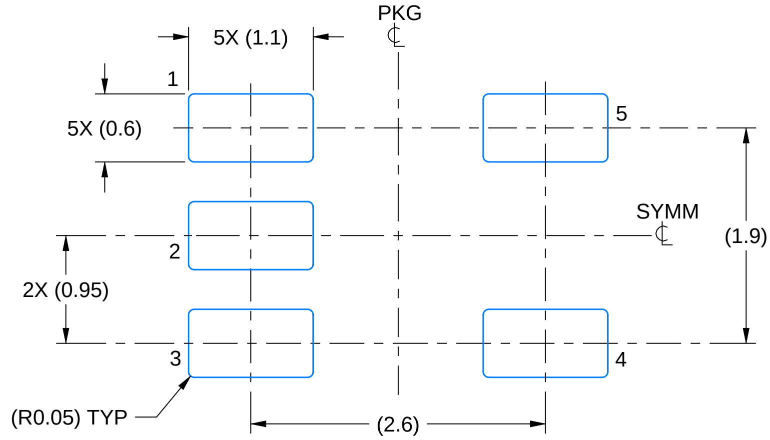
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



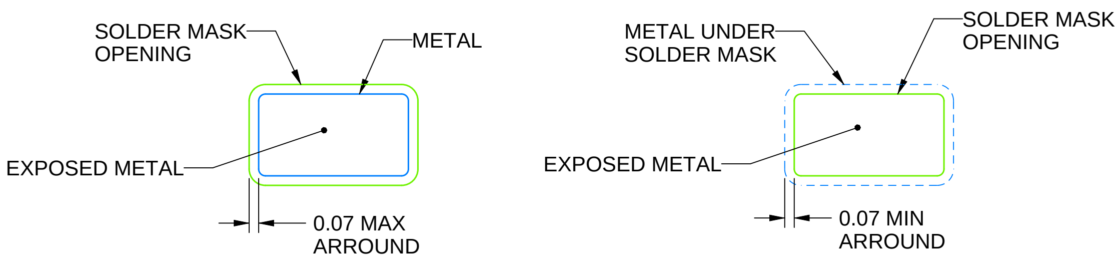
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

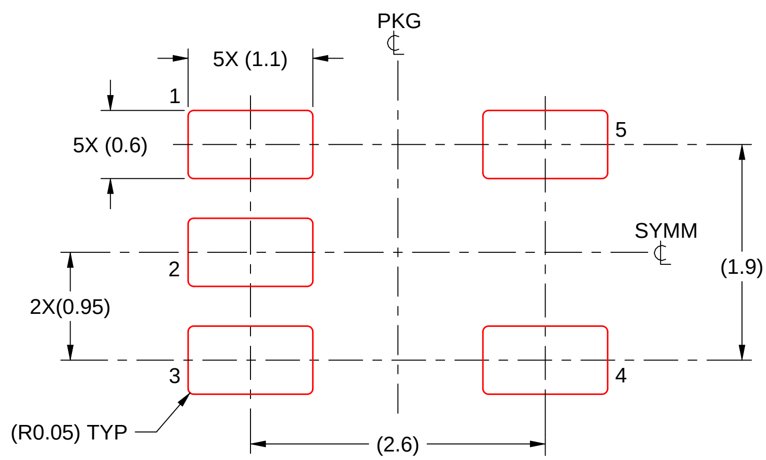
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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