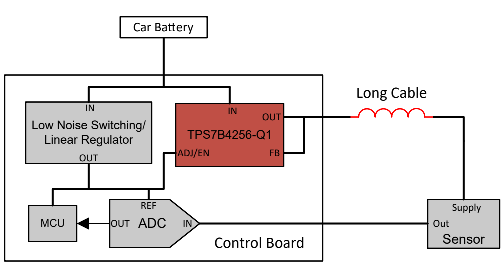
TPS7B4256-Q1 具有 6mV 跟踪容差的汽车类 70mA、40V 电压跟踪 LDO

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 结温：–40°C 至 +150°C，T_J
- 宽输入电压范围：
  - 绝对最大电压范围：-40V 至 +45V
  - 工作范围：3V 至 40V
- 输出电压：
  - 宽工作电压范围：2V 至 40V
  - 输出电压灵活性：在分压器配置中，使用外部电阻器可将 V_{OUT} 调整为高于或低于基准的电压值
- 最大输出电流：70mA
- 非常严格的输出跟踪容差：6mV（最大值）
- 低压降：70mA 时为 225mV（最大值）
- 组合了使能和基准功能
- 轻负载时低静态电流：60μA
- 在各种陶瓷输出电容值范围内可保持稳定：
  - C_{OUT} 范围：1μF 至 100μF
  - ESR 范围：1mΩ 至 2Ω
- 集成保护特性：
  - 反向电流保护
  - 反极性保护
  - 过热保护
  - 提供输出至地和输出至电源短路保护
- 采用以下低热阻 8 引脚封装：
  - HSOIC (DDA)，$R_{θJA}$ = 53.3°C/W
  - SOIC (D)，$R_{θJA}$ = 101°C/W

2 应用

- 动力总成压力传感器
- 动力总成温度传感器
- 动力总成排气传感器
- 动力总成油液浓度传感器
- 车身控制模块 (BCM)



典型应用

3 说明

TPS7B4256-Q1 是一款单片集成低压降 (LDO) 电压跟踪器。该器件采用 8 引脚 SOIC 和 HSOIC 封装。TPS7B4256-Q1 旨在为汽车环境中的非板载传感器供电。由于提供非板载电源的电缆发生故障的风险较高，因此器件配备了集成保护功能，可应对电池短路、反极性、输出至地短路（电流限制）和过热（热关断）等故障情况。该器件采用背对背 PMOS 拓扑，无需使用外部二极管，即可帮助防止出现导致反向电流的故障情况。该器件可承受 45V（绝对最大值）输入电压，并能经受住汽车负载突降瞬态条件的考验。

该器件可在整个温度范围内跟踪施加在可调节输入引脚 (ADJ/EN) 上的基准电压，并在 FB 引脚上具有非常严格的 6mV（最大值）容差。凭借这种跟踪功能，TPS7B4256-Q1 可在高达 70mA 的负载下提供高精度电源电压。基准电压可直接连接至 ADJ/EN 引脚，或通过 ADJ/EN 引脚的外部电阻分压器调整为更低的电压值（最低至 2V）。通过直接将 FB 引脚连至 OUT 引脚，输出电压可调整为 ADJ/EN 引脚电压值（± 跟踪容差）；通过 FB 和 OUT 引脚之间的电阻分压器，输出电压可调整为更高的电压值。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS7B4256-Q1	DDA（HSOIC，8）	4.9mm × 6mm
	D（SOIC，8）	

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

TPS7B4256-Q1 可对 ADC 基准电压进行有效的缓冲，并通过长线缆安全传输此电压（或其调整值）来为非板载传感器供电。如果传感器是比例式的，而且输出由 ADC 进行采样，则 TPS7B4256-Q1 所述特性将有助于显著提高传感器测量的可靠性和精度。

通过将 ADJ/EN 输入引脚置于低电平，TPS7B4256-Q1 可切换至待机模式，从而将 LDO 的静态电流消耗降至 3.5µA 以下。

Table of Contents

4 Pin Configuration and Functions

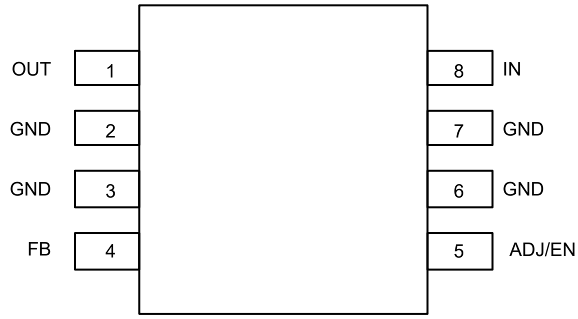


图 4-1. D Package, 8-Pin SOIC (Top View)

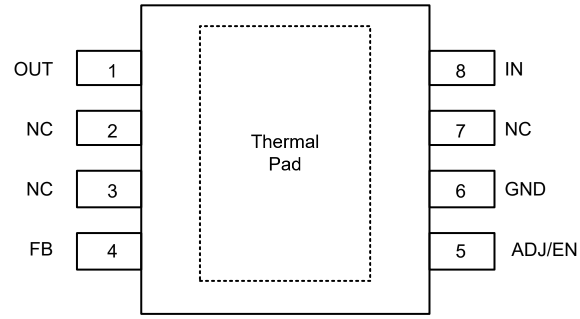


图 4-2. DDA Package, 8-Pin HSOIC (Top View)

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	D	DDA		
ADJ/EN	5	5	I	Adjustable/enable input pin. Connect the external reference voltage to this pin. This pin connects to the inverting input of the error amplifier internally. A low signal below V_{IL} disables the device, and a high signal above V_{IH} enables the device. Connect the voltage reference directly, or with a voltage divider to attain output voltages lower than the reference; see the *Tracker Output Voltage (V_{OUT})* section for more details. To compensate for line influences, place a 0.1-µF capacitor close to this pin.
FB	4	4	I	Feedback pin. This pin is connected to the noninverting input of the error amplifier internally and can be used to control the output voltage. For output voltages equal to or less than the external reference voltage, connect this pin directly to the output pin. To attain output voltage values higher than the reference, use a voltage divider with external feedback resistors; see the *Tracker Output Voltage (V_{OUT})* section for more details.
GND	2, 3, 6, 7	6	G	GND pin. Connect this pin to a low impedance path to ground.
IN	8	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND, as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the input pin of the device as possible to compensate for line influences.
NC	—	2, 3, 7	—	Not internally connected. For best thermal performance, connect these pins to GND.
OUT	1	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to GND; see the *Recommended Operating Conditions* table. Place the output capacitor as close to output of the device as possible.
Thermal Pad	—	Pad		Thermal pad. Connect the pad to GND for best possible thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{IN}	Unregulated input	–40	45	V
V_{OUT}	Regulated output	–5	45	V
V_{FB}	Feedback	–5	45	V
$V_{ADJ/EN}$	Adjustable reference and enable input voltage	–40	45	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may effect the device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2500	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins		

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage	2		40	V
$V_{ADJ/EN}$	Adjust pin voltage	2		40	V
V_{FB}	Feedback pin voltage	0		40	V
I_{OUT}	Output current	0		70	mA
C_{IN}	Input capacitor[(1)]		1		µF
C_{OUT}	Output capacitor[(2)]	1		100	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance recommended is 500 nF.
(2) Effective output capacitance of 500 nF minimum is required for stability.

5.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		TPS7B4256-Q1 D (SOIC) 8 PINS	TPS7B4256-Q1 DDA (HSOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.9	53.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.3	28.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.9	28	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	13.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The thermal data is based on the JEDEC standard high-K board layout, JESD 51-7. This is a two-signal, two-plane, four-layer board with 2-oz. copper on the external layers. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

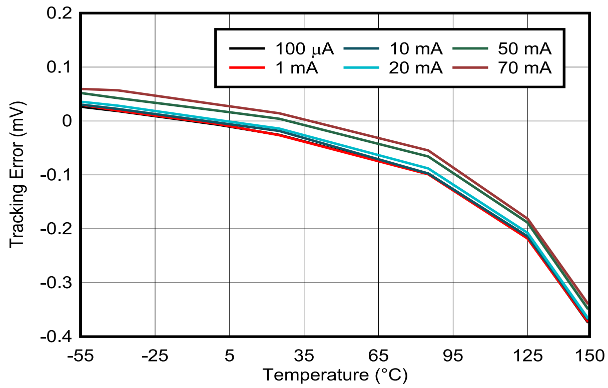
5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5 V, V_{OUT} = V_{FB}, I_{OUT} = 100 μA, C_{OUT} = 1 μF, C_{IN} = 1 μF and $V_{ADJ/EN}$ = 5 V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{IN} = 5.4 V to 40 V, $V_{ADJ/EN}$ = 5 V, I_{OUT} = 100 μA, T_J = 25ºC		50	60	μA
		V_{IN} = 5.4 V to 40 V, $V_{ADJ/EN}$ = 5 V, I_{OUT} = 100 μA, –40ºC < T_J < 85ºC			65	
		V_{IN} = 5.4 V to 40 V, $V_{ADJ/EN}$ = 5 V, I_{OUT} = 100 μA			70	
I_{GND}	Ground current	V_{IN} = 5.4 V to 40 V, $V_{ADJ/EN}$ = 5 V, I_{OUT} = 70 mA			1	mA
$I_{SHUTDOWN}$	Shutdown supply current	V_{EN} = 0 V			3.5	μA
$I_{ADJ/EN}$	ADJ/EN pin current	I_{OUT} = 100 μA to 70 mA			0.9	μA
$V_{UVLO(RISING)}$	Rising input supply UVLO	V_{IN} rising, I_{OUT} = 5 mA	2.6	2.7	2.85	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO	V_{IN} falling, I_{OUT} = 5 mA	2.3	2.4	2.5	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis			300		mV
V_{IL}	Enable logic input low level				0.8	V
V_{IH}	Enable logic input high level		1.8			V
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 400 mV to 40 V, I_{OUT} = 100 μA to 70 mA	–6		6	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 400 mV to 40 V, I_{OUT} = 100 μA	–0.4		0.4	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 400 mV, I_{OUT} = 100 μA to 70 mA [(1)]	–0.5		0.5	mV
V_{DO}	Dropout voltage	I_{OUT} = 70 mA, $V_{ADJ/EN}$ ≥ 3.3 V, V_{IN} = $V_{ADJ/EN}$		130	225	mV
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1 V, V_{OUT} short to 90% x $V_{ADJ/EN}$	85	105	125	mA
PSRR	Power-supply ripple rejection	V_{RIPPLE} = 1 V_{PP}, frequency = 100 Hz, I_{OUT} ≥ 5 mA		80		dB
V_n	Output noise voltage	V_{OUT} = 3.3 V, I_{OUT} = 1 mA, a 5 $μV_{RMS}$ reference is used for this measurement		150		$μV_{RMS}$
I_{REV}	Reverse current at V_{IN}	V_{IN} = 0 V, V_{OUT} = 32 V, $V_{ADJ/EN}$ = 5 V	–0.6		0.6	μA
I_{REV-N1}	Reverse current at negative V_{IN}	V_{IN} = –20 V, V_{OUT} = 20 V, $V_{ADJ/EN}$ = 5 V	–1.1		1.1	μA
I_{REV-N2}	Reverse current at negative V_{IN}	V_{IN} = –20 V, V_{OUT} = 0 V, $V_{ADJ/EN}$ = 5 V	–0.6		0.6	μA
I_{FB}	Feedback pin current			0.1	0.25	μA
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			15		°C

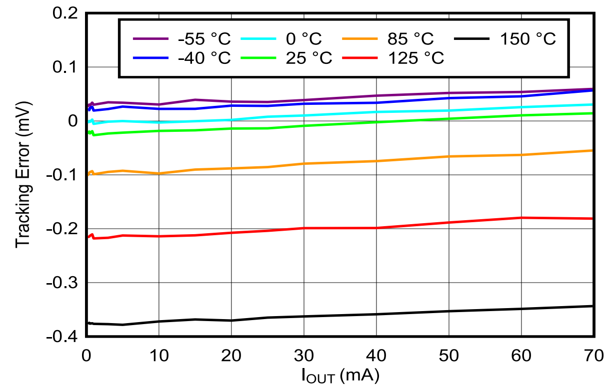
(1) Power dissipation is limited to 2 W for device production testing purposes. The power dissipation can be higher during normal operation. See the thermal dissipation section for more information on how much power the device can dissipate while maintaining a junction temperature below 150℃.

5.6 Typical Characteristics



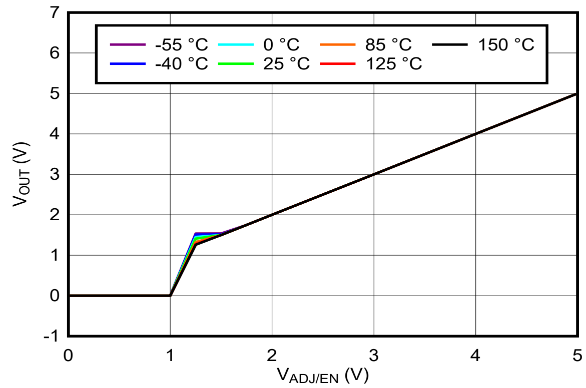
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-1. Tracking Error vs Ambient Temperature



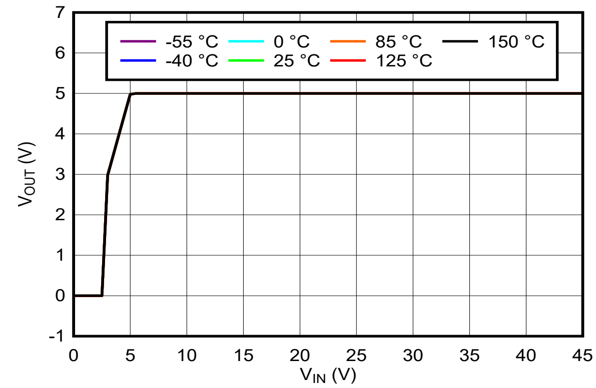
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-2. Tracking Error vs Output Current



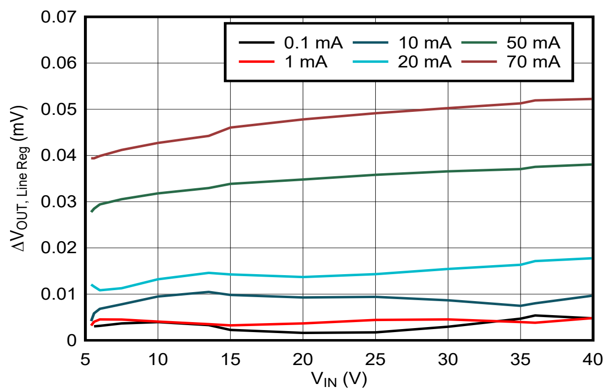
V_{IN} = 13.5 V, V_{FB} = V_{OUT}, I_{OUT} = 10 mA

图 5-3. Output Voltage vs Adjustable Reference Voltage



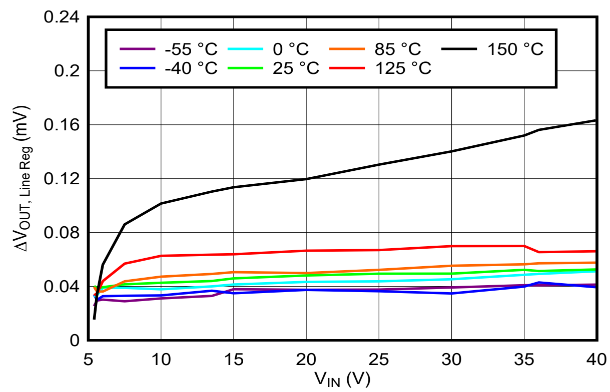
$V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, I_{OUT} = 10 mA

图 5-4. Output Voltage vs Input Voltage



$V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, T_{AMB} = 25°C

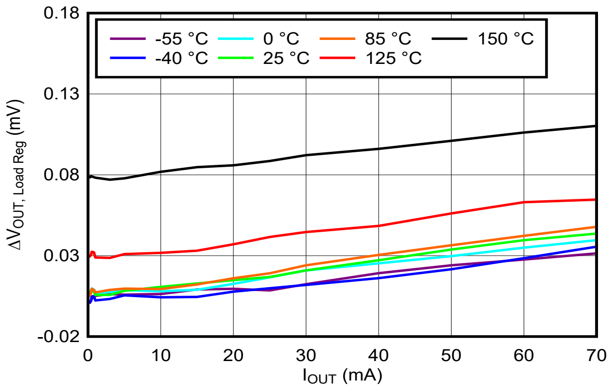
图 5-5. Line Regulation



$V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, I_{OUT} = 70 mA

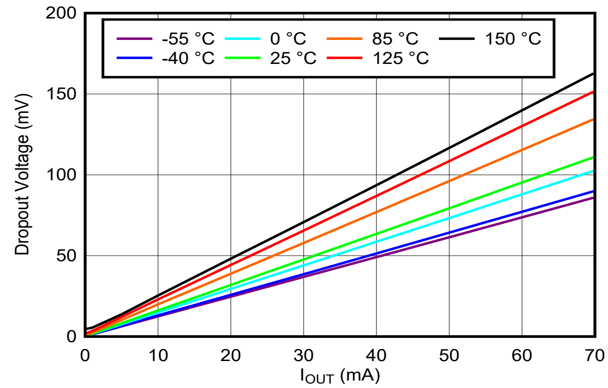
图 5-6. Line Regulation

5.6 Typical Characteristics (continued)



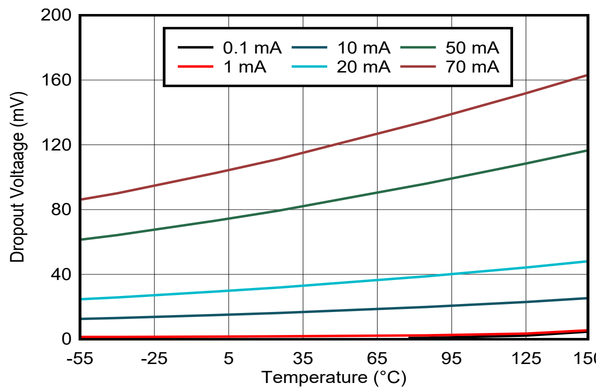
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-7. Load Regulation



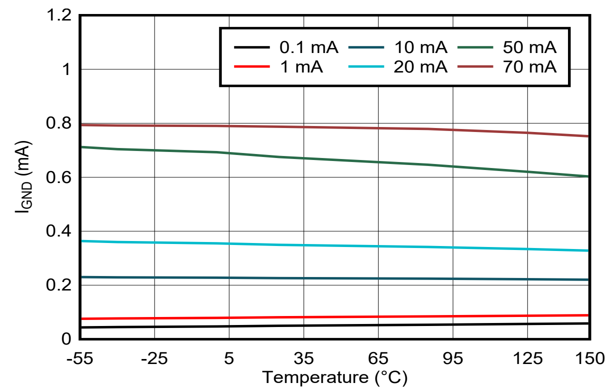
V_{IN} = 5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-8. Dropout Voltage vs Load Current



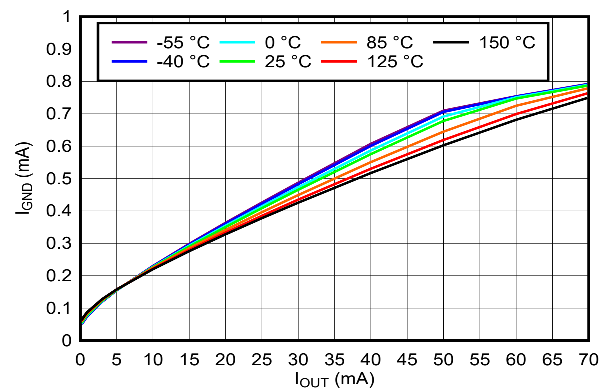
V_{IN} = 5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-9. Dropout Voltage vs Ambient Temperature



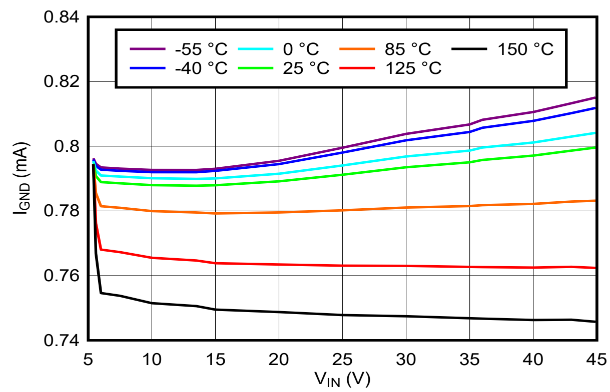
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-10. Ground Current vs Ambient Temperature



V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

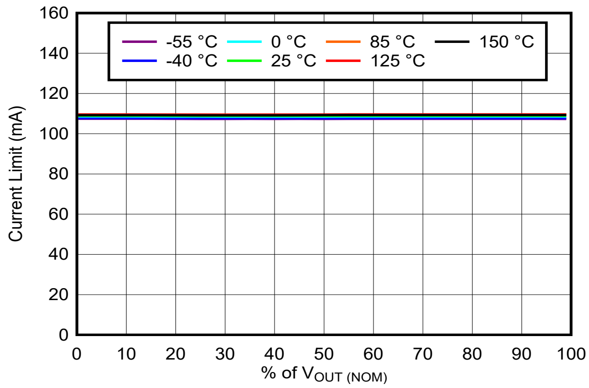
图 5-11. Ground Current vs Output Current



$V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, I_{OUT} = 70 mA

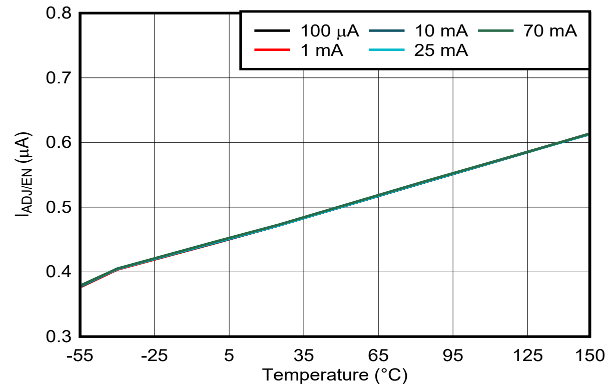
图 5-12. Ground Current vs Input Voltage

5.6 Typical Characteristics (continued)



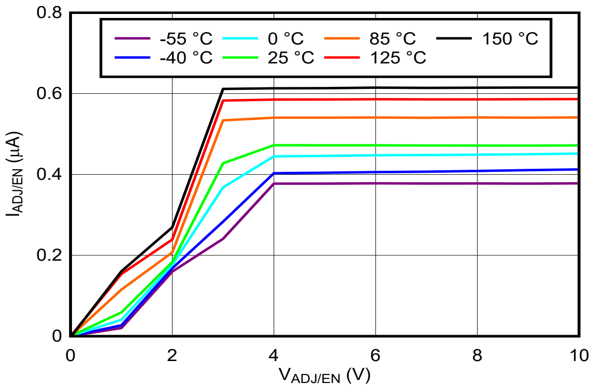
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-13. Current Limit vs Output Voltage



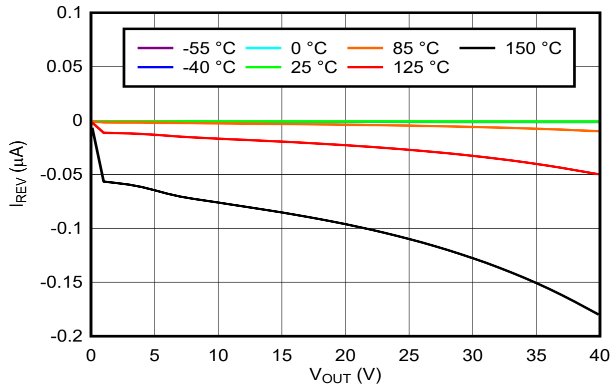
V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-14. Adjustable Pin Current vs Ambient Temperature



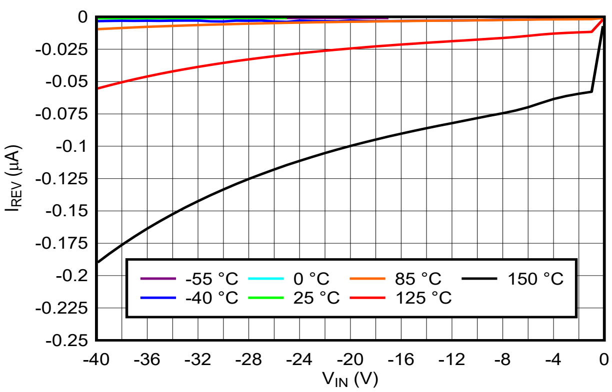
V_{IN} = 13.5 V, V_{FB} = V_{OUT}, I_{OUT} = 70 mA

图 5-15. Adjustable Pin Current vs Adjustable Pin Voltage



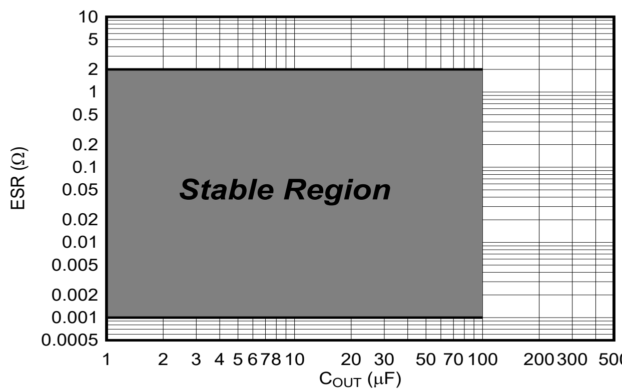
V_{IN} = 0 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

图 5-16. Reverse Current vs Output Voltage



V_{OUT} = 0 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}

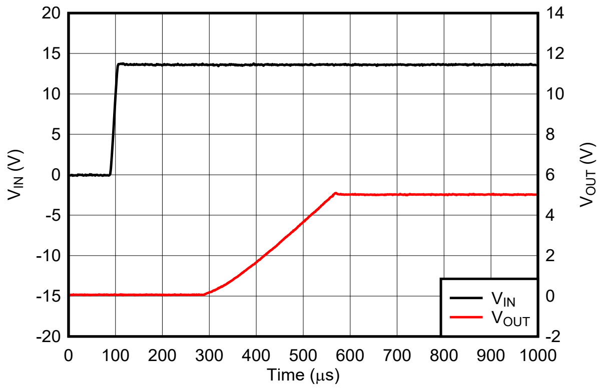
图 5-17. Reverse Current vs Input Voltage



Stable region = 1 mΩ ≤ ESR ≤ 2 Ω, 1 µF ≤ C_{OUT} ≤ 100 µF

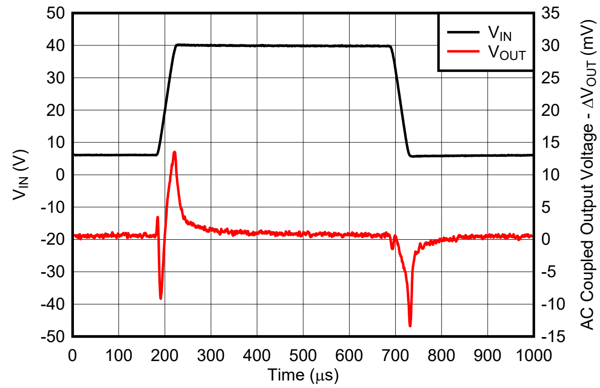
图 5-18. ESR vs Load Capacitance

5.6 Typical Characteristics (continued)



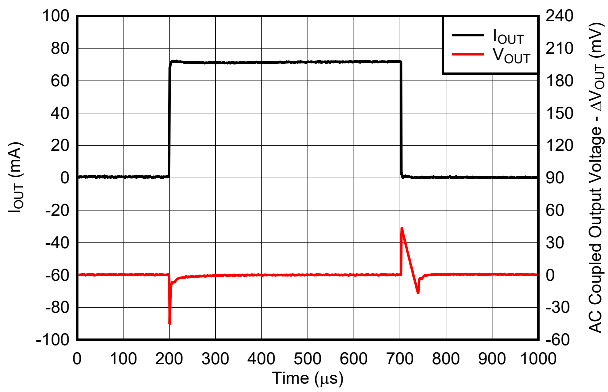
V_{IN} = 0 V to 13.5 V at a rate of 1 V/µs , $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, C_{OUT} = 1 µF, I_{OUT} = 70 mA

图 5-19. Start-Up Profile



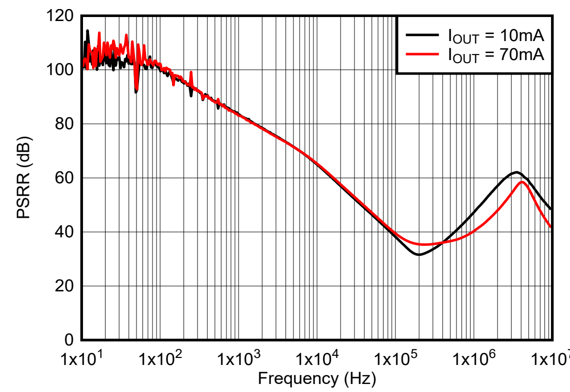
V_{IN} = 6 V to 40 V at a rate of 1 V/µs , $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, C_{OUT} = 1 µF, I_{OUT} = 70 mA

图 5-20. Line Transient



V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, C_{OUT} = 1 µF, I_{OUT} = 1 mA to 70 mA at a rate of 1 A/µs

图 5-21. Load Transient



V_{IN} = 13.5 V, $V_{ADJ/EN}$ = 5 V, V_{FB} = V_{OUT}, C_{OUT} = 1 µF

图 5-22. PSRR vs Frequency

6 Detailed Description

6.1 Overview

The TPS7B4256-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering off-board sensors, multiple features are built into the LDO to protect against fault conditions resulting in short to battery, short to GND, and reverse current protection.

In addition, this device also features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), and reverse polarity protection.

6.2 Functional Block Diagram

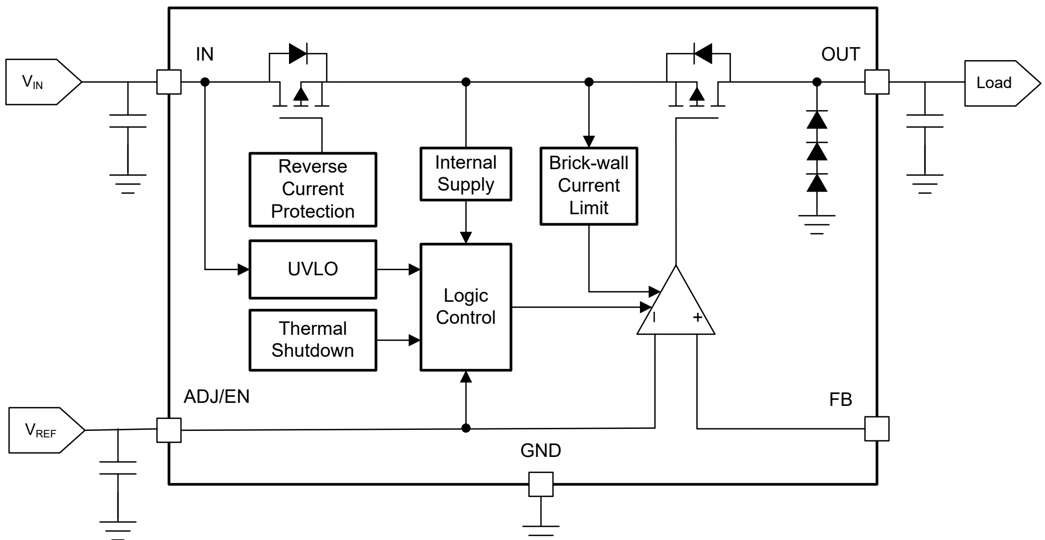


图 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Tracker Output Voltage (V_{OUT})

Because this device is a tracking LDO, the output voltage is determined by the voltage provided to the ADJ/EN pin. The LDO remains disabled as long as $V_{ADJ/EN}$ is less than V_{IL}. When $V_{ADJ/EN}$ exceeds V_{IH}, the output voltage V_{OUT} begins to rise. The device has a soft-start feature incorporated, which allows the output voltage to rise linearly and limits the in-rush current at start-up. After start-up and upon attaining steady state, the feedback pin voltage V_{FB} remains within ±6 mV from the voltage set on the ADJ/EN pin over all specified operating conditions.

6.3.1.1 Output Voltage Equal to Reference Voltage

As shown in 图 6-2, with the external reference voltage applied directly to the ADJ/EN pin and the FB pin connected to the OUT pin, the LDO output voltage is equal to the reference voltage, as given in 方程式 1.

$$V_{OUT} = V_{REF} \quad (1)$$

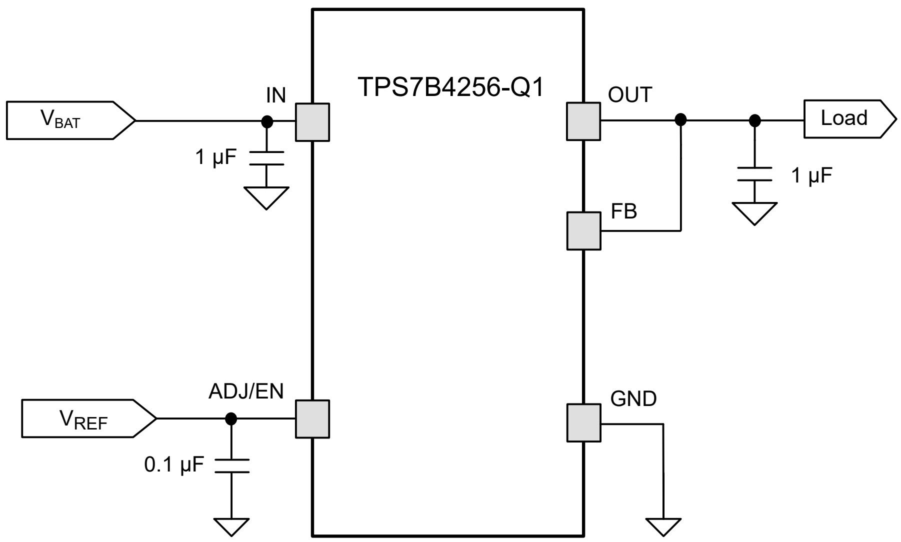


图 6-2. Tracker Output Voltage equal to Reference Voltage

6.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ/EN pin, as shown in 图 6-3, can help generate an output voltage that is lower than the reference voltage. Both R_1 and R_2 must be less than 100 kΩ to minimize the error in voltage caused by the ADJ/EN pin leakage current, $I_{ADJ/EN}$. 方程式 2 calculates V_{OUT}.

$$V_{OUT} = \frac{(V_{REF} \times R_2)}{R_1 + R_2} \quad (2)$$

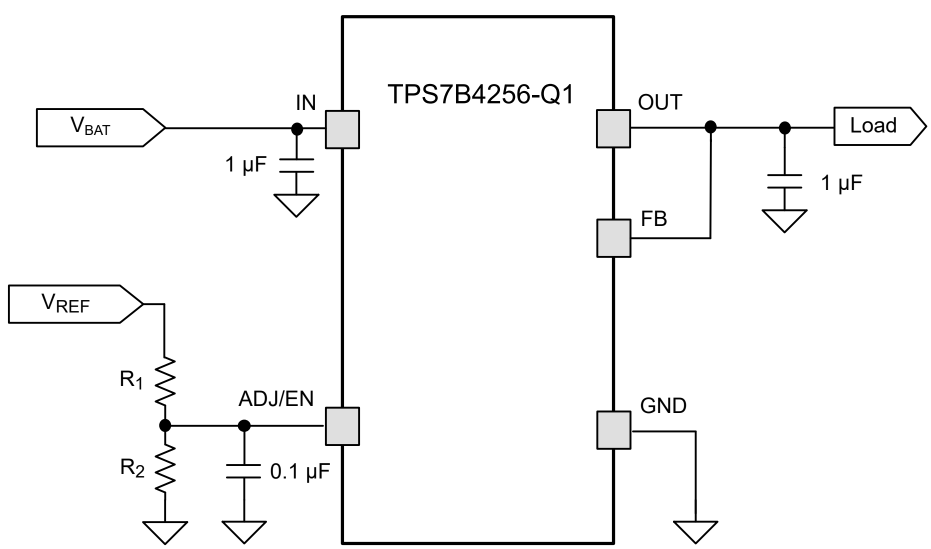


图 6-3. Tracker Output Voltage Lower Than the Reference Voltage

6.3.1.3 Output Voltage Larger Than the Reference Voltage

Connecting an external resistor divider between the OUT and FB pin, as shown in 图 6-4, can help generate an output voltage that is higher than the reference voltage. Both R_1 and R_2 must be less than 100 kΩ to minimize the error in voltage caused by the FB pin leakage current, I_{FB}. 方程式 3 calculates V_{OUT}.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

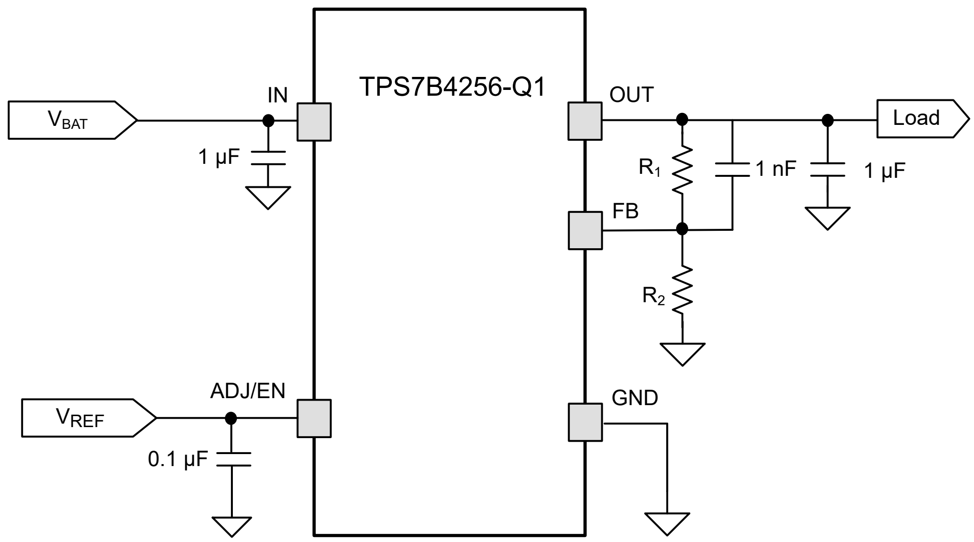


图 6-4. Tracker Output Voltage Higher Than the Reference Voltage

6.3.2 Reverse Current Protection

The TPS7B4256-Q1 incorporates a back-to-back PMOS topology that protects the device from damage against a fault condition, resulting in V_{OUT} being higher than V_{IN} and the subsequent flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the *Absolute Maximum Ratings* are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 1 µs, and along with the body diode of the blocking PMOS transistor, limits the reverse current to I_{REV}.

6.3.3 Undervoltage Lockout

The device has an internally fixed undervoltage lockout (UVLO) threshold. Undervoltage lockout activates when the input voltage V_{IN} drops below the undervoltage lockout level (see the $V_{UVLO(FALLING)}$ parameter in the *Electrical Characteristics* table). This activation makes sure that the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the *Electrical Characteristics* table).

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Although the device can enable at such high temperatures, the device parameters and performance are specified up to a junction temperature of 150°C. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the condition that causes excessive power dissipation is removed. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4256-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4256-Q1 into thermal shutdown degrades device reliability.

6.3.5 Current Limit

The device has an internal current limit circuit to protect the device during overcurrent or shorting conditions. The current-limit circuit, as shown in 图 6-5, is a brick-wall scheme. When the device is in current limit, the device sources I_{CL} and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

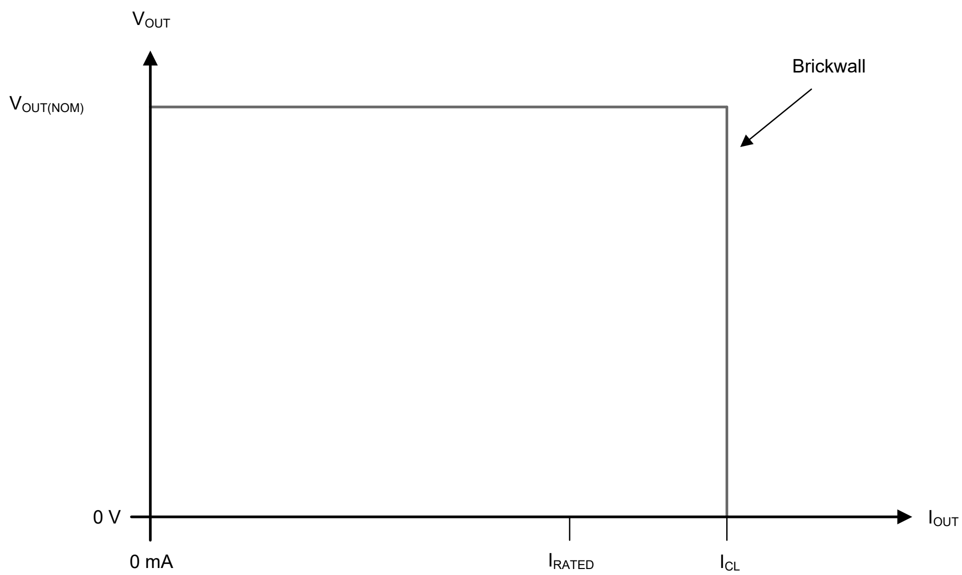


图 6-5. Current Limit: Brick-Wall Scheme

During a current-limit event, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage (V_{IN} – V_{OUT}). If the device heats enough, the device can enter thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device can enter thermal shutdown again and continue this cycle until the current-limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

6.3.6 Output Short to Battery

When the output is shorted to the battery (see 图 6-6), the TPS7B4256-Q1 survives and no damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply (see 图 6-7) at a lower voltage. In this case, the TPS7B4256-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V_{OUT}, which typically runs at 5 V. The back-to-back PMOS topology helps limit the continuous reverse current flowing through V_{IN} to I_{REV}, as provided in the *Electrical Characteristics* table.

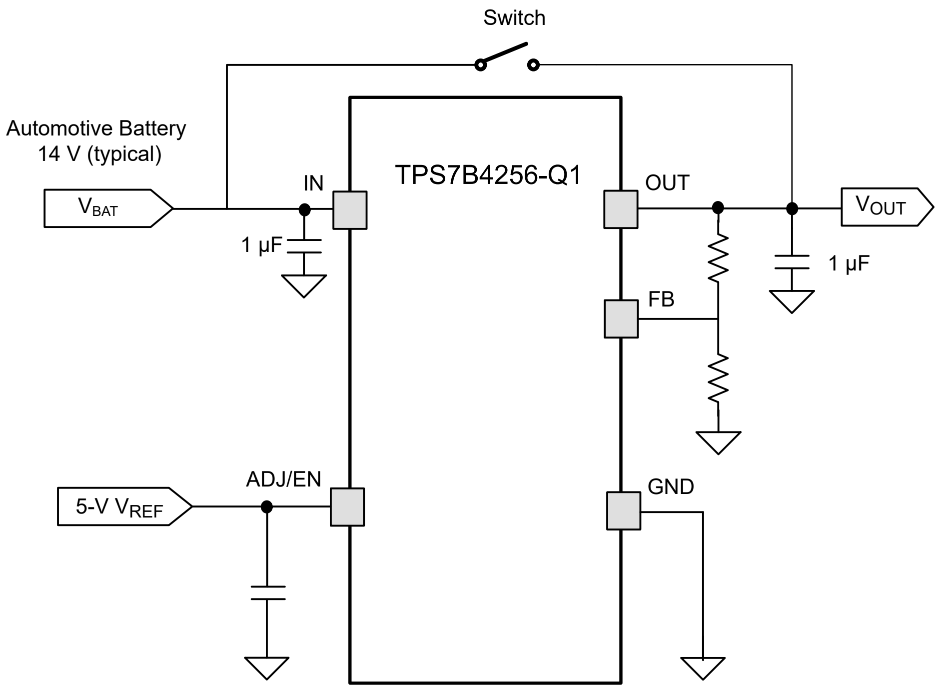


图 6-6. Output Voltage Short to Battery

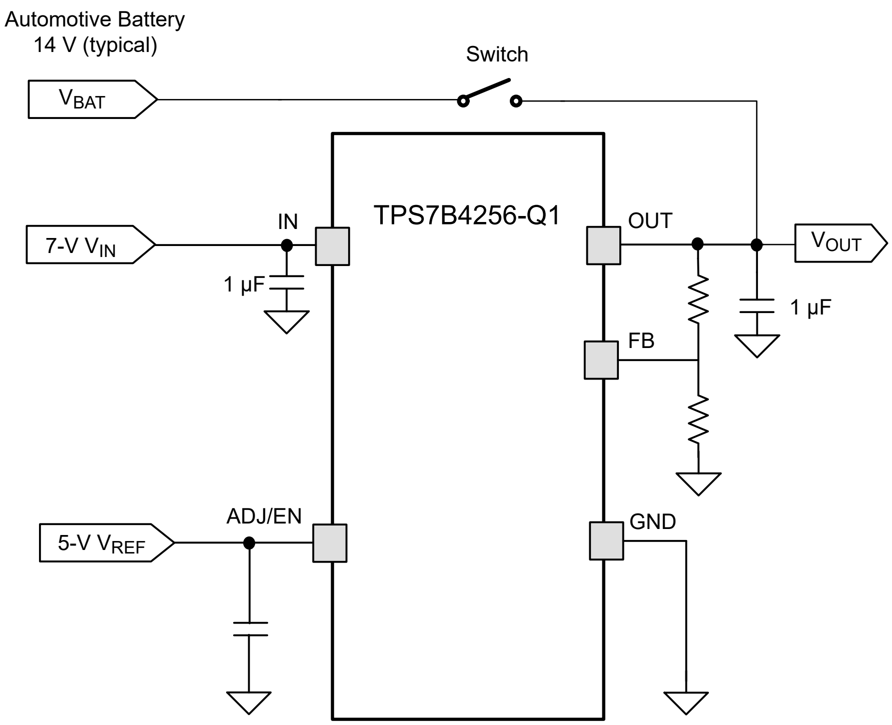


图 6-7. Output Voltage Higher Than the Input

6.3.7 Tracking Regulator With an Enable Circuit

By pulling the reference voltage below V_{IL}, the device disables and enters a sleep state where the device draws 3.5 μA (max) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur. The device can be configured as shown in 图 6-8 in this case. The TPS7B84-Q1 is a 150-mA LDO with ultra-low quiescent current that provides the reference voltage to both the TPS7B4256-Q1 and the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output (I/O).

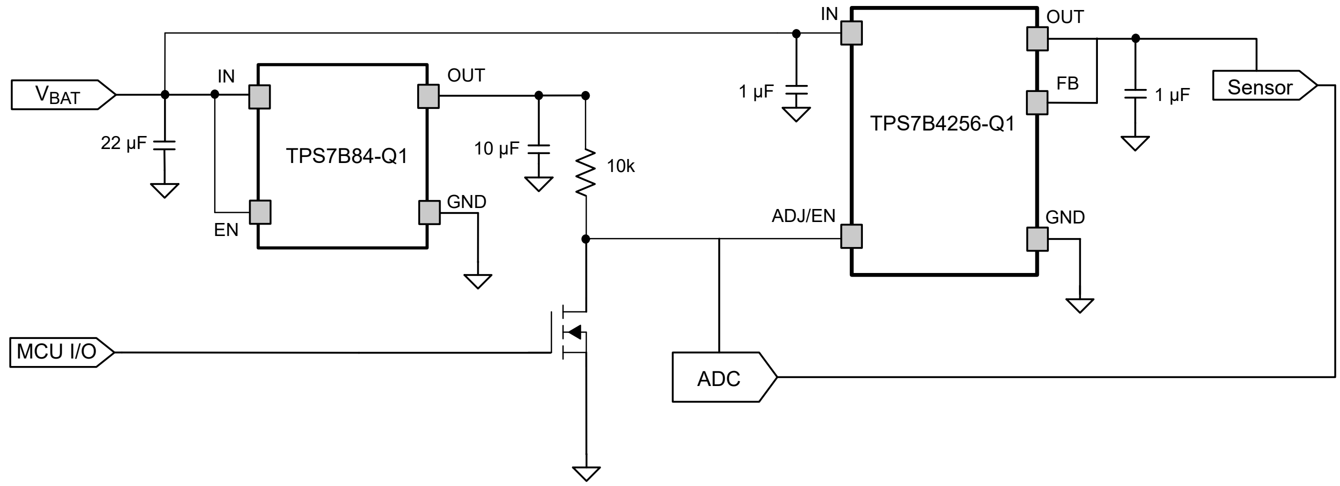


图 6-8. Tracking an LDO With an Enable Circuit

6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER(1)			
	V_{IN}	$V_{ADJ/EN}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(Nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ADJ/EN} < V_{IL}$	Not applicable	$T_J > T_{SD(shutdown)}$

(1) The device turns on when V_{IN} is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than the enable rising threshold V_{IH}.

6.4.1 Normal Operation

The device output voltage $V_{OUT(Nom)}$ tracks the reference voltage at the ADJ/EN pin when the following conditions are met:

- The input voltage is at least 3 V ($V_{IN(min)}$) and greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The reference voltage at the ADJ/EN pin is greater than the enable rising threshold V_{IH} and stays stable at the appropriate V_{REF} value
- The output current is less than $I_{OUT(max)}$ ($I_{OUT} \leq 70$ mA)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the saturation region.

6.4.3 Operation With V_{IN} < 3 V

For input voltages below 3 V and above $V_{UVLO(FALLING)}$, the LDO continues to operate but certain internal circuits can possibly not have the proper headroom to operate within specification. When the input voltage drops below $V_{UVLO(FALLING)}$ the device shuts off.

6.4.4 Disable With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. The output of the device can be shutdown by forcing $V_{ADJ/EN}$ less than V_{IL}. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) when the pass transistor is fully on. This condition arises when the input voltage falls to the point where the error amplifier must drive the gate of the pass transistor to the rail and has no remaining headroom for the control loop to operate. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage directly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage (V_{DO}).

In dropout mode, the output voltage is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients can cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current (I_{RATED}, see the *Recommended Operating Conditions* table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS\ (ON)} = \frac{V_{DO}}{I_{RATED}} \tag{4}$$

7.1.2 Reverse Current

The TPS7B4256-Q1 incorporates reverse current protection that prevents damage from a fault condition, resulting in V_{OUT} being higher than V_{IN}. During such a fault condition, where the V_{IN} and V_{OUT} absolute maximum ratings are not violated and V_{OUT} – V_{IN} is less than 40 V, no damage occurs and less than 1.1 µA of reverse current flows through the LDO. The reverse current comparator typically responds to a reverse voltage condition and, along with the body diode of the blocking PMOS transistor, limits the reverse current in 1 µs.

7.2 Typical Application

图 7-1 shows a typical application circuit for the TPS7B4256-Q1.

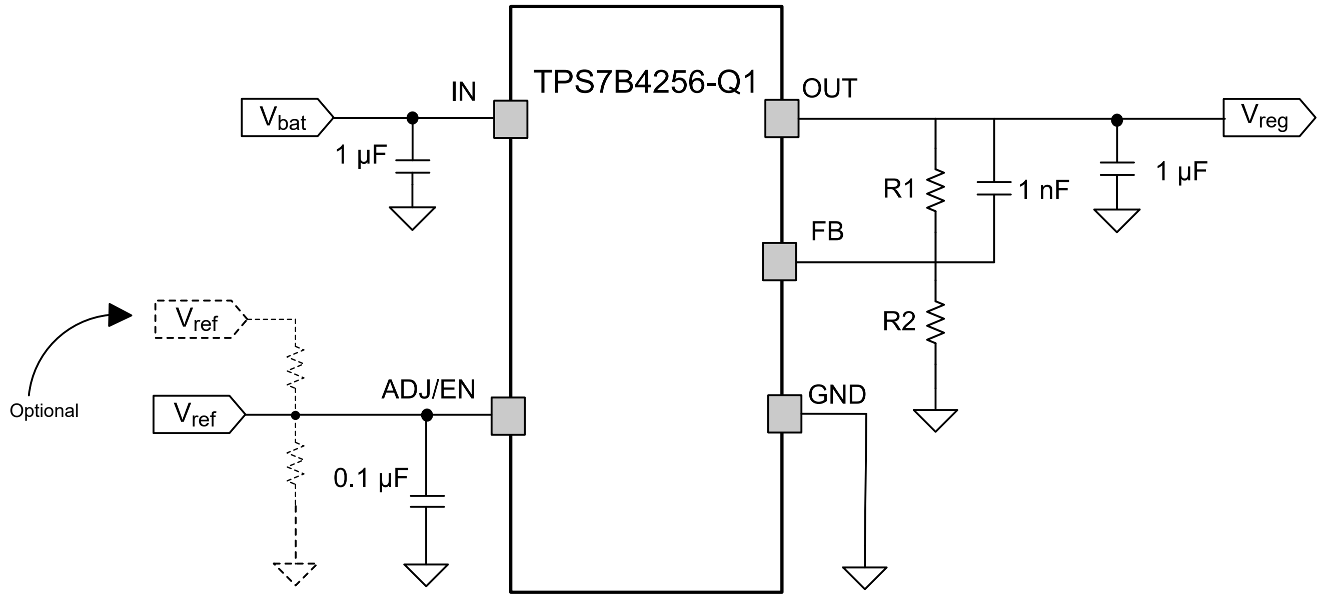


图 7-1. Typical Application Schematic

7.2.1 Design Requirements

Use the parameters listed in 表 7-1 for this design example.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3 V to 40 V
ADJ/EN reference voltage	2 V to 40 V
Output voltage	2 V to 40 V
Output current rating	70 mA
Output capacitor range	1 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Selection

Depending on the end application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4256-Q1 requires an output capacitor of at least 1 µF (500 nF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001 Ω and 2 Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100 µF.

An input capacitor is not required for stability, however, good analog practice is to connect a capacitor (500 nF or higher) between the GND and IN pin of the TPS7B4256-Q1. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.2.2 Feedback Resistor Selection

V_{OUT} is set by the voltage at the ADJ/EN pin and the external feedback resistors R_1 and R_2 according to the following equation:

$$V_{OUT} = V_{ADJ/EN} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (6)$$

7.2.2.3 Feedforward Capacitor

A feedforward capacitor (C_{FF}) is recommended to be connected between the OUT pin and the FB pin. C_{FF} improves transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

As shown in 图 7-2, poor layout practices and using long traces at the FB pin results in the formation of a parasitic capacitor (C_{FB}).

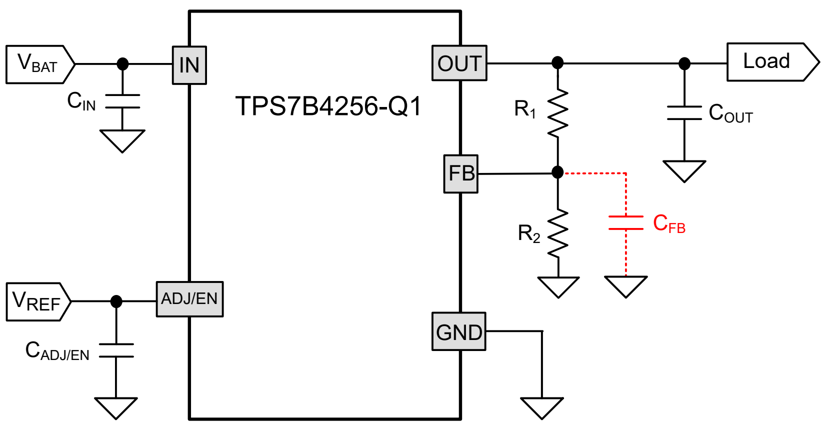


图 7-2. Formation of Parasitic Capacitor at the FB Pin

C_{FB}, along with the feedback resistors R_1 and R_2 can result in the formation of an uncompensated pole in the transfer function of the loop gain. A C_{FB} value as small as 7 pF can cause the parasitic pole frequency, given by 方程式 7, to fall within the bandwidth of the LDO and result in instability.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (7)$$

Adding a feedforward capacitor (C_{FF}), as shown in 图 7-3, creates a zero in the loop gain transfer function that can compensate for the parasitic pole created by C_{FB}. 方程式 8 and 方程式 9 calculate the pole and zero frequencies.

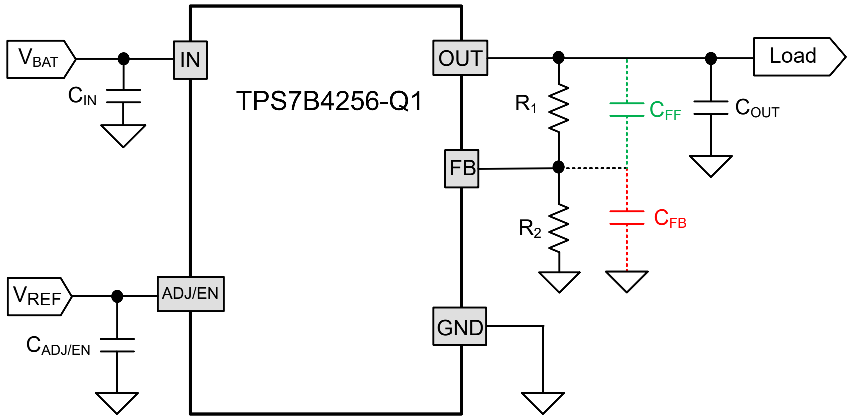


图 7-3. Feedforward Capacitor Can Compensate the Effects of the Parasitic Capacitor

$$f_P = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \tag{8}$$

$$f_Z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \tag{9}$$

The C_{FF} value that makes f_P equal to f_Z, and result in a pole-zero cancellation, depends on the values of C_{FB} and the feedback resistors used in the application. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies given by 方程式 8 and 方程式 9 are related as:

$$\frac{f_P}{f_Z} \approx \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{ADJ/EN}} \tag{10}$$

In most applications, particularly where a 3.3-V or 5-V V_{OUT} is generated, this ratio is not very large, implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. Even for large V_{OUT} values, where this ratio can be as large as 20, a C_{FF} value in the range 100 pF ≤ C_{FF} ≤ 10 nF typically helps prevent instability caused by the parasitic capacitance on the feedback node.

Following good layout practices, as described in the *Layout Guidelines* section and in the *TRKRLDOEVM-119 General-Purpose Tracker LDO Evaluation Module* user guide, helps minimize the parasitic feedback pin capacitance to values that prevent the resulting parasitic pole from causing instability.

7.2.3 Application Curves

The following images illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness for the SOIC-8 (D) and HSOIC-8 (DDA) packages. These plots are generated with a 101.6-mm × 101.6-mm × 1.6-mm PCB of two and four layers. For the 2-layer board, the bottom layer is a ground plane of constant size, and the top layer copper is connected to GND and varied. For the 4-layer board, the second layer is a ground plane of constant size, the third layer is a power plane of constant size, and the top and bottom layers copper fills are connected to GND and varied at the same rate. For the 4-layer board, inner planes use 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 3 × 3 array of thermal vias with a 300-µm drill diameter and 25-µm copper plating is located underneath the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. *PowerPAD™ Thermally Enhanced Package* application note discusses the impact that thermal vias have on thermal performance.

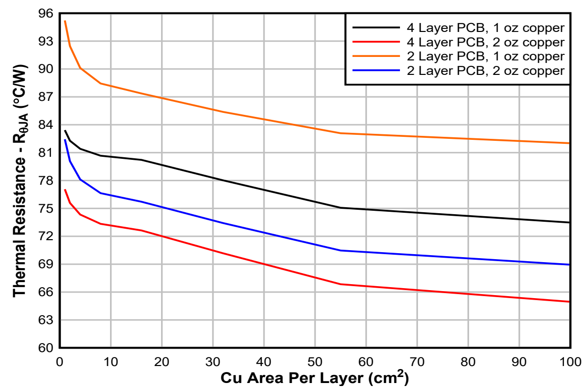


图 7-4. $R_{\theta JA}$ vs Copper Area (SOIC-8 Package)

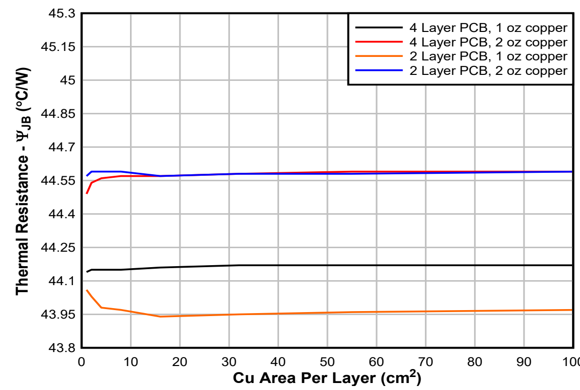


图 7-5. ψ_{JB} vs Copper Area (SOIC-8 Package)

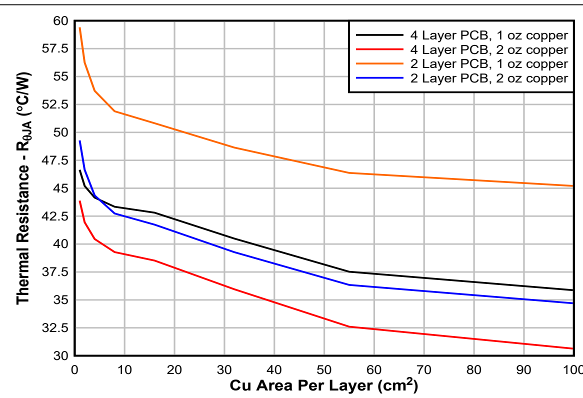


图 7-6. $R_{\theta JA}$ vs Copper Area (HSOIC-8 Package)

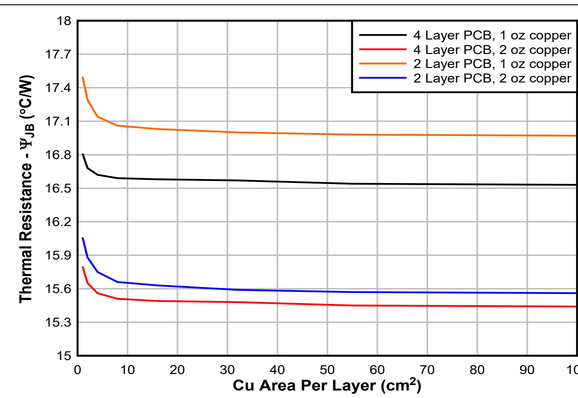


图 7-7. ψ_{JB} vs Copper Area (HSOIC-8 Package)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4256-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and provide stability. Every capacitor must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to provide the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7B4256-Q1 evaluation board, available at www.ti.com.

7.4.1.3 Power Dissipation and Thermal Considerations

方程式 11 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \tag{11}$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT}, the term $I_Q \times V_{IN}$ in 方程式 11 can be ignored.

Calculate the junction temperature (T_J) with 方程式 12 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{12}$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

方程式 13 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \tag{13}$$

The maximum ambient air temperature (T_{AMAX}) at which the device can operate can be calculated with 方程式 14 for a given maximum junction temperature (T_{JMAX}).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \tag{14}$$

7.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (图 7-8), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

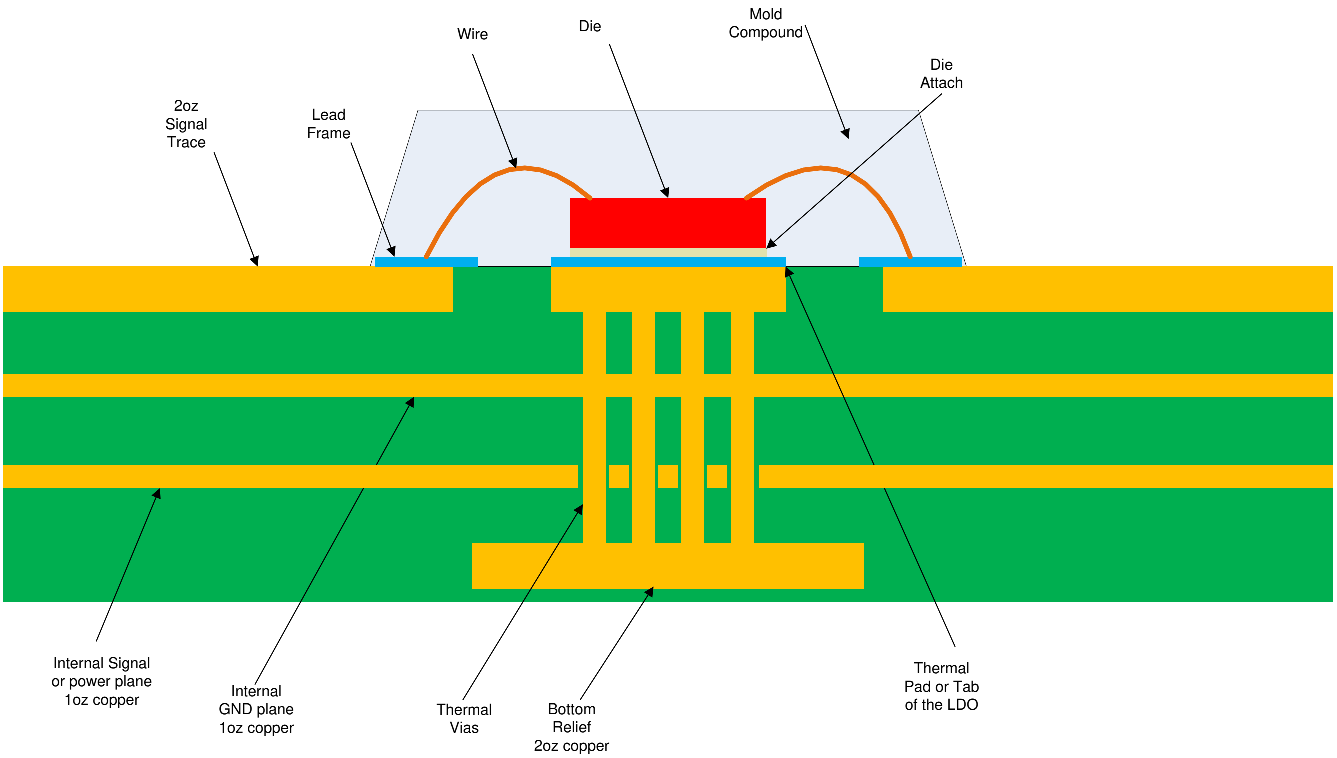
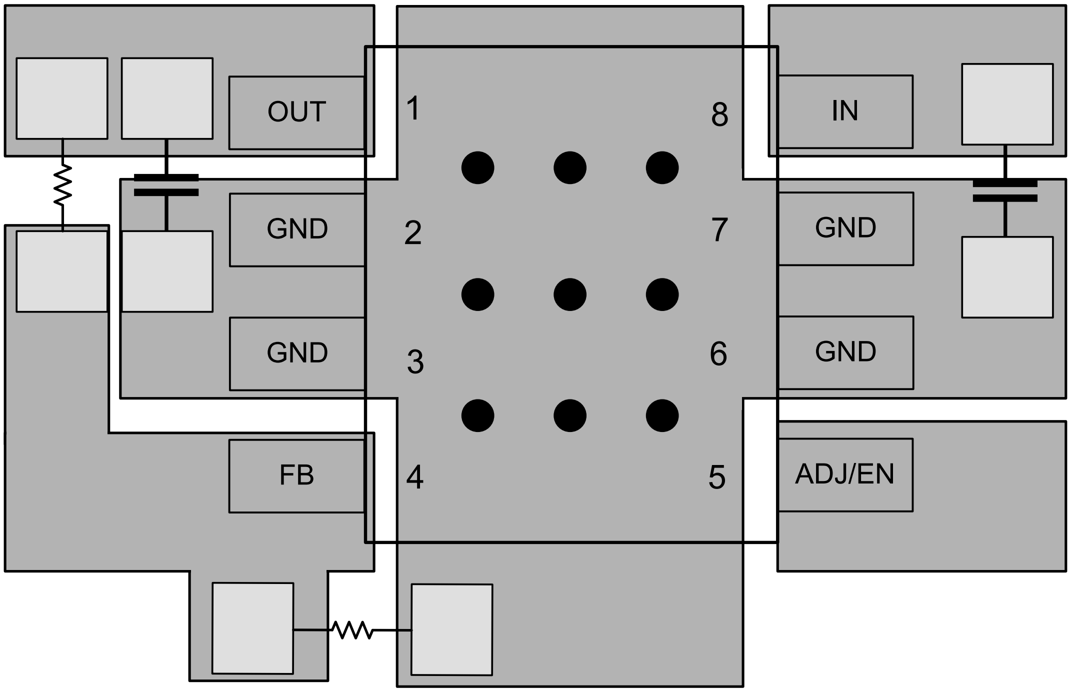


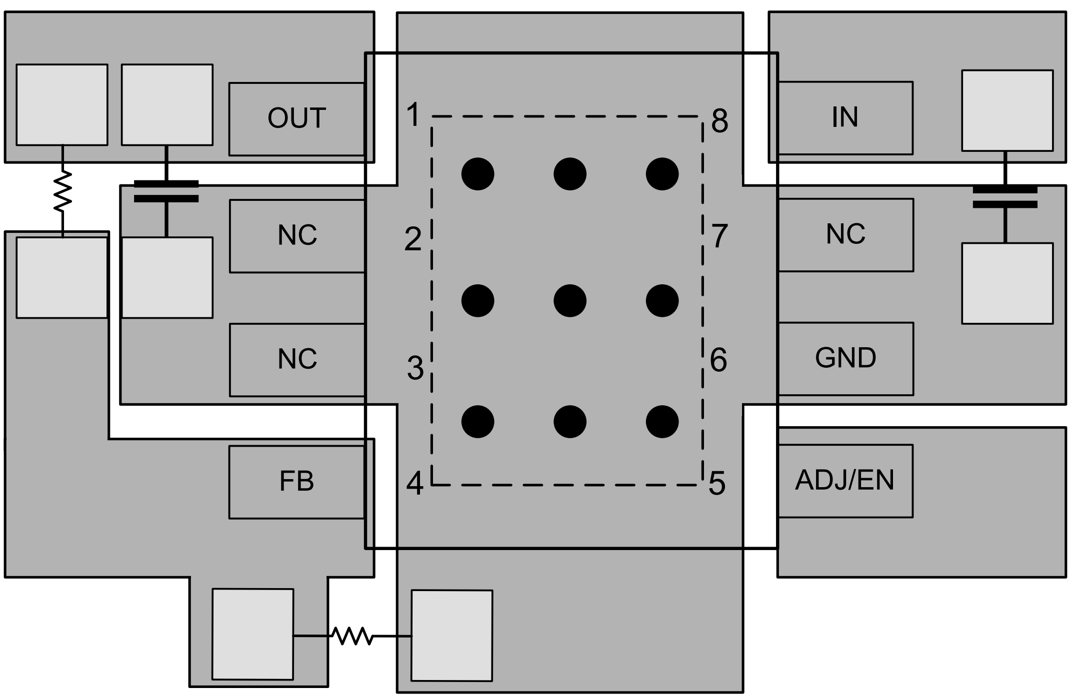
图 7-8. JEDEC Standard 2s2p PCB

7.4.1.5 Layout Examples



● Circles denote PCB via connections

图 7-9. D Package Layout Example



● Circles denote PCB via connections

图 7-10. DDA Package Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7B4256**Q DDAR Q1**	In the HSOIC (DDA) package: **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **R** is the packaging quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.
TPS7B4256**Q DR Q1**	In the SOIC (D) package: **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **R** is the packaging quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2023) to Revision A (November 2023) **Page**

- 将文档状态从*预告信息* 更改为*量产数据* 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4256QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B4256F	Samples
TPS7B4256QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B4256E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

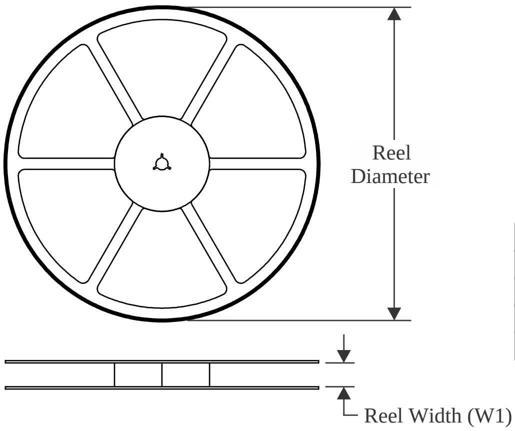
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

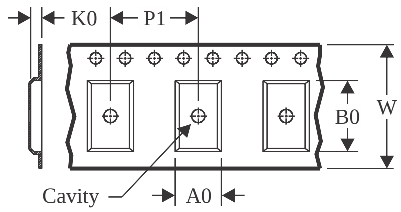
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

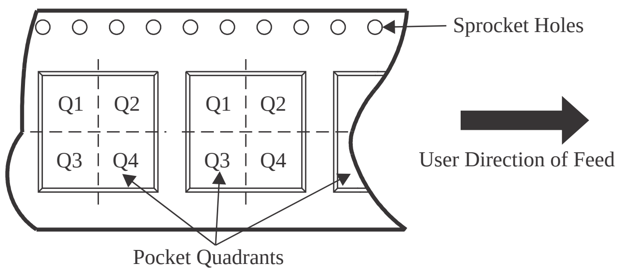


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

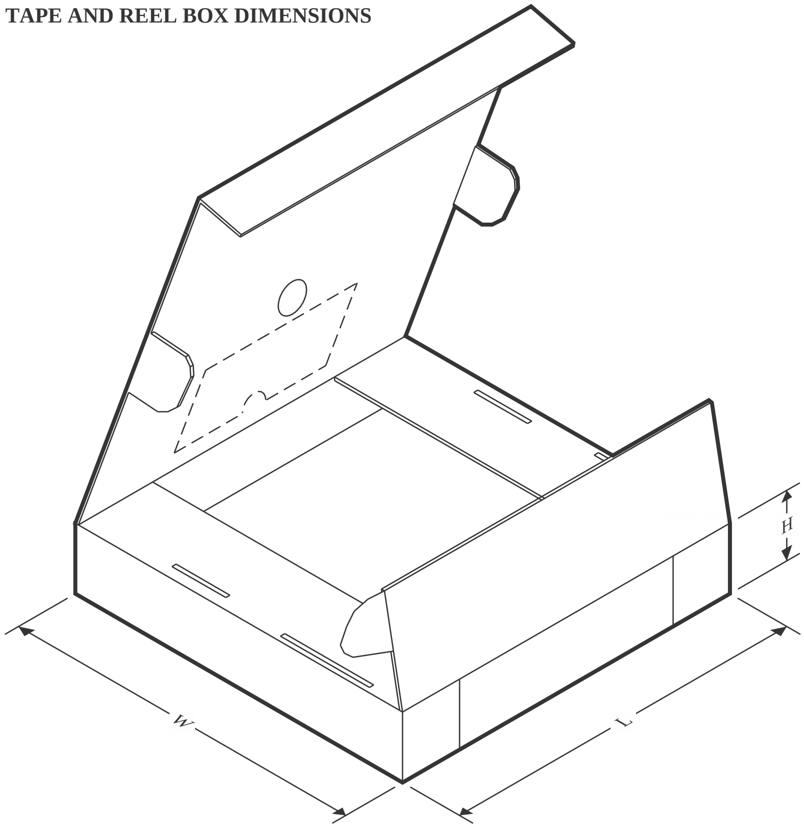
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

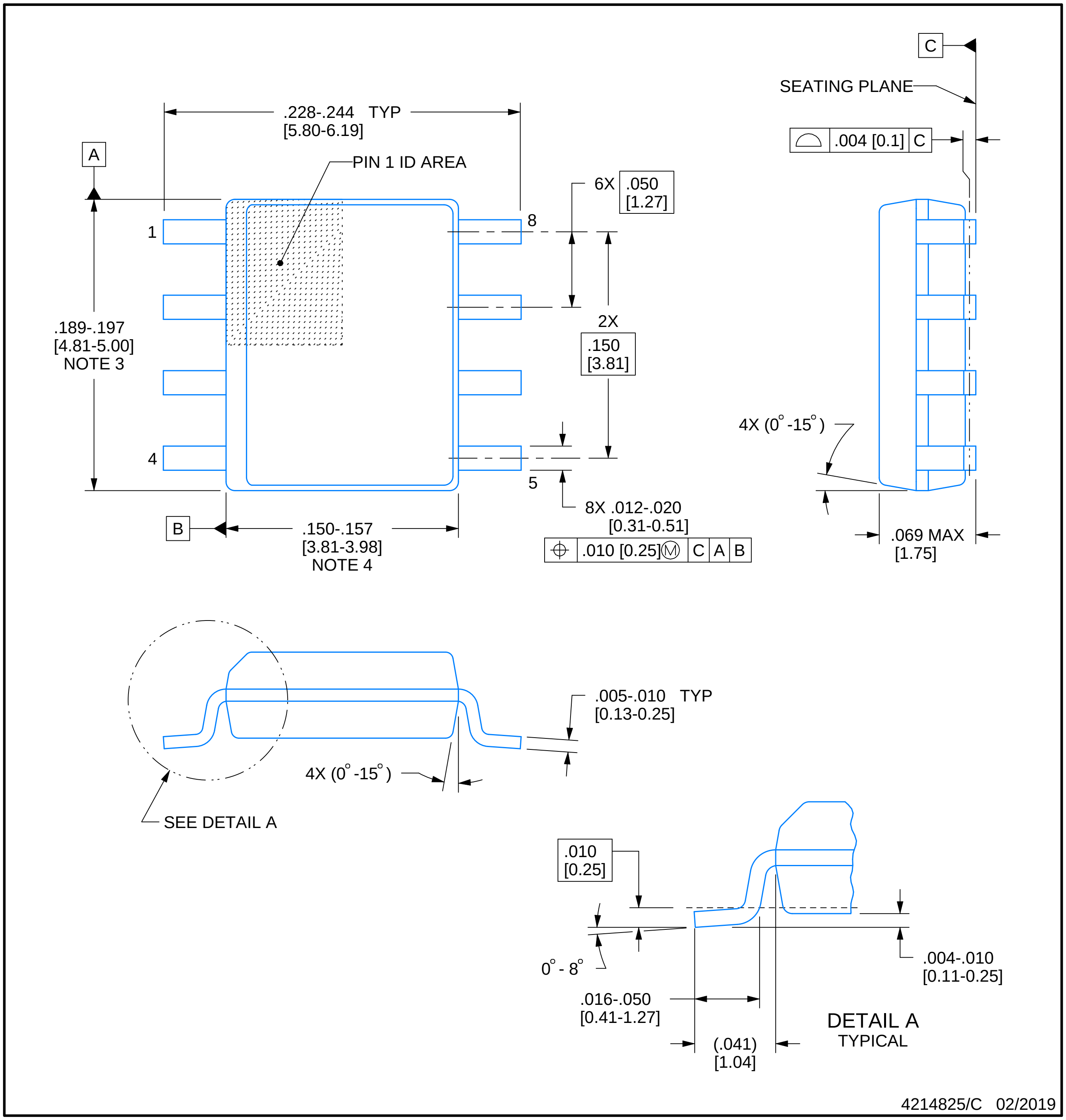
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4256QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B4256QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



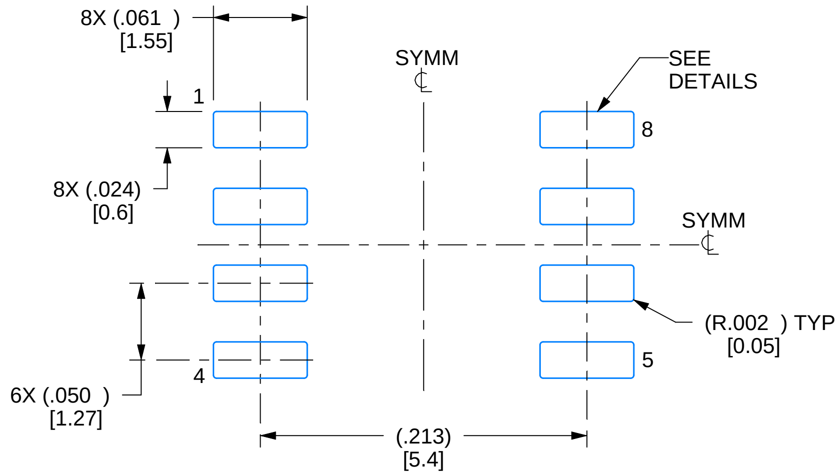
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4256QDDARQ1	SO PowerPAD	DDA	8	2500	353.0	353.0	32.0
TPS7B4256QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

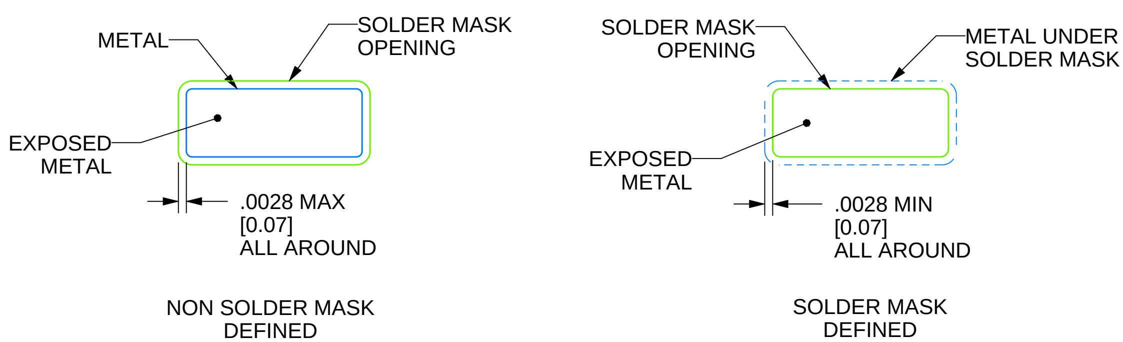


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

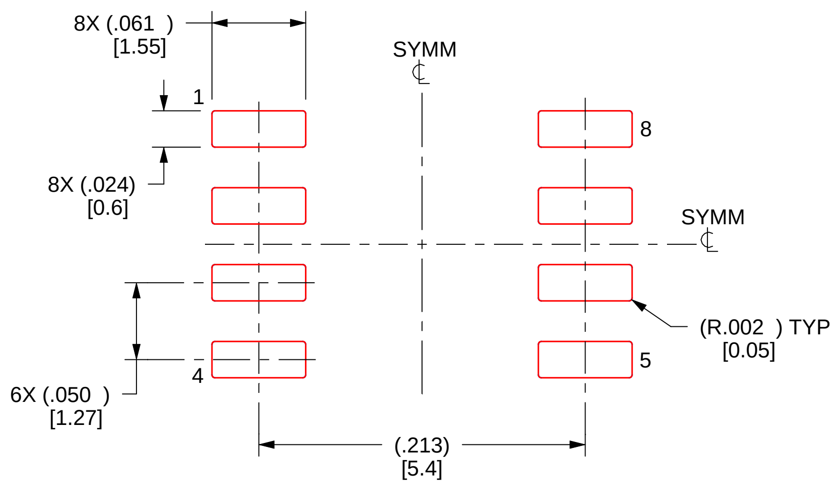


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

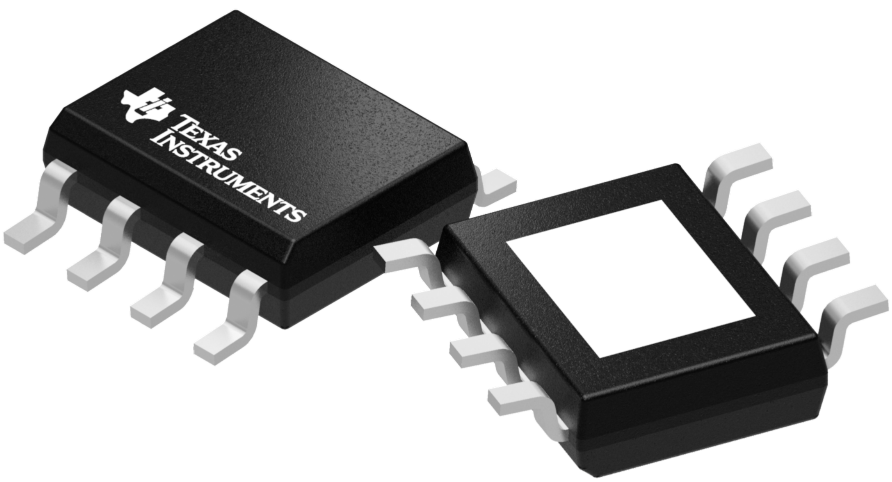


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

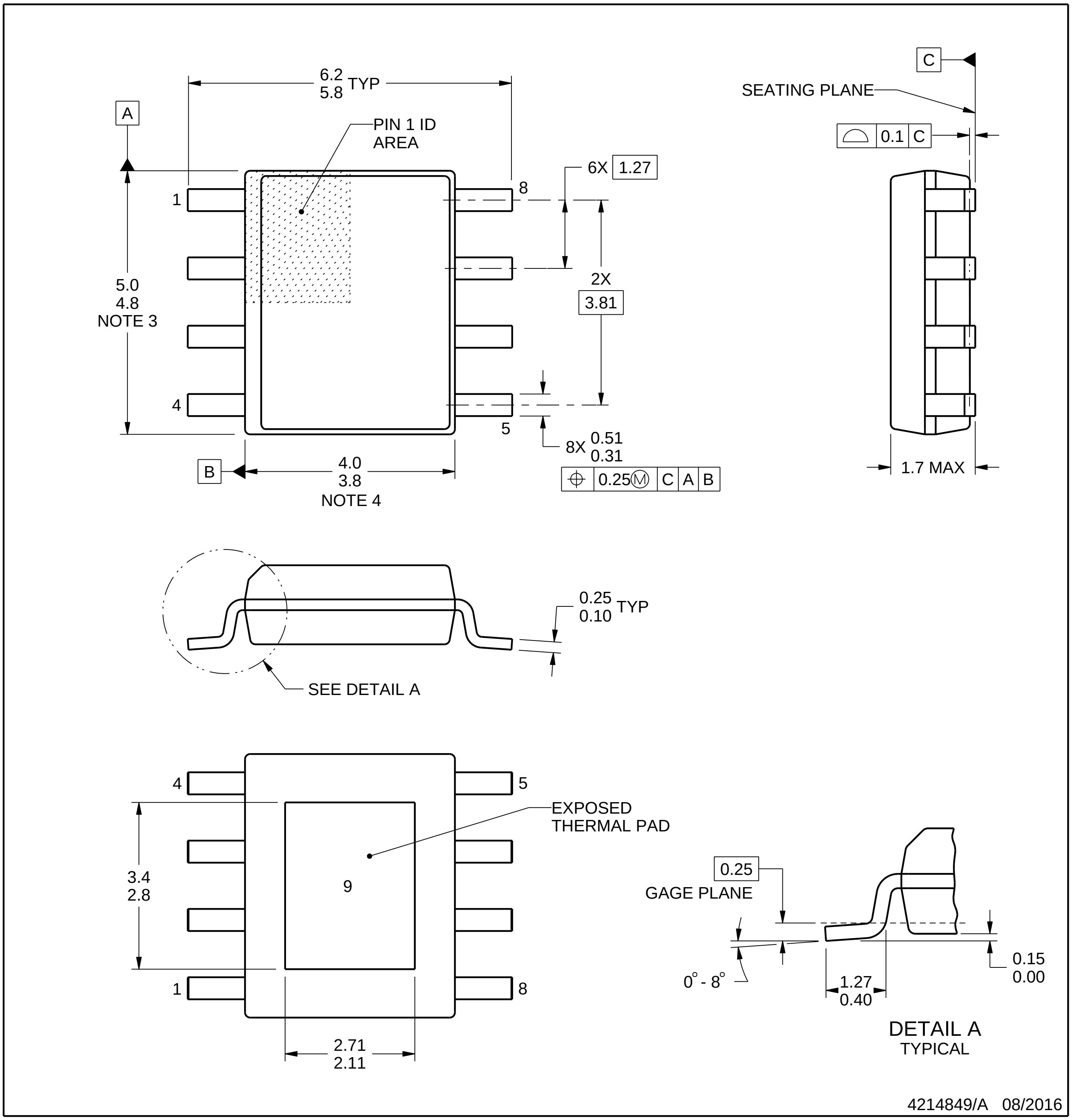


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

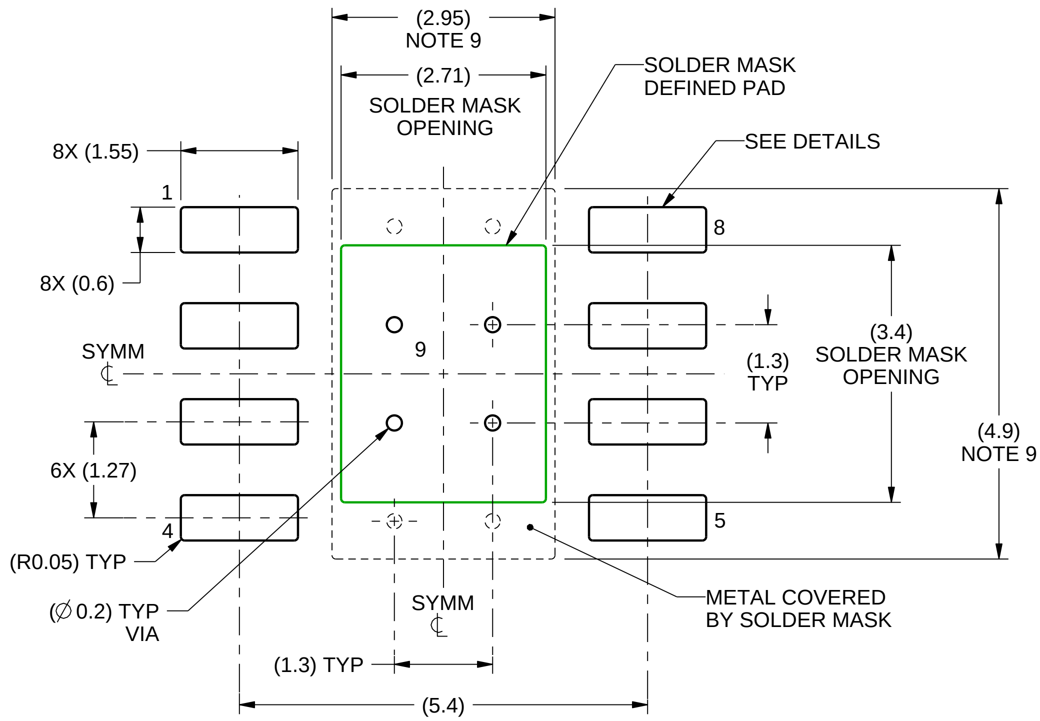
PLASTIC SMALL OUTLINE



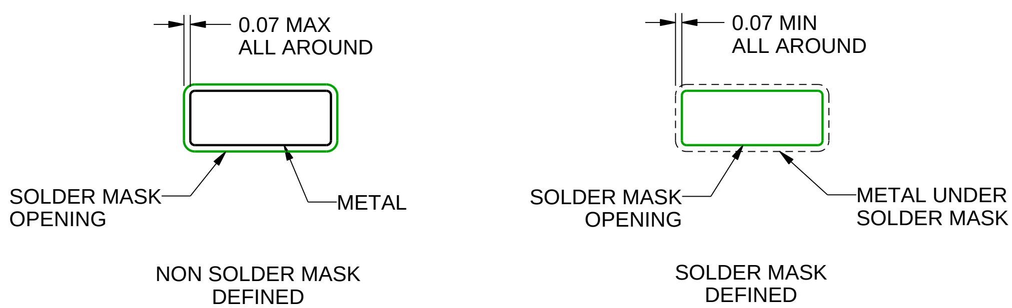
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

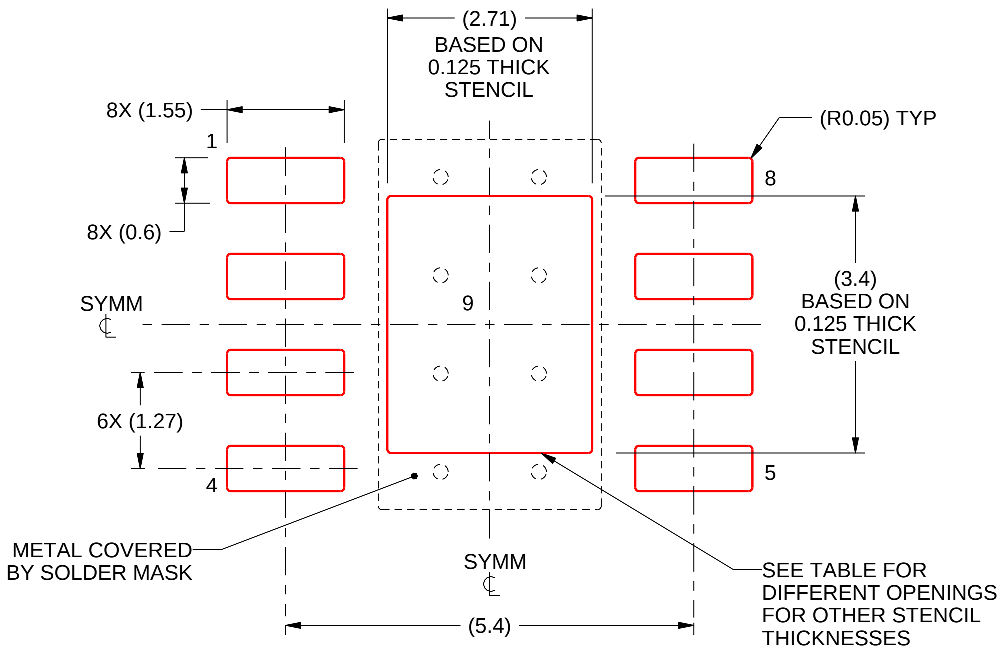


SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265