TEXAS INSTRUMENTS
TPS92663A-Q1
ZHCSMB0 – OCTOBER 2020

TPS92663A-Q1 适用于汽车前灯系统的高亮度 LED 矩阵管理器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 125°C T_A
  - 器件 HBM 分级等级：H1C
  - 器件 CDM 分级等级：C5
- 输入电压范围：4.5 V 至 60 V
- 6 个集成旁路开关
  - 3 个串联开关各有 2 个子灯串
  - 20V 最大跨开关电压
  - 62V 最大开关到接地电压
- 多点 UART 通信接口
  - 多达 16 个可寻址器件
  - 在同一总线上集成 TPS92662A-Q1
- 与 CAN 物理层兼容
  - 电缆线束中具有最少的导线数
- 具有 2 个多路复用器输入的 8 位 ADC
- 晶体振荡器驱动器
- 可编程 10 位 PWM 调光
  - 单个相移和脉宽
  - 器件间同步
- LED 开路/短路检测和保护

2 应用

- 汽车前照灯系统
- 高亮度 LED 矩阵系统
- ADB 或无眩光远光灯
- 连续转向和动画日间行车灯

3 说明

TPS92663A-Q1 LED 矩阵管理器器件通过提供单个像素级 LED 控制来实现完全动态的自适应照明解决方案。

该器件的 3 个串联集成开关各有 2 个子灯串，可绕过单个 LED。各个子灯串允许器件接受单个或多个电流源。它还能并联 2 个开关，用于绕过高电流 LED。

主微控制器通过多点通用异步收发器 (UART) 串行接口，控制和管理 TPS92663A-Q1 器件。串行接口支持使用 CAN 收发器，实现更可靠稳健的物理层。应用可使用 TPS92663A-Q1 器件，也可以使用与该器件在同一总线上的 TPS92662A-Q1 器件。

具有两个多路复用输入的内置 8 位 ADC 可用于系统温度补偿和测量分箱值，从而实现 LED 分箱和编码。

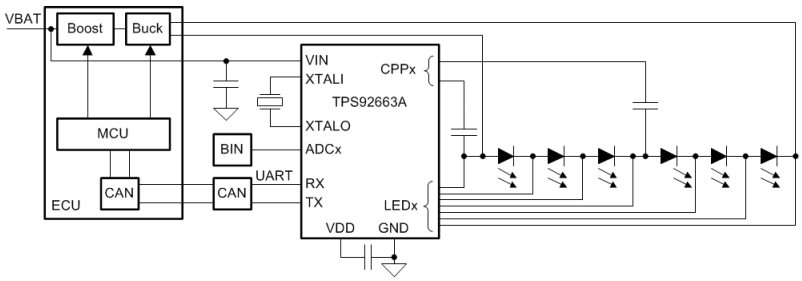
内部电荷泵轨为 LED 旁路开关提供栅极驱动电压。旁路开关的低电阻 ($R_{DS(on)}$) 可最大程度地减少传导损耗和功率耗散。

灯串中每个 LED 的相移和脉冲宽度是可编程的。该器件使用内部寄存器来调节 PWM 频率。可以对多个器件进行同步。在 PWM 调光操作过程中，开关转换具有可编程的压摆率，用于缓解 EMI 问题。该器件具有开路 LED 保护功能（阈值可编程）。串行接口会报告开路 LED 或短路 LED 故障。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TPS92663A-Q1	PWP (24)	7.70mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2020	*	Initial release

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92663AQPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92663AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

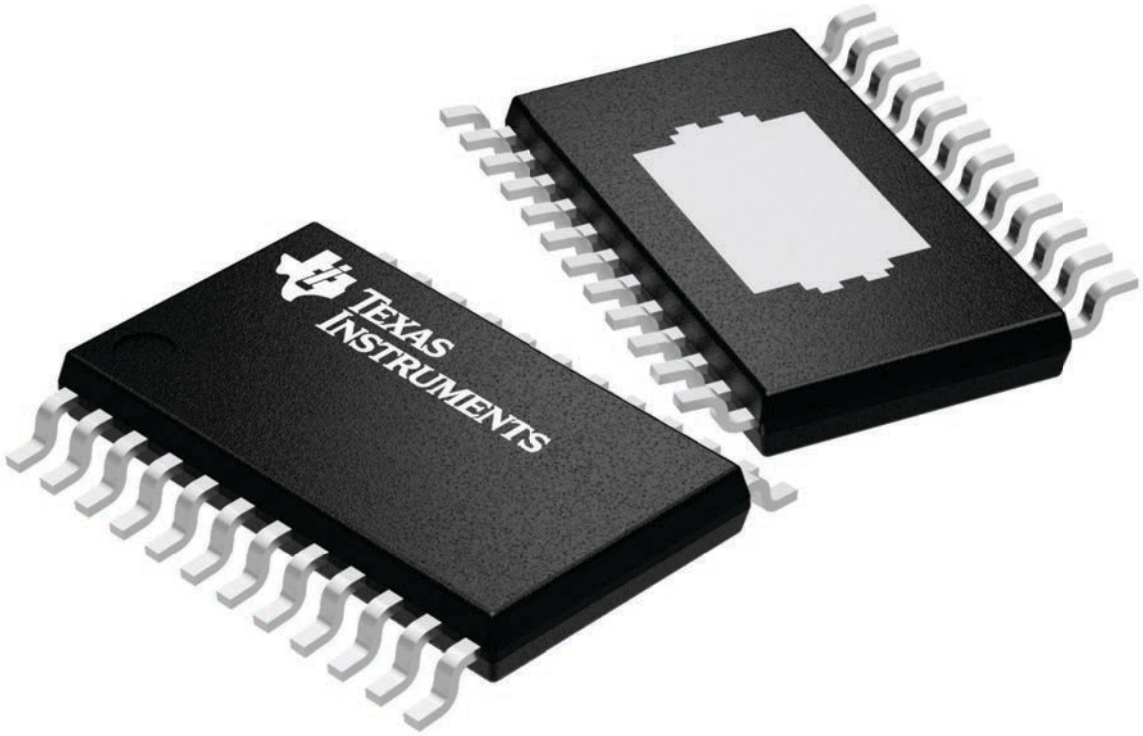
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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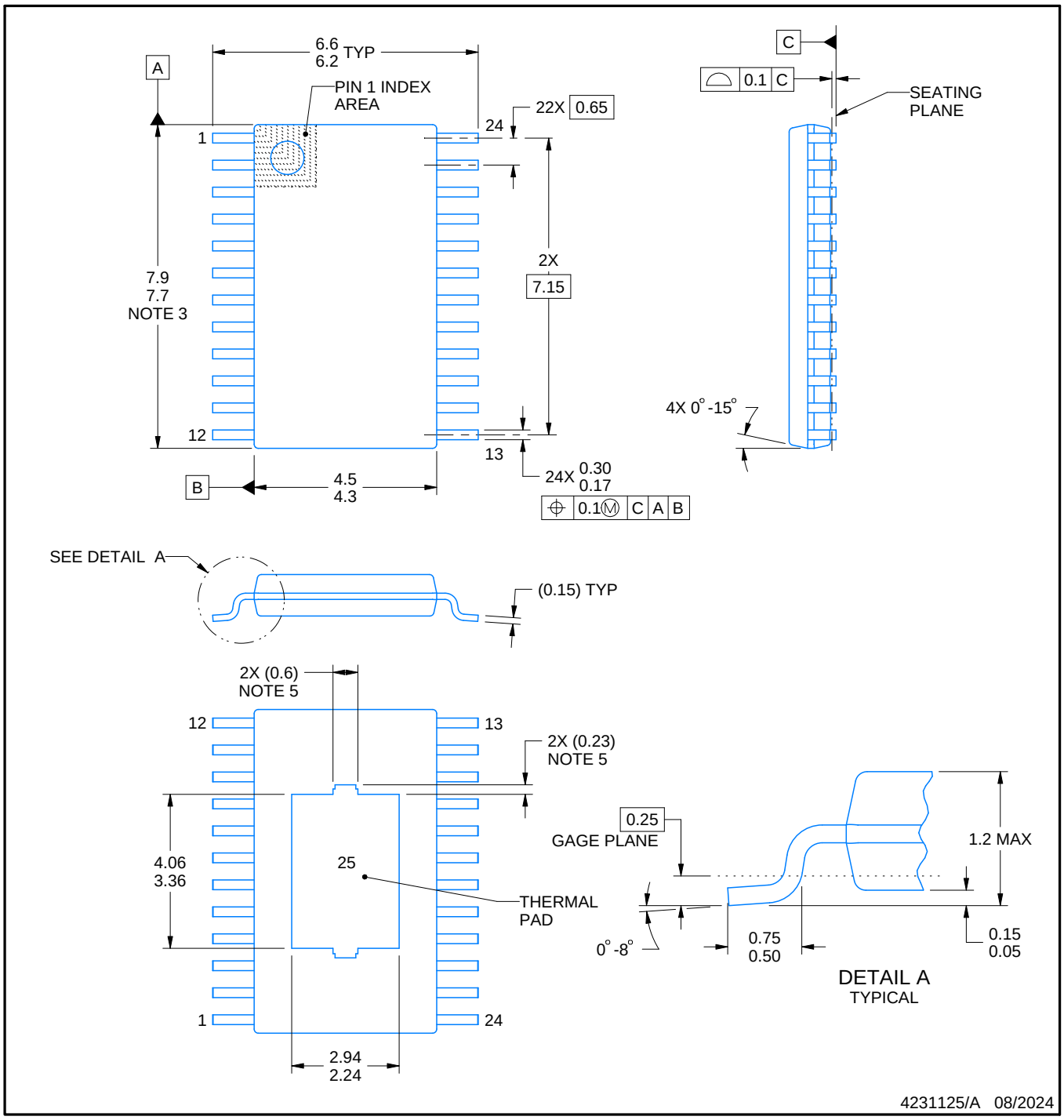
PACKAGE OUTLINE

PWP0024W

PowerPAD™ TSSOP - 1.2 mm max height

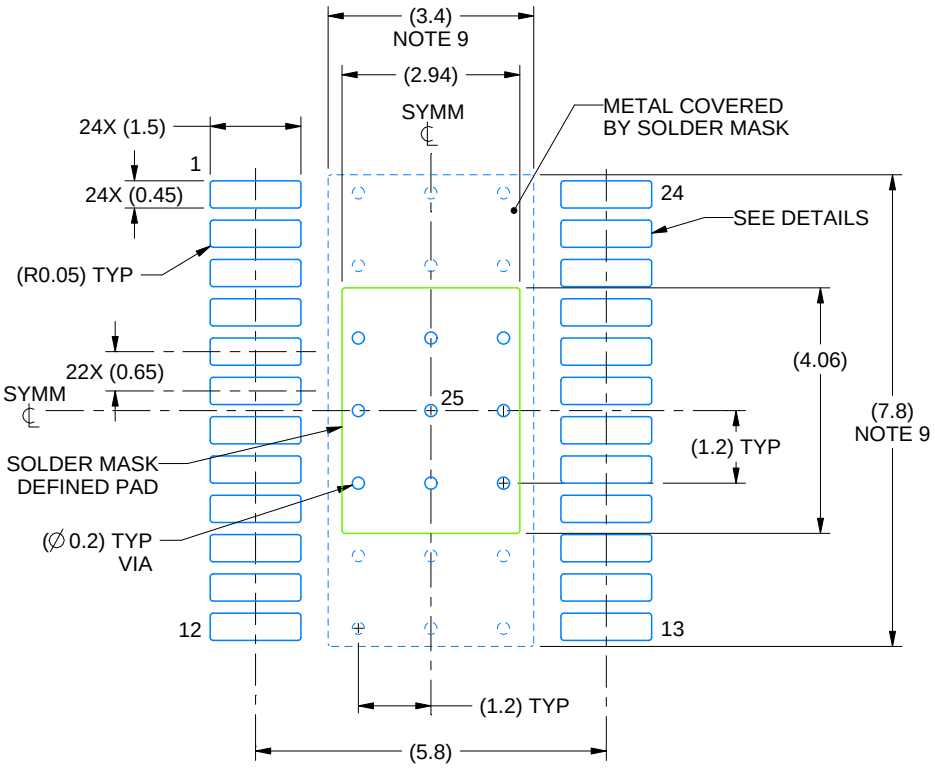
SMALL OUTLINE PACKAGE



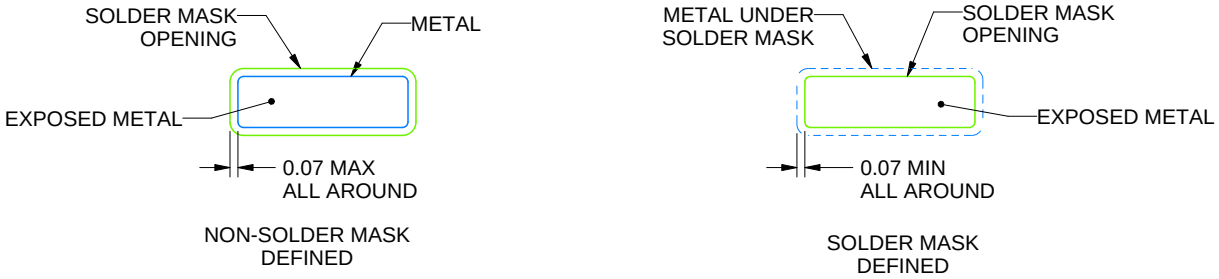
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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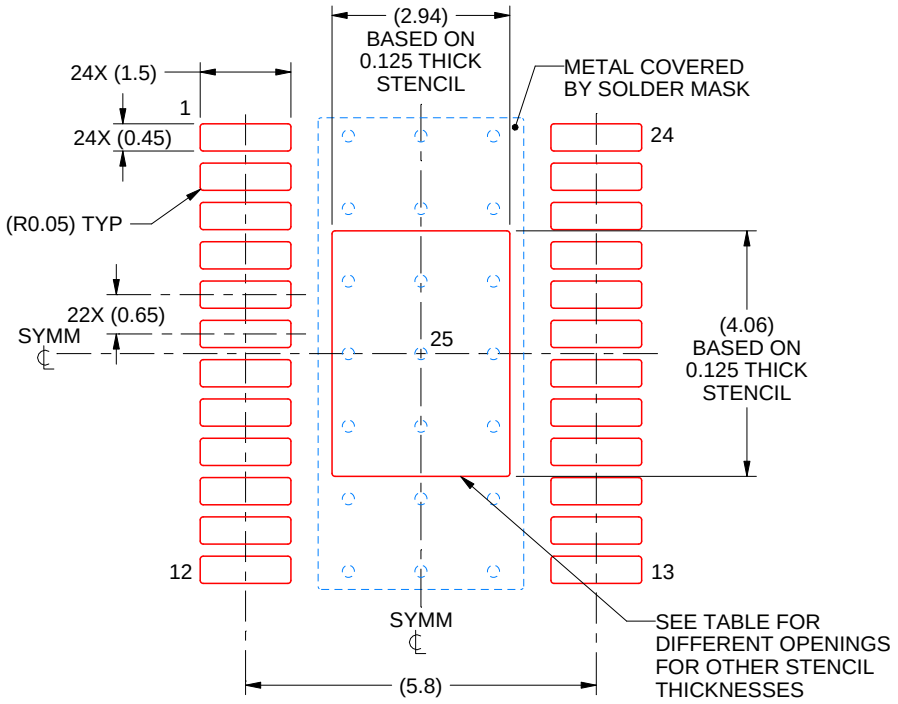
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.29 X 4.54
0.125	2.94 X 4.06 (SHOWN)
0.15	2.68 X 3.71
0.175	2.48 X 3.43

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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