

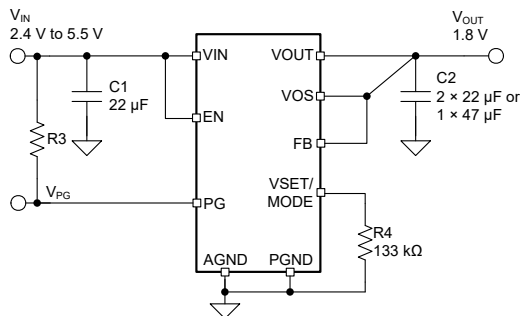
TPSM8286xA 具有集成电感器、采用薄型超模压塑料 QFN 和 MagPack™ 封装的 2.4V 至 5.5V 输入、4A/6A 降压电源模块

1 特性

- 效率高达 96%
- 优异的热性能
- 1% 的输出电压精度
- 可实现快速瞬态响应的 DCS-Control 拓扑
- 专为满足低 EMI 要求而设计
 - 采用 MagPack 技术屏蔽电感器和 IC
 - 无键合线封装
 - 通过优化的引脚排列简化了布局
- 输入电压范围为 2.4V 至 5.5V
- 同一器件型号可提供：
 - 0.6V 至 V_{IN} 可调节输出电压
 - 13 个集成式固定输出电压选项
 - 强制 PWM 或省电模式
- 具有窗口比较器的电源正常状态指示器
- 2.4MHz 开关频率
- 4μA 运行静态电流
- 输出电压放电
- 100% 占空比模式
- -40°C 至 125°C 工作温度范围
- 间距为 0.5mm 的 QFN 封装：
 - RDJ、RDM：3.5mm × 4.0mm
 - RCF (MagPack)：2.3mm × 3.0mm
- 设计尺寸小：
 - RDJ、RDM：35mm² 设计尺寸
 - RCF (MagPack)：28mm² 设计尺寸
- 也可使用 I²C 接口：TPSM82866C

2 应用

- 适用于 FPGA、CPU、ASIC 的内核电源
- 光学模块
- 工业运输
- 工厂自动化和控制
- 航天和国防



典型应用原理图 - 固定输出电压选项

3 说明

TPSM8286xA 器件系列包含旨在实现小解决方案尺寸和高效率的 4A 和 6A 降压转换器电源模块。该电源模块集成了同步降压转换器和电感器，可简化设计、减少外部元件并节省印刷电路板 (PCB) 面积。该器件采用紧凑的薄型封装，旨在通过标准表面贴装设备进行自动组装。采用的 DCS-Control 架构可实现严格的输出电压精度（即使与小型输出电容搭配工作时也是如此），以及出色的负载瞬态性能。该系列转换器在中高负载条件下以 PWM 模式运行，并在轻负载时自动进入节能模式运行，从而在整个负载电流范围内保持高效率。此类器件还可强制进入 PWM 模式运行，以实现超小的输出电压纹波。器件的 EN 和 PG 引脚支持顺序配置，可带来灵活的系统设计。集成的软启动功能降低了输入电源需要提供的浪涌电流。RDJ 封装支持高度为 1.4mm 的薄型设计。

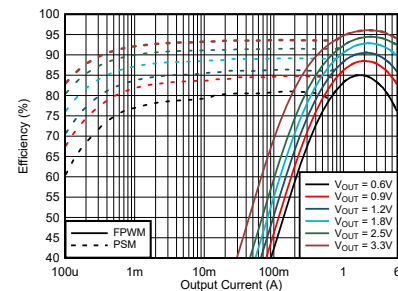
器件信息

器件型号 ⁽³⁾	输出电流	封装 ⁽¹⁾	本体尺寸 (标称值)
TPSM82864A	4A	RDJ 或 RDM	3.50mm × 4.00mm
TPSM82866A	6A	(B0QFN, 23)	
TPSM82864A ⁽²⁾	4A	RCF (QFN-FCMOD, 15)	2.30mm × 3.00mm
TPSM82866A	6A		

(1) 有关更多信息，请参阅节 11。

(2) 预发布信息 (非量产数据)。

(3) 请参阅器件选项表。



TPSM82866AA0HRDMR - 效率与输出电流间的关系曲线； $V_{IN} = 5.0V$



Table of Contents

1 特性	1	8 Application and Implementation	17
2 应用	1	8.1 Application Information.....	17
3 说明	1	8.2 Typical Application.....	17
4 Device Options	3	8.3 Power Supply Recommendations.....	26
5 Pin Configuration and Functions	3	8.4 Layout.....	26
6 Specifications	5	9 Device and Documentation Support	29
6.1 Absolute Maximum Ratings.....	5	9.1 Device Support.....	29
6.2 ESD Ratings.....	5	9.2 Documentation Support.....	29
6.3 Recommended Operating Conditions.....	5	9.3 接收文档更新通知.....	29
6.4 Thermal Information.....	6	9.4 支持资源.....	29
6.5 Electrical Characteristics.....	7	9.5 Trademarks.....	29
6.6 Typical Characteristics.....	9	9.6 静电放电警告.....	29
7 Detailed Description	10	9.7 术语表.....	29
7.1 Overview.....	10	10 Revision History	30
7.2 Functional Block Diagram.....	10	11 Mechanical, Packaging, and Orderable	
7.3 Feature Description.....	10	Information	30
7.4 Device Functional Modes.....	14		

4 Device Options

ORDERABLE PART NUMBER ⁽¹⁾	OUTPUT CURRENT	OPERATING FREQUENCY	NOMINAL INDUCTANCE	BODY SIZE	DEVICE HEIGHT
TPSM82864AA0SRDJR	4 A	2.4 MHz	220 nH	3.5 mm × 4.0 mm	1.4 mm
TPSM82866AA0SRDJR	6 A				1.8 mm
TPSM82864AA0HRDMR	4 A				
TPSM82866AA0HRDMR	6 A				
TPSM82864AA0PRCFR ⁽²⁾	4 A		200 nH	2.3 mm × 3.0 mm	1.95 mm
TPSM82866AA0PRCFR	6 A				
TPSM82864BA0PRCFR ⁽²⁾	4 A	1.2 MHz			
TPSM82866BA0PRCFR ⁽²⁾	6 A				

(1) For more information, see 节 11.

(2) Preview information (not Production Data).

5 Pin Configuration and Functions

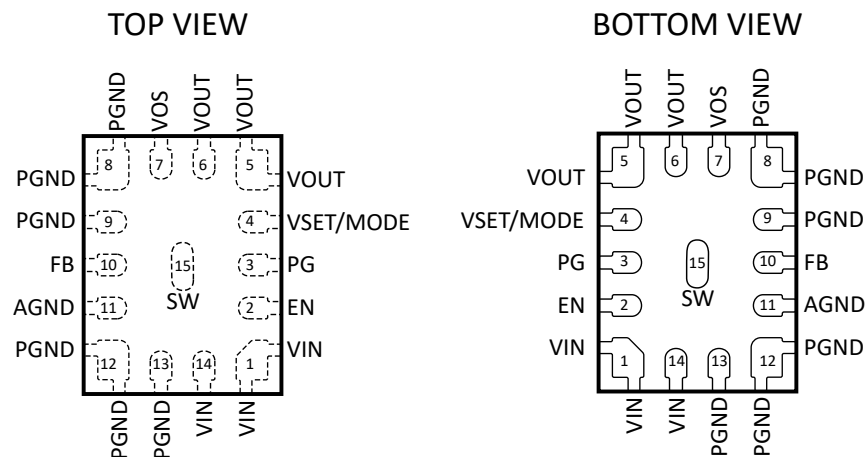


图 5-1. TPSM82864A, TPSM82866A - RCF (15 Pin) QFN-FCMOD

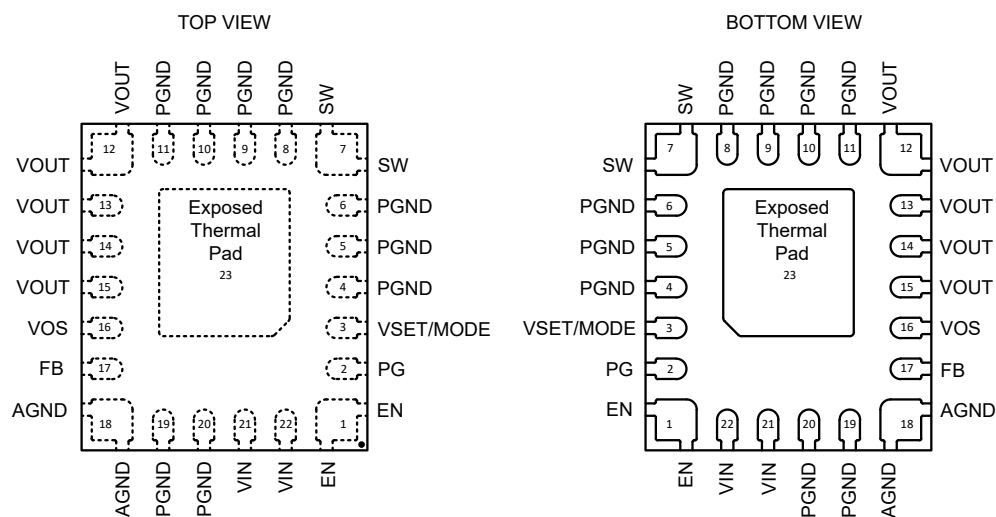


图 5-2. TPSM82864A, TPSM82866A - RDJ (23 Pin) and RDM (23 Pin) B0QFN

表 5-1. Pin Functions

PIN			TYPE ⁽¹⁾	DESCRIPTION
NAME	RDJ and RDM	RCF		
AGND	18	11	P	Analog ground pin. Must be connected to a common GND plane.
EN	1	2	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
FB	17	10	I	Voltage feedback input. Connect the output voltage resistor divider to this pin. When using a fixed output voltage, connect directly to VOUT.
PG	2	3	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
PGND	4, 5, 6, 8, 9, 10, 11, 19, 20	8, 9, 12, 13	P	Power ground pin. Must be connected to common GND plane.
SW	7	15	O	Switch pin of the power stage. This pin can be left floating.
VIN	21, 22	1, 14	P	Power supply input voltage pin
VOS	16	7	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
VOUT	12, 13, 14, 15	5, 6	P	Output voltage pin
VSET/ MODE	3	4	I	Connecting a resistor to GND selects one of the fixed output voltages. Tying the pin high or low selects an adjustable output voltage. After the device has started up, the pin operates as a MODE input. Applying a high level selects forced PWM mode operation and a low level selects power save mode operation.
Exposed Thermal Pad	23	-	P	Internally connected to PGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability. Must be connected to common GND plane.

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN, VOS, FB, PG, VSET/MODE	– 0.3	6	V
	SW (DC), VOUT	– 0.3	VIN + 0.3	
	SW (AC, less than 10ns) ⁽³⁾	– 2.5	10	
ISINK_PG	Sink current at PG		2	mA
TJ	Junction temperature	– 40	125	°C
Tstg	Storage temperature	– 40	125	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VIN	Supply voltage range	2.4		5.5	V
VOUT	Output voltage range	0.6		VIN	V
tF_VIN	Falling transition time at VIN ⁽¹⁾			10	mV/μs
IOUT	Output current, TPSM82864A			4	A
	Output current, TPSM82866A			6	
RVSET	Nominal resistance range for external voltage selection resistor (E96 resistor series)	10		249	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
TJ	Junction temperature	– 40		125	°C

- (1) The falling slew rate of VIN must be limited if VIN goes below VUVLO (see Power Supply Recommendations).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPSM8286xA						UNIT
		RDM (23 PINS)		RDJ (23 PINS)		RCF (15 PINS)		
		JEDEC 51-5	EVM	JEDEC 51-5	EVM	JEDEC 51-7	EVM	
R _{θ JA}	Junction-to-ambient thermal resistance	43.2	25.9	43.3	25.4	66.4	29.9	°C/W
R _{θ JC(top)}	Junction-to-case (top) thermal resistance	42.5	n/a ⁽²⁾	34.3	n/a ⁽²⁾	31.8	n/a ⁽²⁾	°C/W
R _{θ JC(bottom)}	Junction-to-case (bottom) thermal resistance	21.1	n/a ⁽²⁾	22.2	n/a ⁽²⁾	n/a ⁽³⁾	n/a ⁽²⁾	°C/W
R _{θ JB}	Junction-to-board thermal resistance	14.9	n/a ⁽²⁾	10.8	n/a ⁽²⁾	19.5	n/a ⁽²⁾	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	6.8	3.7	3.6	2.4	(-2.2) ⁽⁴⁾	(-4.2) ⁽⁴⁾	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	14.8	12.7	10.7	10.9	18.8	15.5	°C/W

(1) For more information about thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

(2) Not applicable to an EVM.

(3) Only applicable for packages with exposed thermal pad.

(4) The junction temperature is lower than the inductor temperature leading to a temperature increase towards the top of the package

6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , and $V_{IN} = 2.4\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current into VIN pin	EN = High, no load, device not switching		4	10	μA
I_{Q_VOS}	Quiescent current into VOS pin	EN = High, no load, device not switching, $V_{VOS} = 1.8\text{ V}$		8		μA
I_{SD}	Shutdown current	EN = Low, $T_J = -40^{\circ}\text{C}$ to 85°C		0.24	1	μA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		$^{\circ}\text{C}$
	Thermal shutdown hysteresis	T_J falling		20		$^{\circ}\text{C}$
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN and VSET/MODE		1.0			V
V_{IL}	Low-level input threshold voltage at EN and VSET/MODE				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	μA
START-UP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching with a 249-k Ω resistor connected between VSET/MODE and GND	420	650	1100	μs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good	0.8	1	1.5	ms
$V_{PG(low)}$	Power-good lower threshold	V_{FB} referenced to $V_{FB(nominal)}$	85	91	96	%
$V_{PG(high)}$	Power-good upper threshold	V_{FB} referenced to $V_{FB(nominal)}$	103	111	120	%
$V_{PG,OL}$	Low-level output voltage	$I_{sink} = 1\text{ mA}$			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	$V_{PG} = 5.0\text{ V}$		0.01	0.1	μA
$t_{PG,DLY}$	Power good delay	Rising and falling edges		34		μs
OUTPUT						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, $T_J = 0^{\circ}\text{C}$ to 85°C	- 1		1	%
		Fixed voltage operation, FPWM, no load	- 2		2	%
V_{FB}	Feedback voltage	Adjustable voltage operation	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation, $V_{FB} = 0.6\text{ V}$		0.01	0.4	μA
R_{DIS}	Output discharge resistor at VOS pin			3.5		Ω
	Load regulation	$V_{OUT} = 1.2\text{ V}$, FPWM		0.04		%/A
POWER SWITCH						
R_{DP}	Dropout resistance	TPSM8286xAA0SRDJ 100% mode. $V_{IN} = 3.3\text{ V}$, $T_J = 25^{\circ}\text{C}$		28	35	m Ω
		TPSM8286xAA0PRCF 100% mode. $V_{IN} = 3.3\text{ V}$, $T_J = 25^{\circ}\text{C}$		26		m Ω
		TPSM8286xAA0HRDM 100% mode. $V_{IN} = 3.3\text{ V}$, $T_J = 25^{\circ}\text{C}$		26		m Ω
I_{LIM}	High-side FET forward current limit	TPSM82864A	5	5.5	6	A
		TPSM82866A	7	7.9	9	A
	Low-side FET forward current limit	TPSM82864A		4.5		A
		TPSM82866A		6.5		A
	Low-side FET negative current limit			- 3		A

$T_J = -40^{\circ}\text{C}$ to 125°C , and $V_{IN} = 2.4\text{ V}$ to 5.5 V . Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{IN} = 5\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sw}	PWM switching frequency	TPSM82866Ax, $I_{\text{OUT}} = 1\text{ A}$, $V_{\text{OUT}} = 1.2\text{ V}$		2.4		MHz

6.6 Typical Characteristics

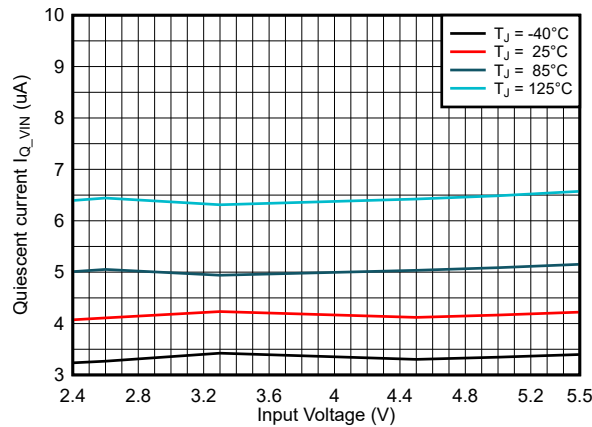


图 6-1. Quiescent Current into V_{IN} I_{Q_VIN}

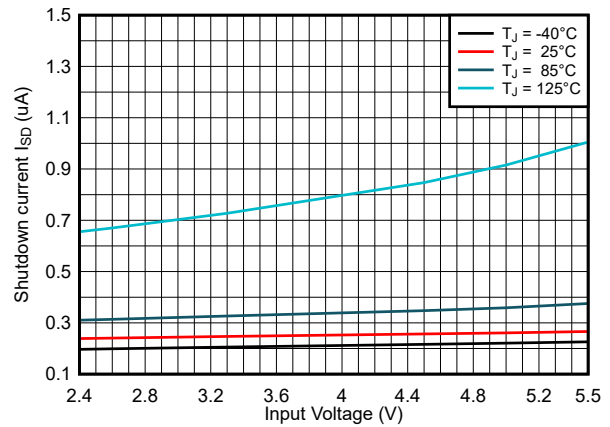


图 6-2. Shutdown Current I_{SD}

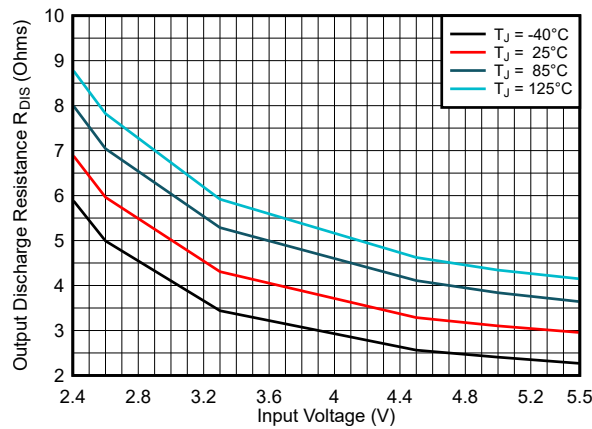
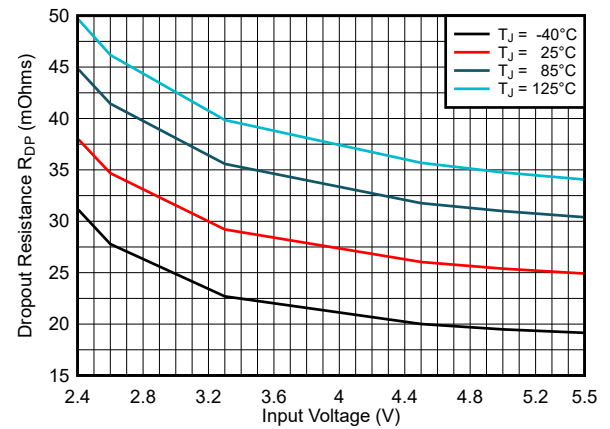
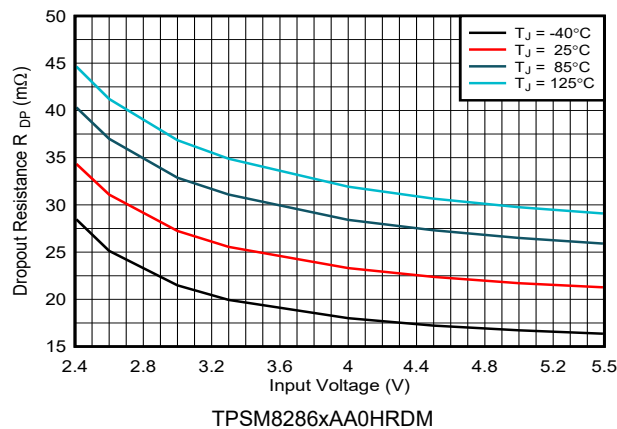


图 6-3. Output Discharge Resistance R_{OIS}



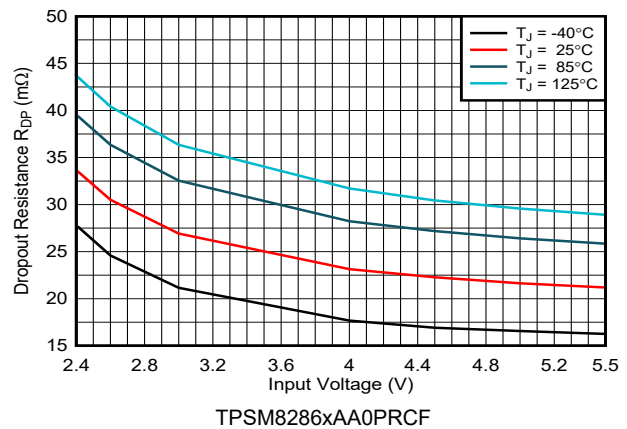
TPSM8286xAA0SRDJ

图 6-4. Dropout Resistance R_{DP}



TPSM8286xAA0HRDM

图 6-5. Dropout Resistance R_{DP}



TPSM8286xAA0PRCF

图 6-6. Dropout Resistance R_{DP}

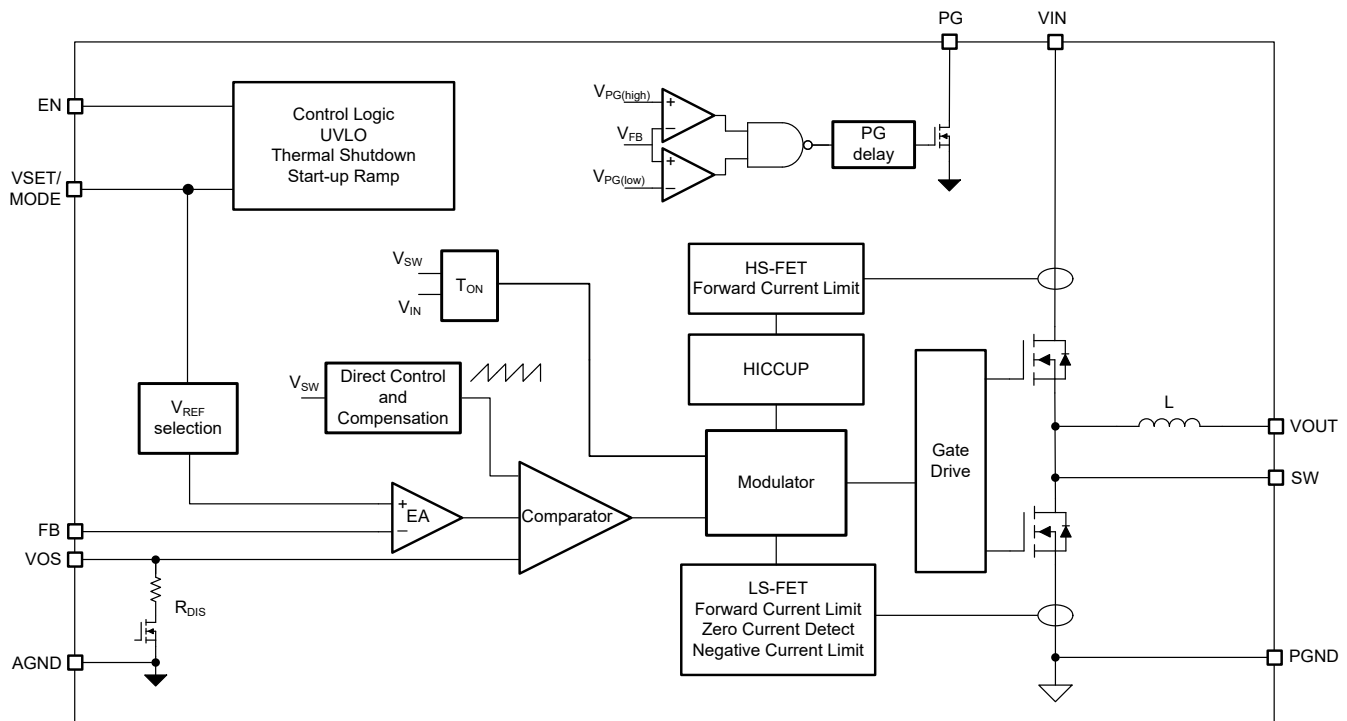
7 Detailed Description

7.1 Overview

The TPSM8286xA synchronous step-down converter power module is based on DCS-Control (Direct Control with Seamless transition into power save mode). This topology is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control. The DCS-Control topology operates in PWM (pulse width modulation) mode for medium-to-heavy load conditions and in PSM (power save mode) at light load currents. In PWM, the converter operates with the nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes using a single building block and, therefore, has a seamless transition from PWM to PSM without effects on the output voltage. The TPSM8286xA offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

The TPSM8286xxxP versions in the RCF package use MagPack technology to deliver the highest-performance power module design. Leveraging our proprietary integrated-magnetics MagPack packaging technology, these power modules deliver industry-leading power density, high efficiency and good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the device seamlessly enters power save mode (PSM) operation. In PSM, the converter operates with a reduced switching frequency and a minimum quiescent current to maintain high efficiency. Power save mode is based on a fixed on-time architecture, as shown in 方程式 1. The inductance used in the RCF package using MagPack technology is 200 nH typical where the inductance used in the RDJ and RDM packages is 220 nH typical.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

For very small output voltages, an absolute minimum on time of approximately 50ns is kept to limit switching losses. The operating frequency is thereby reduced from the nominal value, which keeps efficiency high. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

The load current at which PSM is entered is at one half of the ripple current of the inductor and can be estimated as:

$$I_{Load(PSM - entry)} = \frac{V_{IN} \times t_{ON}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (3)$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitance.

7.3.2 Forced PWM Mode

After the device has powered up and ramped up V_{OUT}, the VSET/MODE pin acts as a digital input. With a high level on the VSET/MODE pin, the device enters forced PWM (FPWM) mode and operates with a constant switching frequency over the entire load range, even at very light loads. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications but lowers efficiency at light loads.

7.3.3 Optimized Transient Performance from PWM to PSM Operation

For most converters, the load transient response in PWM mode is improved compared to PSM, because the converter reacts faster on the load step and actively sinks energy on the load release. As an additional feature, the TPSM8286xA automatically stays in PWM mode for 128 cycles after a heavy load release to bring the output voltage back to the regulation level faster. After these 128 cycles of PWM mode, it automatically returns to PSM (if VSET/MODE is low). See Figure 7-1. Without this optimization, the output voltage overshoot is higher.

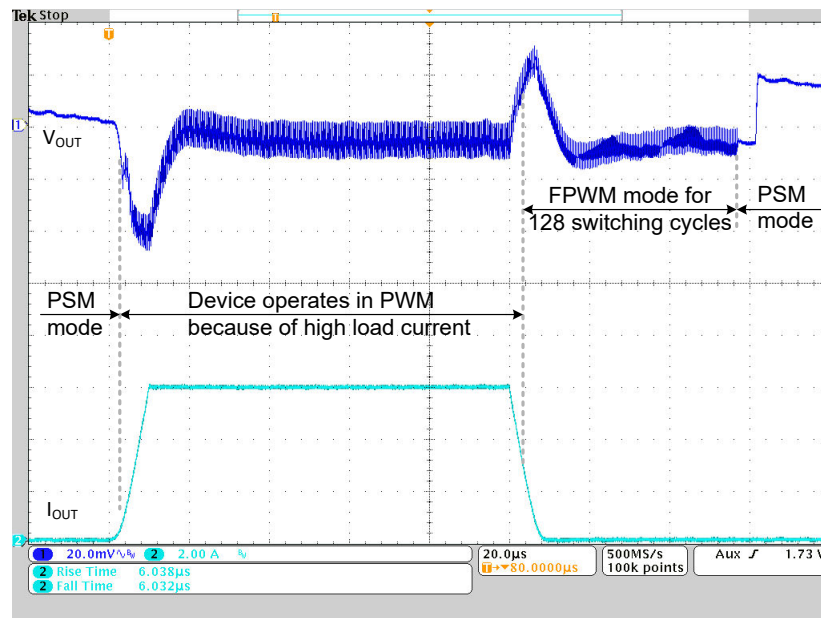


图 7-1. Optimized Transient Performance from PWM to PSM

7.3.4 Low Dropout Operation (100% Duty Cycle)

The device offers a low dropout operation by entering 100% duty cycle mode if the input voltage comes close to the target output voltage. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(max)} \times R_{DP} \quad (4)$$

where

- $V_{OUT(min)}$ = Minimum output voltage the load can accept
- $I_{OUT(max)}$ = Maximum output current
- R_{DP} = Resistance from V_{IN} to V_{OUT} (high-side $R_{DS(on)}$ + R_{DC} of the inductor)

7.3.5 Soft Start

After enabling the device, there is a 650- μ s enable delay (t_{Delay}) before the device starts switching. The t_{Delay} time varies with the VSET/MODE resistor used and is longest with a resistance of 249 k Ω or higher. After the enable delay, an internal soft-start circuit ramps up the output voltage in 1 ms (t_{Ramp}). This action avoids excessive inrush current and creates a smooth output voltage ramp up. This action also prevents excessive voltage drops of batteries that have a high internal impedance. 图 7-2 shows the start-up sequence.

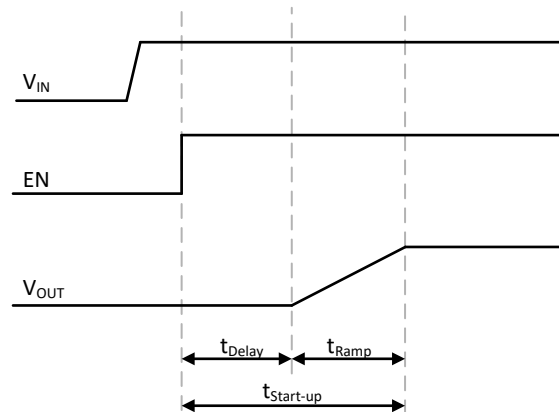


图 7-2. Start-Up Sequence

The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.6 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM} , cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on until the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 256 times, the device stops switching. The device then automatically re-starts with soft start after a typical delay time of 16 ms has passed. The device repeats this mode until the high load condition disappears. This HICCUP short-circuit protection reduces the current consumed from the input supply because the device only draws input current approximately 10% of the time during an overload condition. 图 8-37 shows the hiccup short-circuit protection.

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned

off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in forced PWM mode.

7.3.7 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) disables the device when the input voltage is lower than V_{UVLO} . When the input voltage recovers, the device automatically returns to operation with soft start.

7.3.8 Thermal Shutdown

When the junction temperature exceeds T_{JSD} , the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with soft start.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOS pin in shutdown mode. Do not leave the EN pin floating.

The typical enable threshold value of the EN pin is 0.66 V for rising input signals and the typical shutdown threshold is 0.52 V for falling input signals.

7.4.2 Output Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge is active when the EN pin is pulled low, when the input voltage is below the UVLO threshold or during thermal shutdown. The discharge is active down to an input voltage of 1.6 V (typical).

7.4.3 Power Good (PG)

The device has an open-drain power-good pin, which is specified to sink up to 2 mA. The power-good output requires a pullup resistor connected to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. 表 7-1 shows the typical PG pin logic.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	$0.9 \times V_{OUT_NOM} \leq V_{VOUT} \leq 1.1 \times V_{OUT_NOM}$	✓	
	$V_{VOUT} < 0.9 \times V_{OUT_NOM}$ or $V_{VOUT} > 1.1 \times V_{OUT_NOM}$		✓
Shutdown	EN = low		✓
Thermal shutdown	$T_J > T_{JSD}$		✓
UVLO	$1.8 \text{ V} < V_{IN} < V_{UVLO}$		✓
Power supply removal	$V_{IN} < 1.8 \text{ V}$	undefined	

The PG pin has a 34- μs delay time on the falling edge and a 34- μs delay before PG goes high. See 图 7-3.

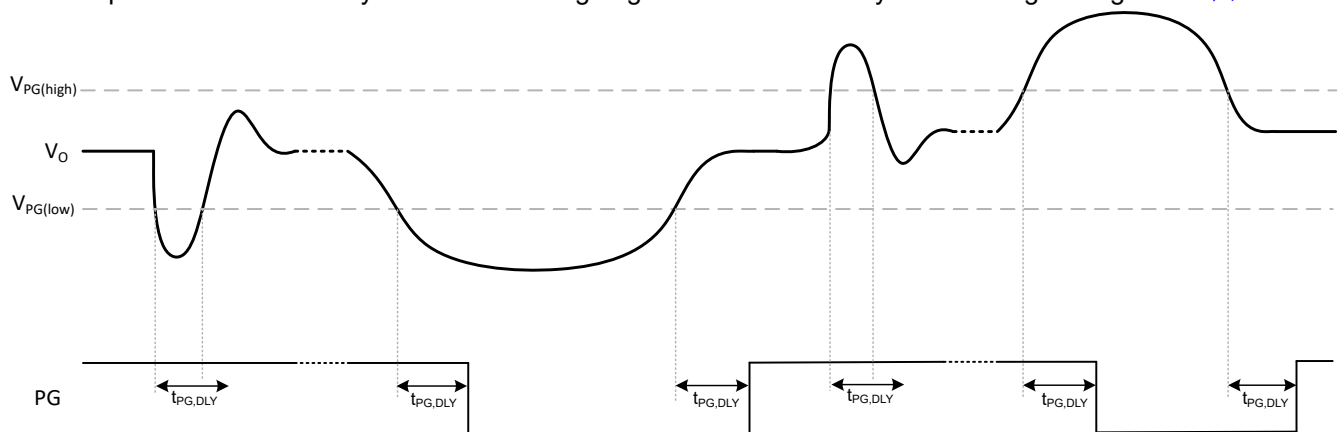


图 7-3. Power-Good Transient and Delay Behavior

7.4.4 Output Voltage and Mode Selection (VSET/MODE)

The TPSM8286xA family devices are configurable as either an adjustable output voltage or a fixed output voltage, depending on the needs of each individual application. This feature simplifies the logistics during mass production, as one part number offers several fixed output voltage options as well as an adjustable output voltage option. During the enable delay (t_{Delay}), the device configuration is set by an external resistor connected to the VSET/MODE pin through an internal R2D (resistor to digital) converter. This configures the V_{REF} input to the error amplifier (EA) to be either the V_{FB} voltage (0.6-V typical) or the selected output voltage. 表 7-2 shows the options.

表 7-2. Output Voltage Selection Table

RESISTOR AT VSET/MODE PIN (E96 SERIES, $\pm 1\%$ ACCURACY, 200 ppm/ $^{\circ}\text{C}$ OR BETTER)	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
249 k or logic high	Adjustable (through a resistive divider on the FB pin)
205 k	3.30 V
162 k	2.50 V
133 k	1.80 V
105 k	1.50 V
68.1 k	1.35 V
56.2 k	1.20 V
44.2 k	1.10 V
36.5 k	1.05 V
28.7 k	1.00 V
23.7 k	0.95 V
18.7 k	0.90 V
15.4 k	0.85 V
12.1 k	0.80 V
10 k or logic low	Adjustable (through a resistive divider on the FB pin)

The R2D converter has an internal current source, which applies current through the external resistor, and an internal ADC, which reads back the resulting voltage level. Depending on the detected resistance, the output voltage is set. After this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Make sure that the additional leakage current path is less than 20 nA and the capacitance is not greater than 30 pF from this pin to GND during R2D conversion, otherwise a false V_{OUT} value is set. For more details, refer to the [Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies White Paper](#). When the device is set to a fixed output voltage, the FB pin must be connected to the output directly. See 图 7-4.

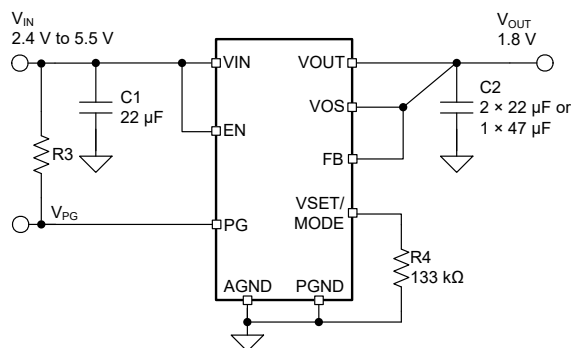


图 7-4. Fixed Output Voltage Application Circuit

After the start-up period ($t_{\text{Start-up}}$), a different operation mode can be selected. When VSET/MODE is set to high, the device is in [forced PWM mode](#). Otherwise, the VSET/MODE resistor pulls the pin low and the device operates in [power save mode](#).

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPSM8286xA is a synchronous step-down converter power module family. The following section discusses the selection of the external components to complete the power supply design. The required power inductor is integrated inside the TPSM8286xA. The integrated shielded inductor has a value of 220 nH with a $\pm 20\%$ tolerance for the RDJ and RDM packages. The RCF MagPack package not only has a 200 nH shielded inductor but also shields the IC for a better EMI performance. The TPSM82864A and TPSM82866A in the RDJ and RDM packages are pin-to-pin and BOM-to-BOM compatible. The TPSM8286xAA0HRDMR devices give a higher efficiency than the TPSM8286xAA0SRDJR devices due to the increased height. For a given package height (RDM or RDJ), the 4A and 6A version give the same efficiency and performance and are different only in the rated output current. The RCF package, using MagPack technology, is less than half the size of the other package versions (RDM and RDJ), thus shrinking the total design size by about 20%, while maintaining the same high efficiency as the other packages.

8.2 Typical Application

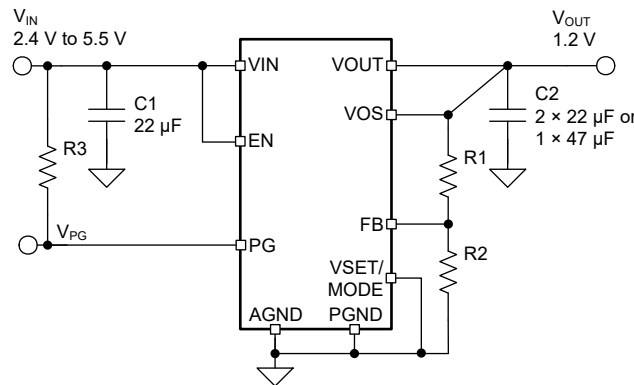


图 8-1. Typical Application

8.2.1 Design Requirements

For this design example, use 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	1.2 V
Maximum output current	6 A

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER ⁽¹⁾
C1	22 µF, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44	Murata
C2	47 µF, Ceramic capacitor, 6.3 V, X6S, size 0805, JMK212BC6476MG-T or GRM21BC80J476ME01L	Taiyo Yuden or Murata
R1	Depending on the output voltage, Chip resistor, 1/16 W, 1%	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%	Std

(1) See the *Third-party Products* disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting The Output Voltage

With the VSET/MODE pin set high or low, an adjustable output voltage is set by an external resistor divider according to [方程式 5](#):

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (5)$$

To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity but lower light-load efficiency, as explained in the [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief](#).

When a fixed output voltage is selected, connect the FB pin directly to the output. R1 and R2 are not needed, as V_{OUT} is set through a resistor on the VSET/MODE pin. Select the recommended resistor value from the list in [表 7-2](#).

8.2.2.2 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. The input capacitor must be placed between VIN and PGND as close as possible to those pins. For most applications, 22 µF is sufficient, though a larger value reduces input current ripple. The input capacitor plays an important role in the EMI performance of the system as explained in the [Simplify Low EMI Design With Power Modules White Paper](#).

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. The capacitor value can range from 2 × 22 µF up to 150 µF. The recommended typical output capacitors are 2 × 22 µF or 1 × 47 µF with an X5R or better dielectric. Values over 150 µF can degrade the loop stability of the converter.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. Make sure that the effective input capacitance is at least 10 µF and the effective output capacitance is at least 22 µF.

8.2.3 Application Curves

$V_{IN} = 5.0\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $T_A = 25^\circ\text{C}$, BOM = 表 8-2, unless otherwise noted. Solid lines show the FPWM mode and dashed lines show PSM.

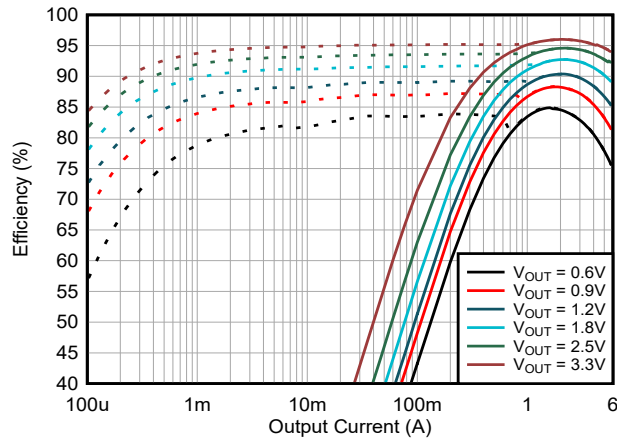


图 8-2. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$

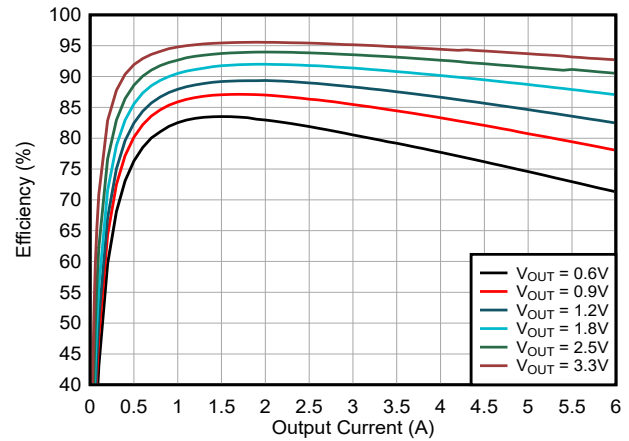


图 8-3. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 85^\circ\text{C}$

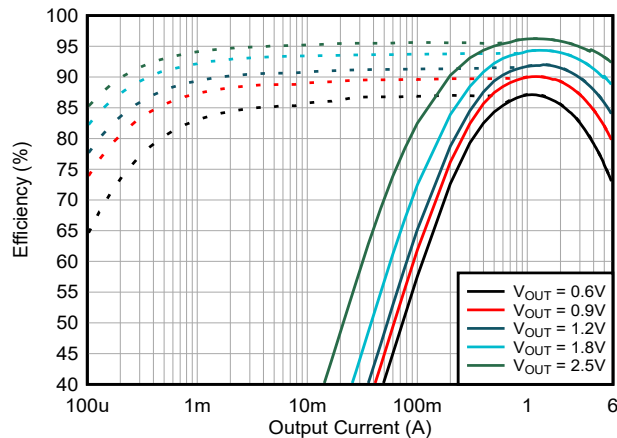


图 8-4. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$

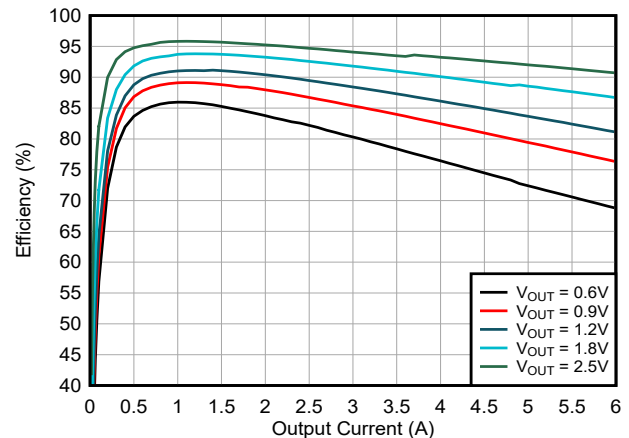
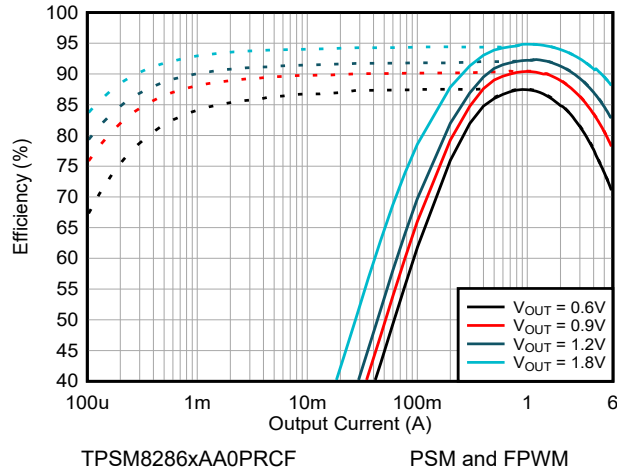
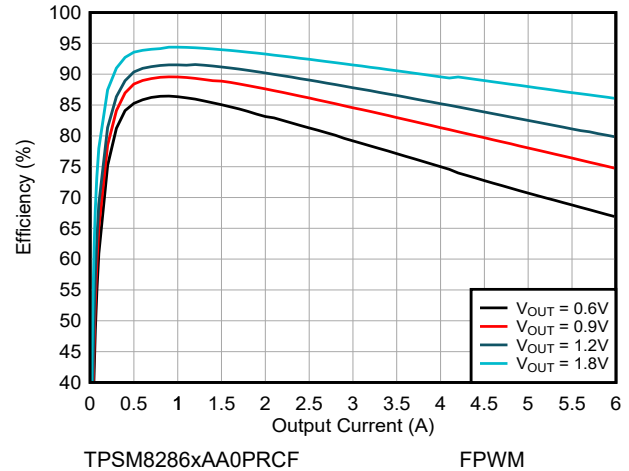
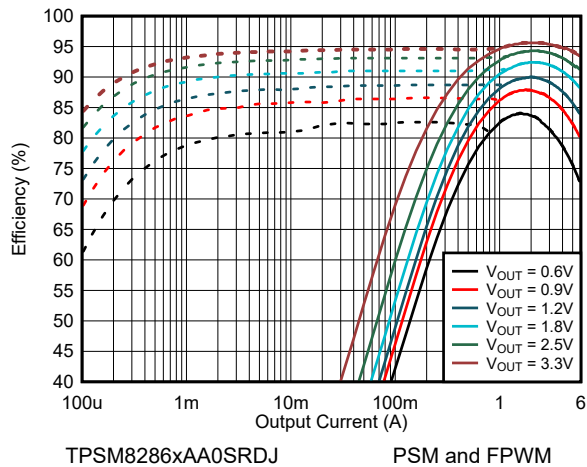
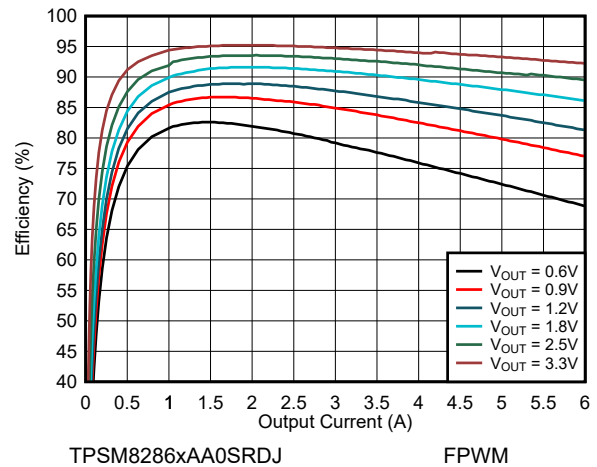
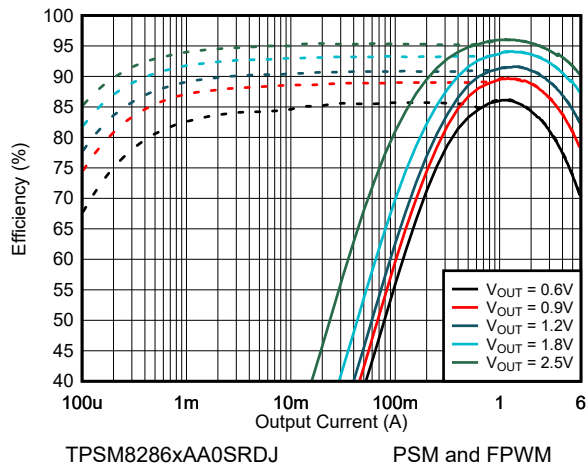
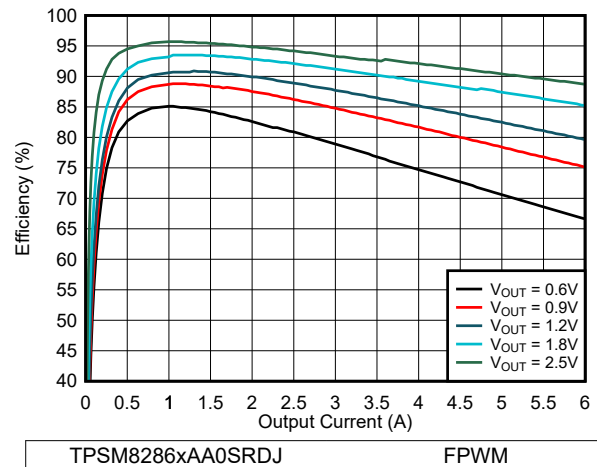


图 8-5. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 85^\circ\text{C}$

图 8-6. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 25^\circ\text{C}$ 图 8-7. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 85^\circ\text{C}$ 图 8-8. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$ 图 8-9. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 85^\circ\text{C}$ 图 8-10. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ 图 8-11. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 85^\circ\text{C}$

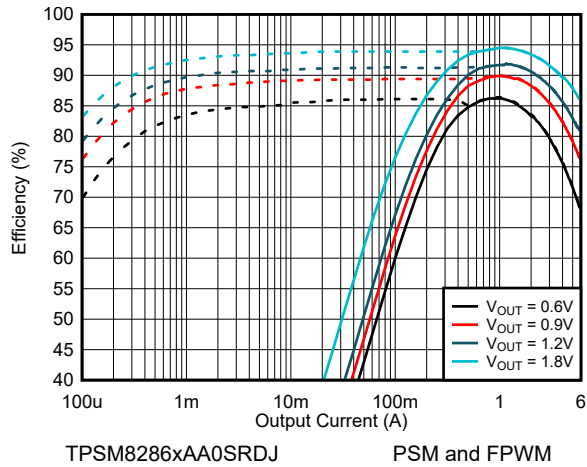


图 8-12. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 25^\circ\text{C}$

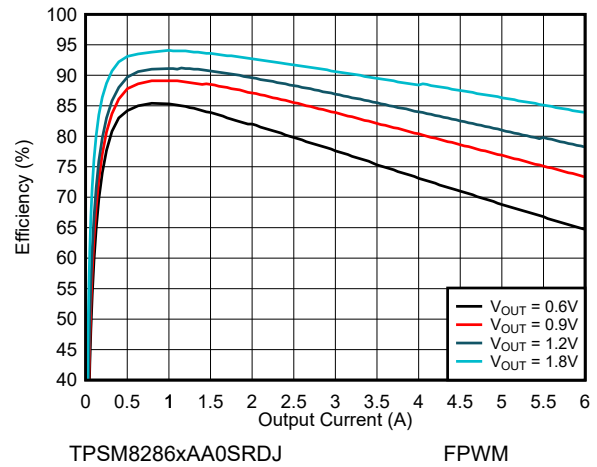


图 8-13. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 85^\circ\text{C}$

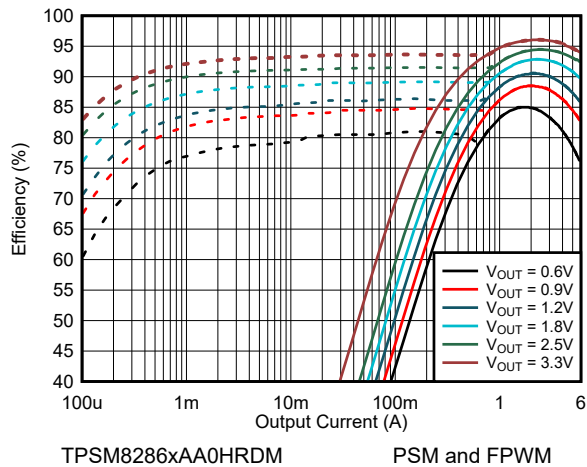


图 8-14. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 25^\circ\text{C}$

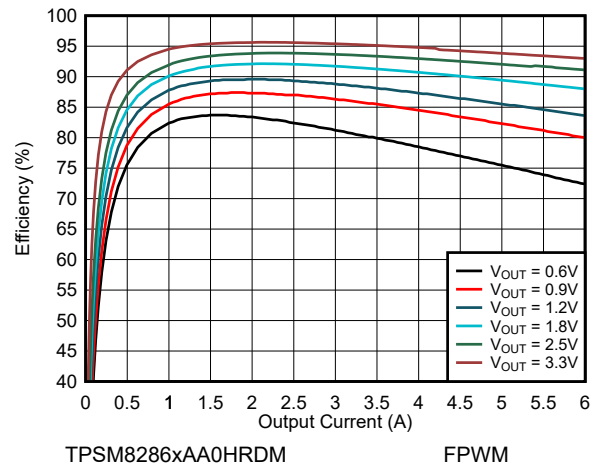


图 8-15. Efficiency $V_{IN} = 5.0\text{ V}$ and $T_A = 85^\circ\text{C}$

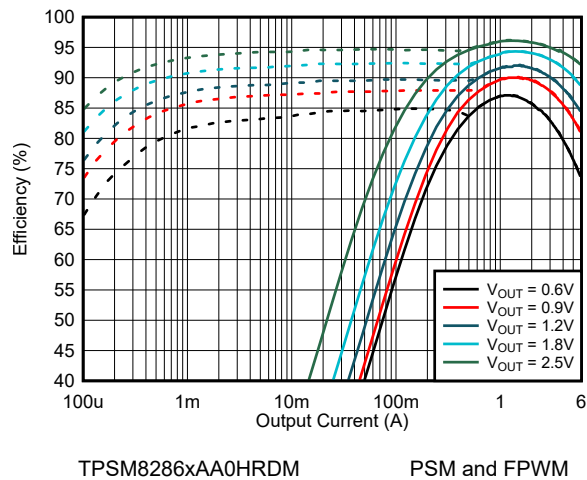


图 8-16. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$

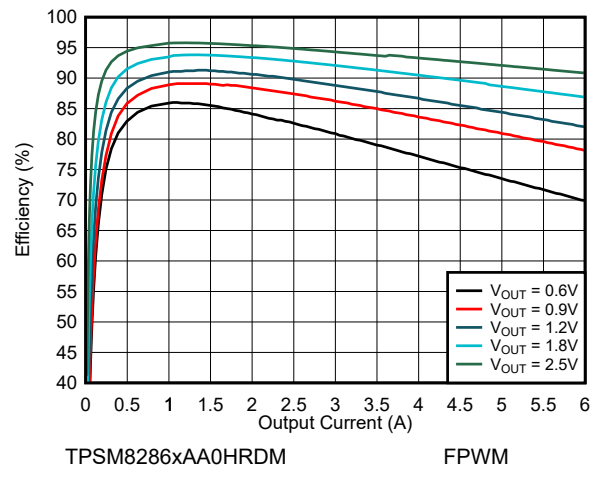
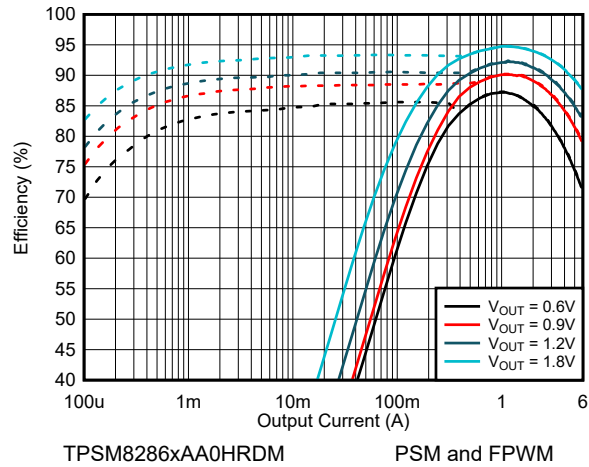
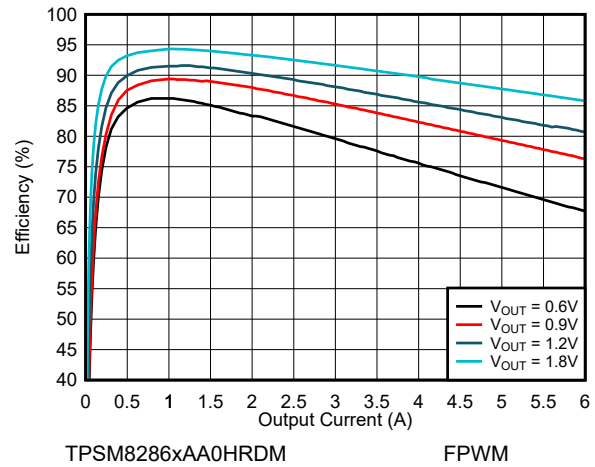
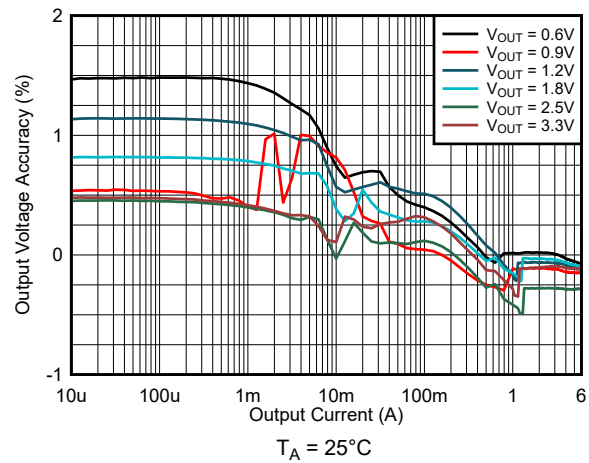
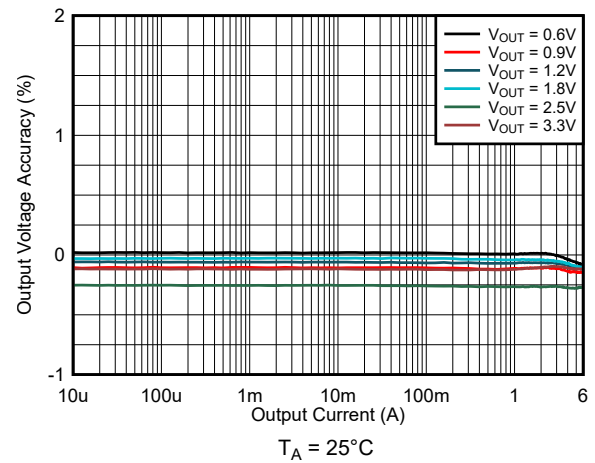
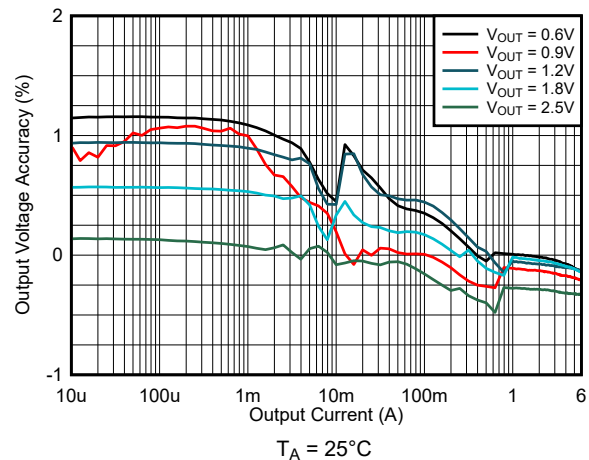
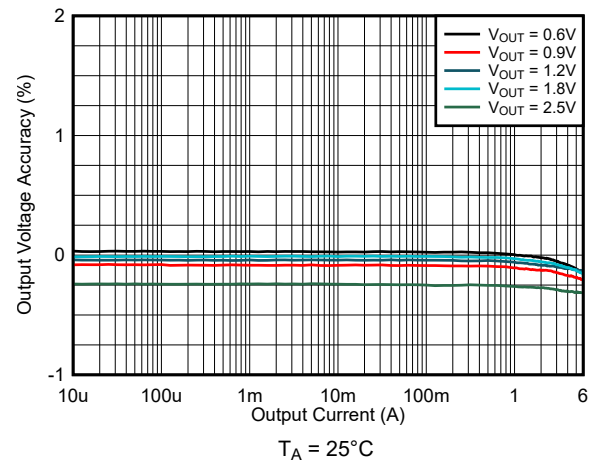


图 8-17. Efficiency $V_{IN} = 3.3\text{ V}$ and $T_A = 85^\circ\text{C}$

图 8-18. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 25^\circ\text{C}$ 图 8-19. Efficiency $V_{IN} = 2.8\text{ V}$ and $T_A = 85^\circ\text{C}$ 图 8-20. Load Regulation $V_{IN} = 5.0\text{ V}$ and PSM图 8-21. Load Regulation $V_{IN} = 5.0\text{ V}$ and FPWM图 8-22. Load Regulation $V_{IN} = 3.3\text{ V}$ and PSM图 8-23. Load Regulation $V_{IN} = 3.3\text{ V}$ and FPWM

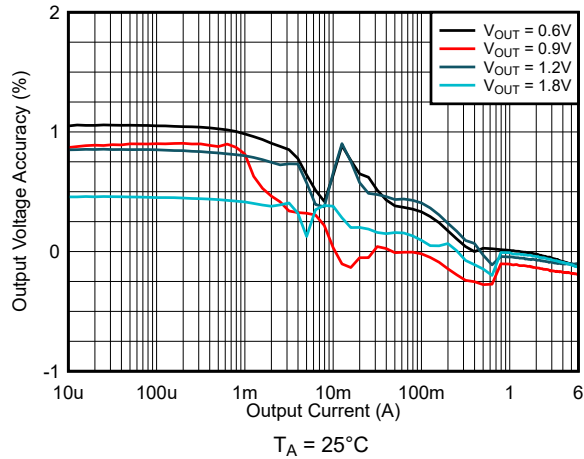


图 8-24. Load Regulation $V_{IN} = 2.8\text{ V}$ and PSM

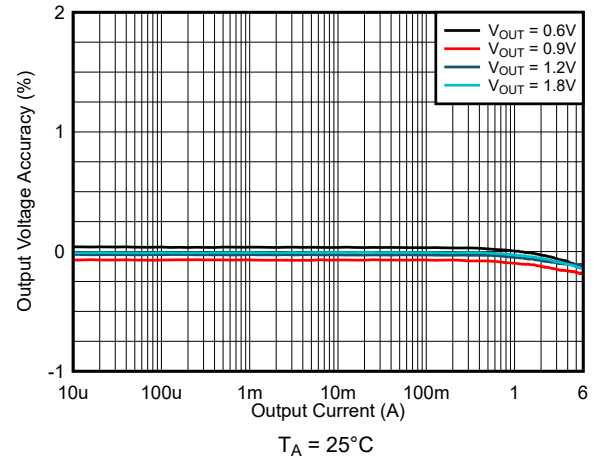


图 8-25. Load Regulation $V_{IN} = 2.8\text{ V}$ and FPWM

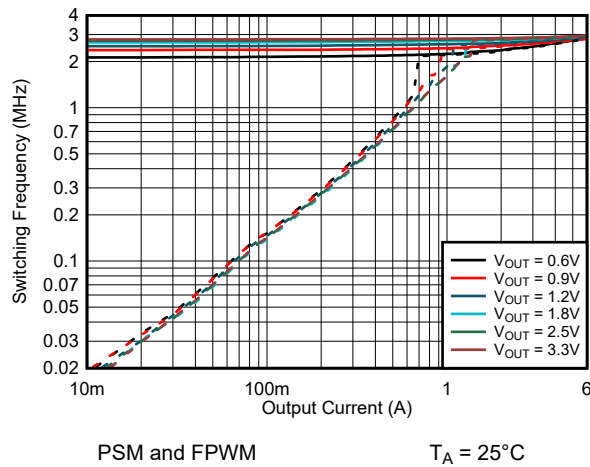


图 8-26. Switching Frequency $V_{IN} = 5.0\text{ V}$

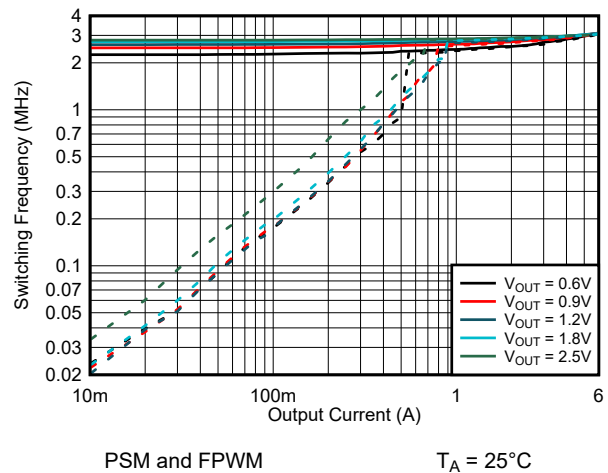
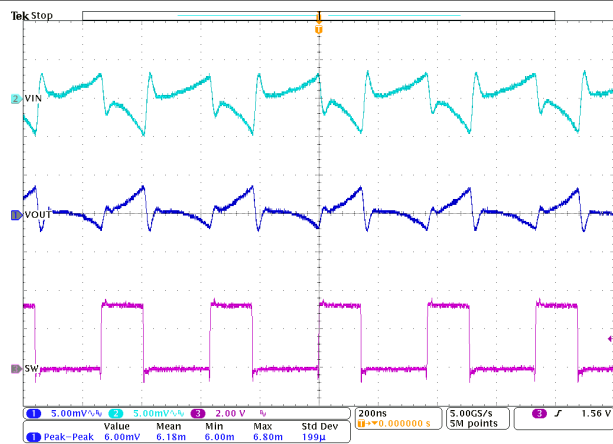
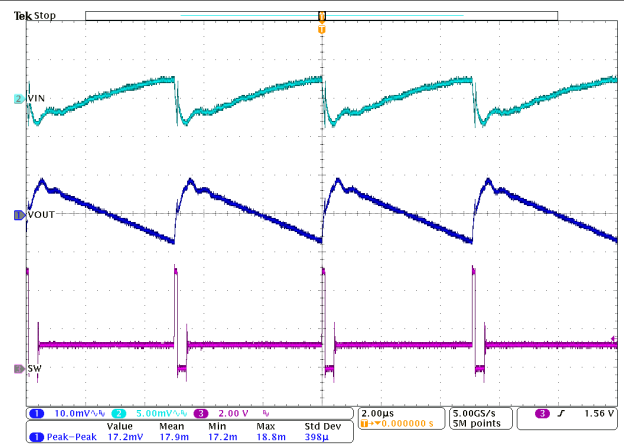


图 8-27. Switching Frequency $V_{IN} = 3.3\text{ V}$



$V_{IN} = 3.3\text{ V}$ $V_{OUT} = 1.2\text{ V}$ $C_{OUT} = 1 \times 47\mu\text{F}$

图 8-28. FPWM Operation $I_{OUT} = 3\text{ A}$



$V_{IN} = 5.0\text{ V}$ $V_{OUT} = 1.2\text{ V}$ $C_{OUT} = 1 \times 47\mu\text{F}$

图 8-29. PSM Operation $I_{OUT} = 0.1\text{ A}$

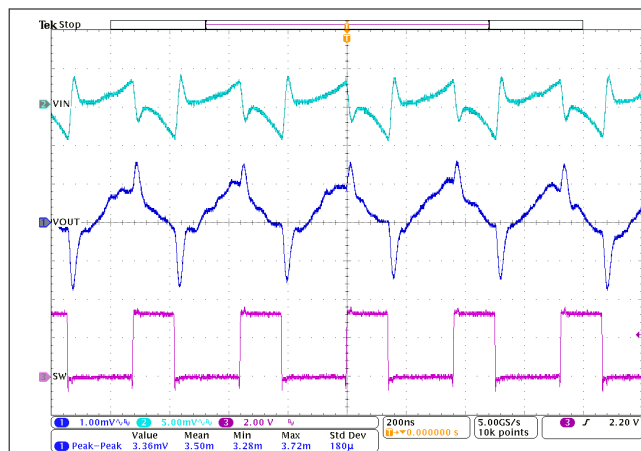
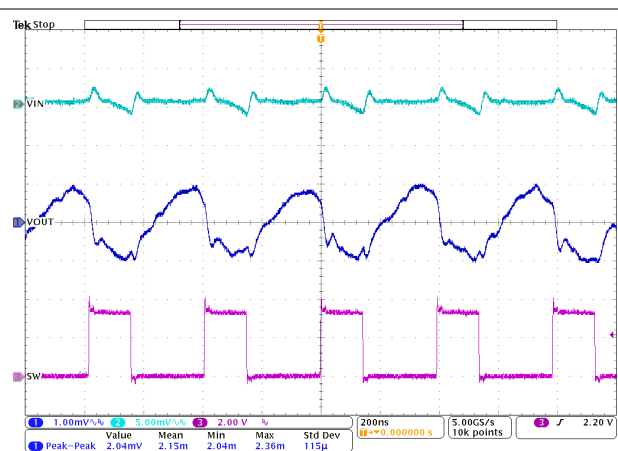
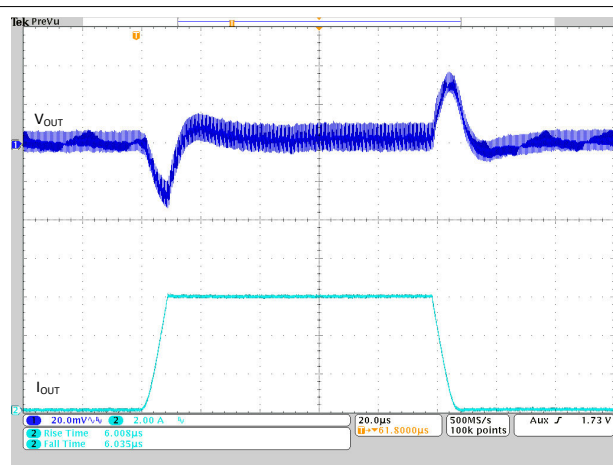
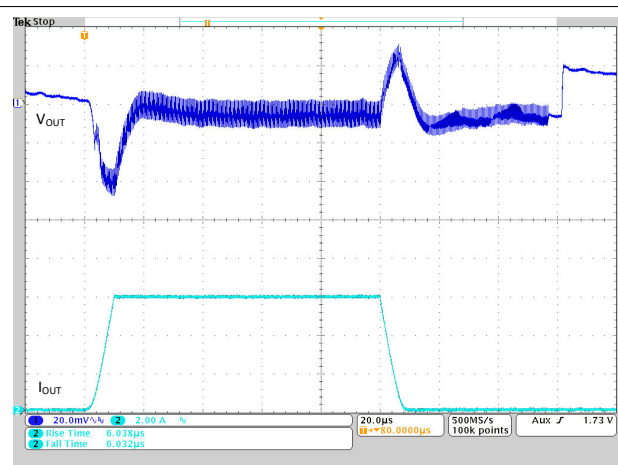
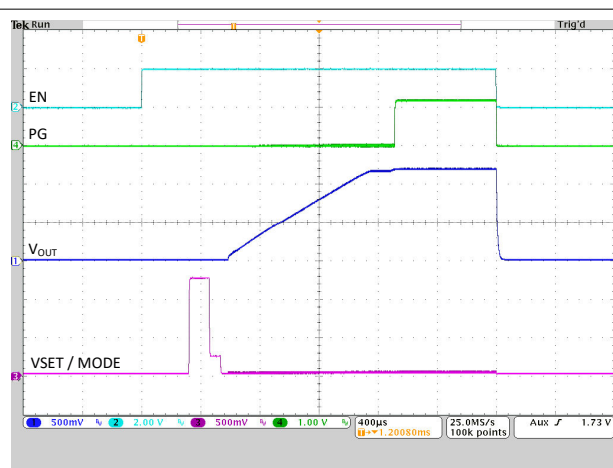

 $V_{IN} = 3.3 \text{ V}$ $V_{OUT} = 1.2 \text{ V}$ $C_{OUT} = 3 \times 22\mu\text{F}$
图 8-30. FPWM Operation $I_{OUT} = 3 \text{ A}$ 
 $V_{IN} = 3.3 \text{ V}$ $V_{OUT} = 1.2 \text{ V}$ $C_{OUT} = 3 \times 22\mu\text{F}$
图 8-31. FPWM Operation $I_{OUT} = 0.1 \text{ A}$ 
 $V_{IN} = 5.0 \text{ V}$ $V_{OUT} = 1.2 \text{ V}$ $C_{OUT} = 2 \times 22\mu\text{F}$
图 8-32. Load Transient FPWM $I_{OUT} = 0 \text{ A} \rightarrow 6 \text{ A}$ 
 $V_{IN} = 5.0 \text{ V}$ $V_{OUT} = 1.2 \text{ V}$ $C_{OUT} = 2 \times 22\mu\text{F}$
图 8-33. Load Transient PSM $I_{OUT} = 0 \text{ A} \rightarrow 6 \text{ A}$ 
 $R_{VSET} = 56.2 \text{ k}\Omega$ $I_{OUT} = 6.0 \text{ A}$

图 8-34. Start-Up into Full Load

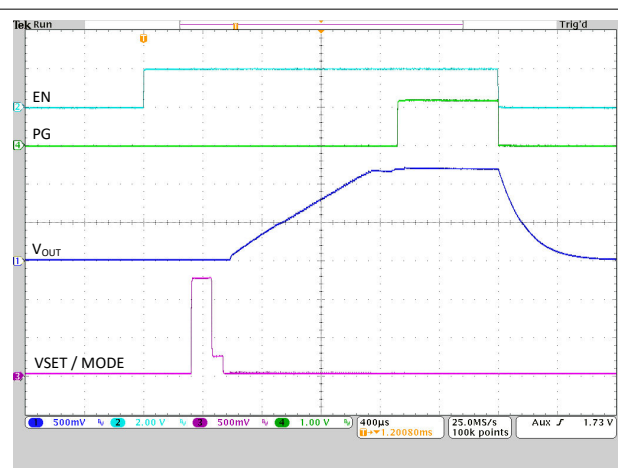
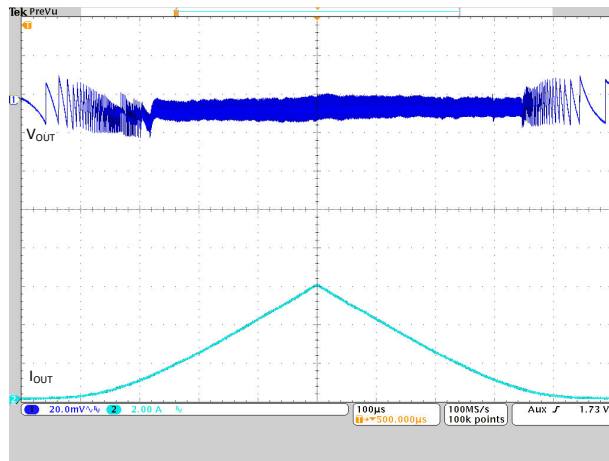
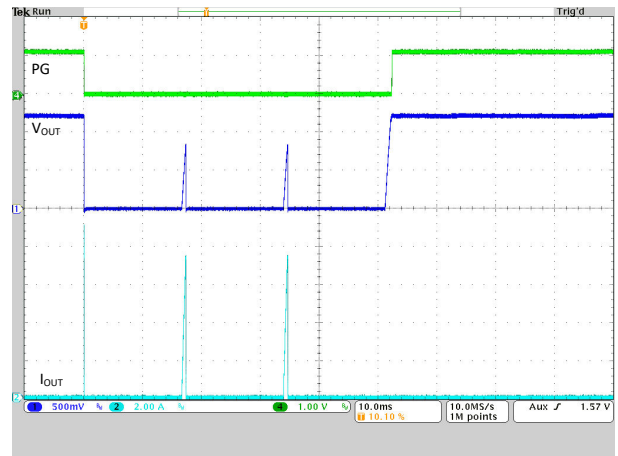

 $R_{VSET} = 56.2 \text{ k}\Omega$ $I_{OUT} = 0 \text{ A}$

图 8-35. Start-Up with No Load



$V_{IN} = 5.0\text{ V}$ $V_{OUT} = 1.2\text{ V}$ $C_{OUT} = 2 \times 22\mu\text{F}$

图 8-36. Load Sweep $I_{OUT} = 20\text{ mA} \rightarrow 6\text{ A}$



$R_{LOAD} = 100\text{ m}\Omega$ (during overload)

图 8-37. HICCUP Short-Circuit Protection

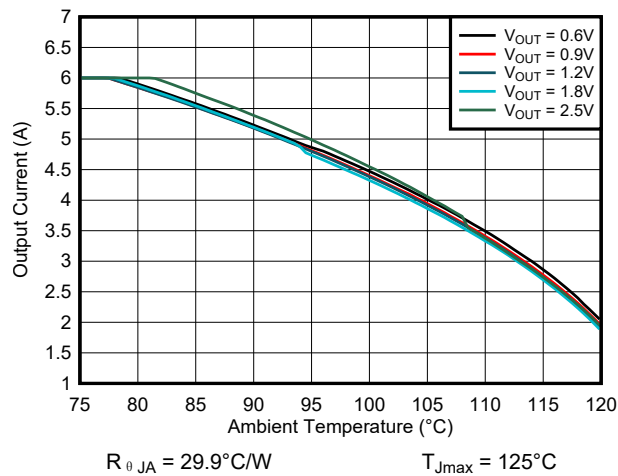


图 8-38. Safe Operating Area $V_{IN} = 3.3\text{-V}$
TPSM82866AA0PRCFR

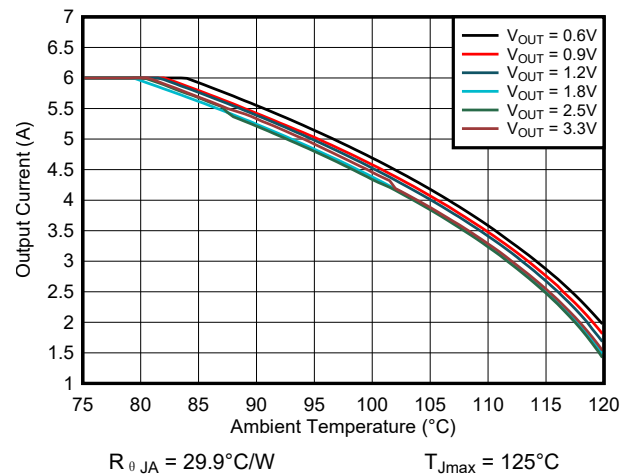


图 8-39. Safe Operating Area $V_{IN} = 5.0\text{-V}$
TPSM82866AA0PRCFR

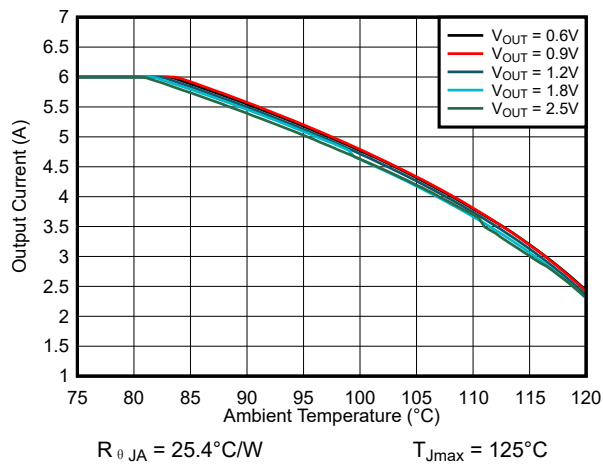


图 8-40. Safe Operating Area $V_{IN} = 3.3\text{-V}$
TPSM82866AA0SRDJR

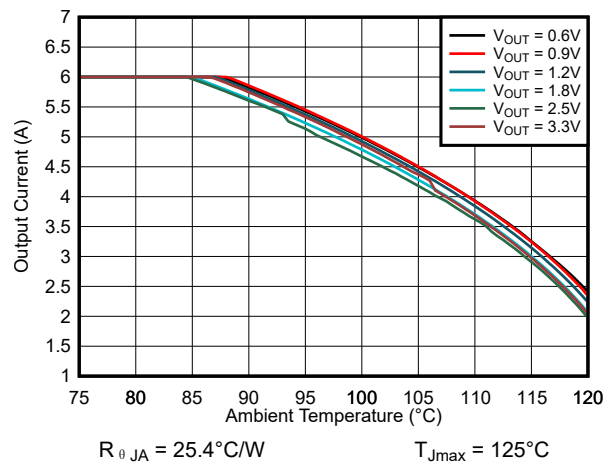


图 8-41. Safe Operating Area $V_{IN} = 5.0\text{-V}$
TPSM82866AA0SRDJR

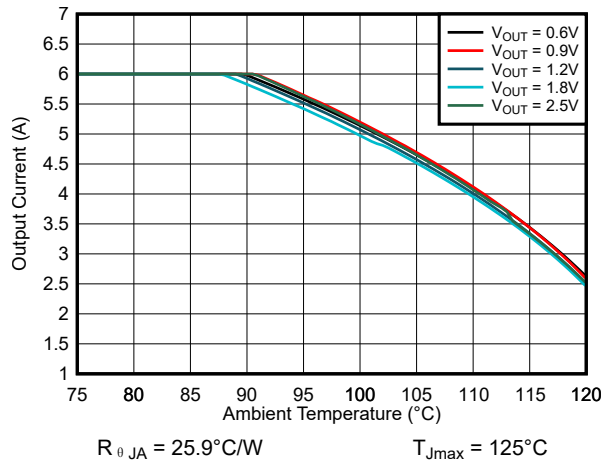


图 8-42. Safe Operating Area $V_{IN} = 3.3\text{-V}$
TPSM82866AA0HRDMR

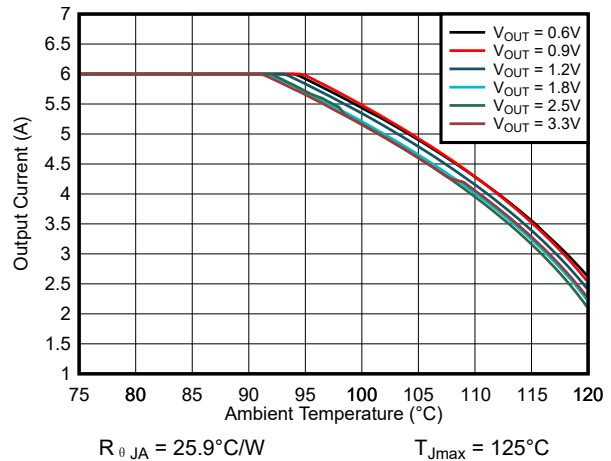


图 8-43. Safe Operating Area $V_{IN} = 5.0\text{-V}$
TPSM82866AA0HRDMR

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. The average input current of the TPSM8286xA is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

Make sure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10 mV/μs if the input voltage drops below V_{UVLO} .

8.4 Layout

8.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8286xA demands careful attention to make sure of best performance. A poor layout can lead to issues like the following:

- Bad line and load regulation
- Instability
- Increased EMI radiation
- Noise sensitivity

Refer to the [Five Steps to a Great PCB Layout for a Step-Down Converter Technical Brief](#) for a detailed discussion of general best practices. The following are specific recommendations for the TPSM8286xA:

- Place the input capacitor as close as possible to the VIN and PGND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and PGND pins avoiding vias.
- Place the output capacitor close to the VOUT and PGND pins and route directly avoiding vias.
- Place the FB resistors R1 and R2 close to the FB and AGND pins and place R4 close to the VSET/MODE pin to minimize noise pickup.
- The sense traces connected to the VOS pin is a signal trace. Take special care to avoid noise being induced. Keep the trace away from SW.
- To improve thermal performance, use GND vias under the exposed thermal pad. Directly connect the AGND and PGND pins to the exposed thermal pad with copper on the top PCB layer.

- Refer to 图 8-44 and 图 8-45 for an example of component placement, routing, and thermal design.
- The recommended land pattern for the TPSM8286xA is shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD) when some pins (such as VIN, VOUT, and PGND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

8.4.2 Layout Examples

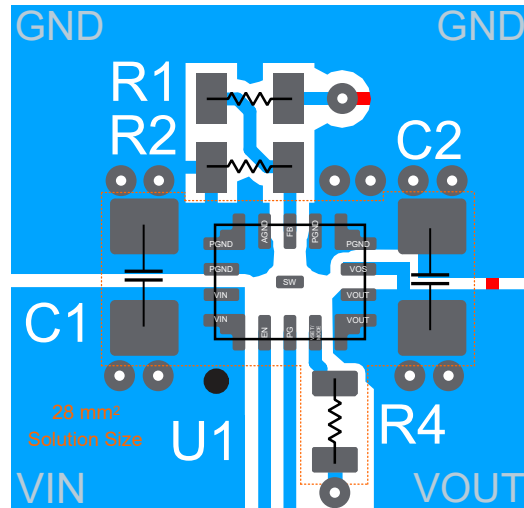


图 8-44. Layout Example RCF package

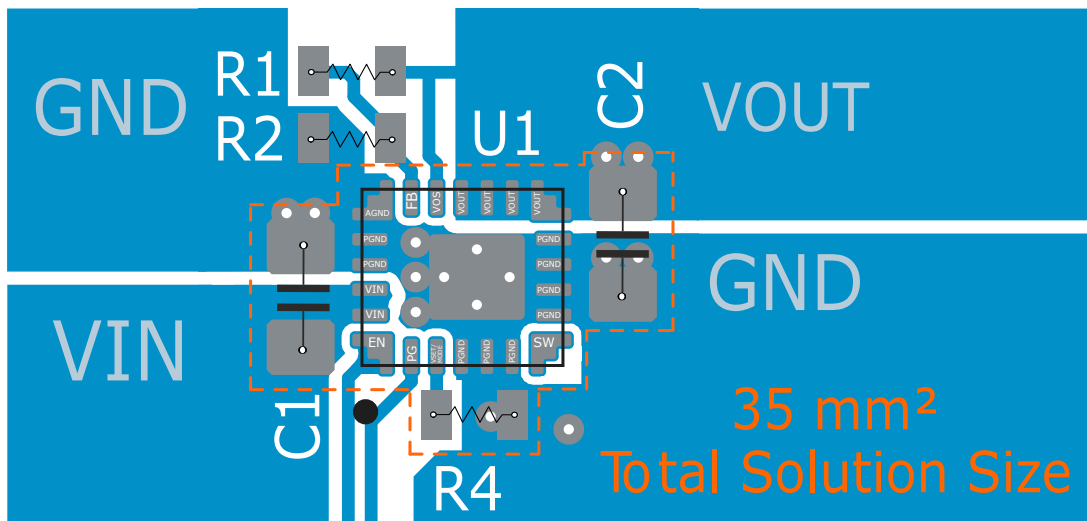


图 8-45. Layout Example RDJ and RDM package

8.4.2.1 Thermal Considerations

The TPSM8286xA power module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8286xA, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrate the required derating in maximum output current at high ambient temperatures. For more details on how to use the thermal parameters in real applications, see the [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report](#) and [Semiconductor and IC Package Thermal Metrics Application Report](#).

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics Application Report](#)
- Texas Instruments, [Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies White Paper](#)
- Texas Instruments, [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief](#)
- Texas Instruments, [Simplify Low EMI Design With Power Modules White Paper](#)

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.5 Trademarks

MagPack™ and TI E2E™ are trademarks of Texas Instruments.

所有商标均为其各自所有者的财产。

9.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2024) to Revision D (November 2024)	Page
---	------

- | | |
|--|---|
| • Changed TPSM82866AA0PRCFR from Advance Information to Production Data..... | 3 |
|--|---|

Changes from Revision B (November 2022) to Revision C (June 2024)	Page
---	------

- | | |
|---|---|
| • Added TPSM82864AA0PRCFR (preview), TPSM82864BA0PRCFR (preview), TPSM82866AA0PRCFR (advance information), and TPSM82866BA0PRCFR (preview) to the data sheet..... | 3 |
|---|---|

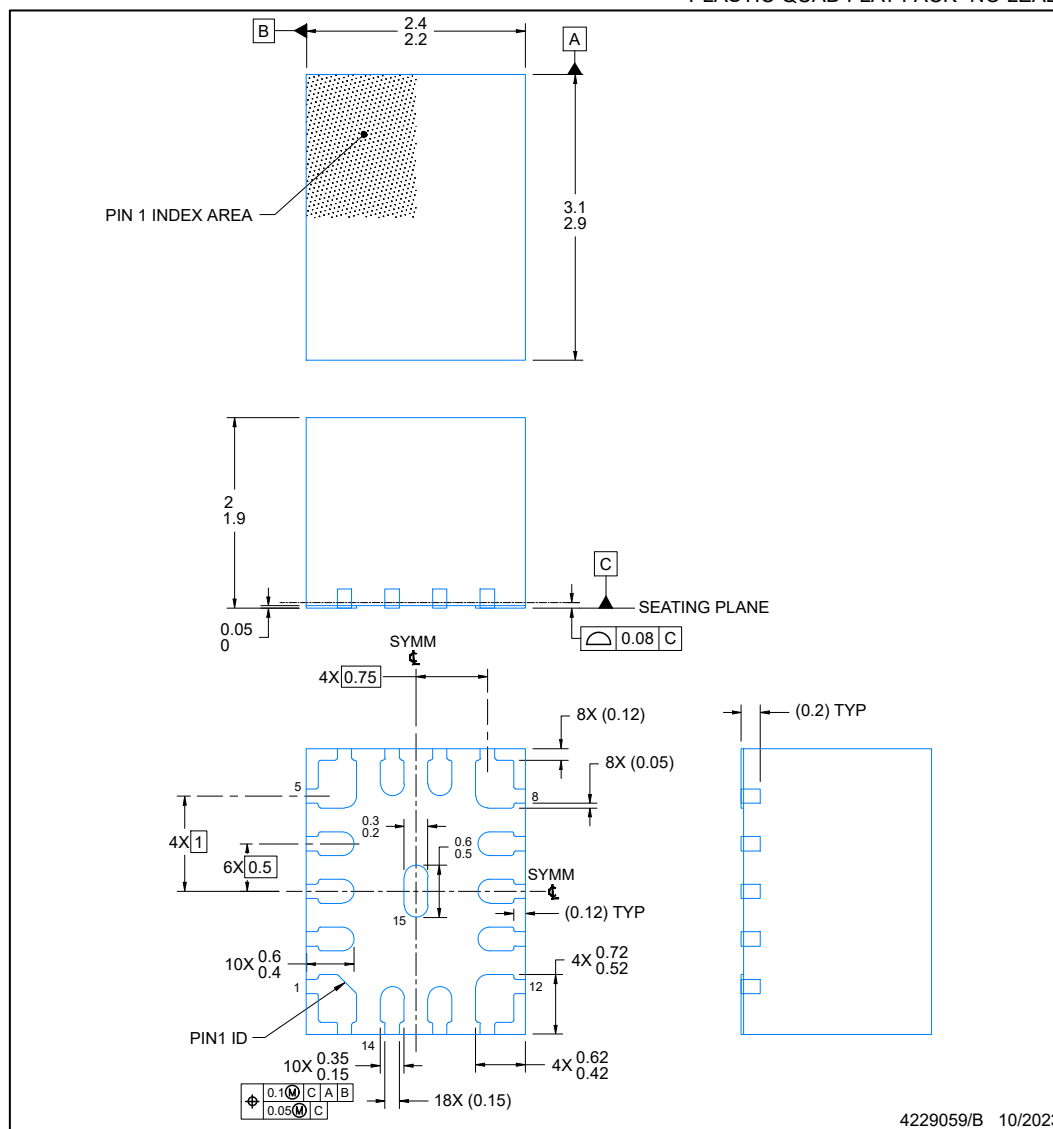
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RCF0015A QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

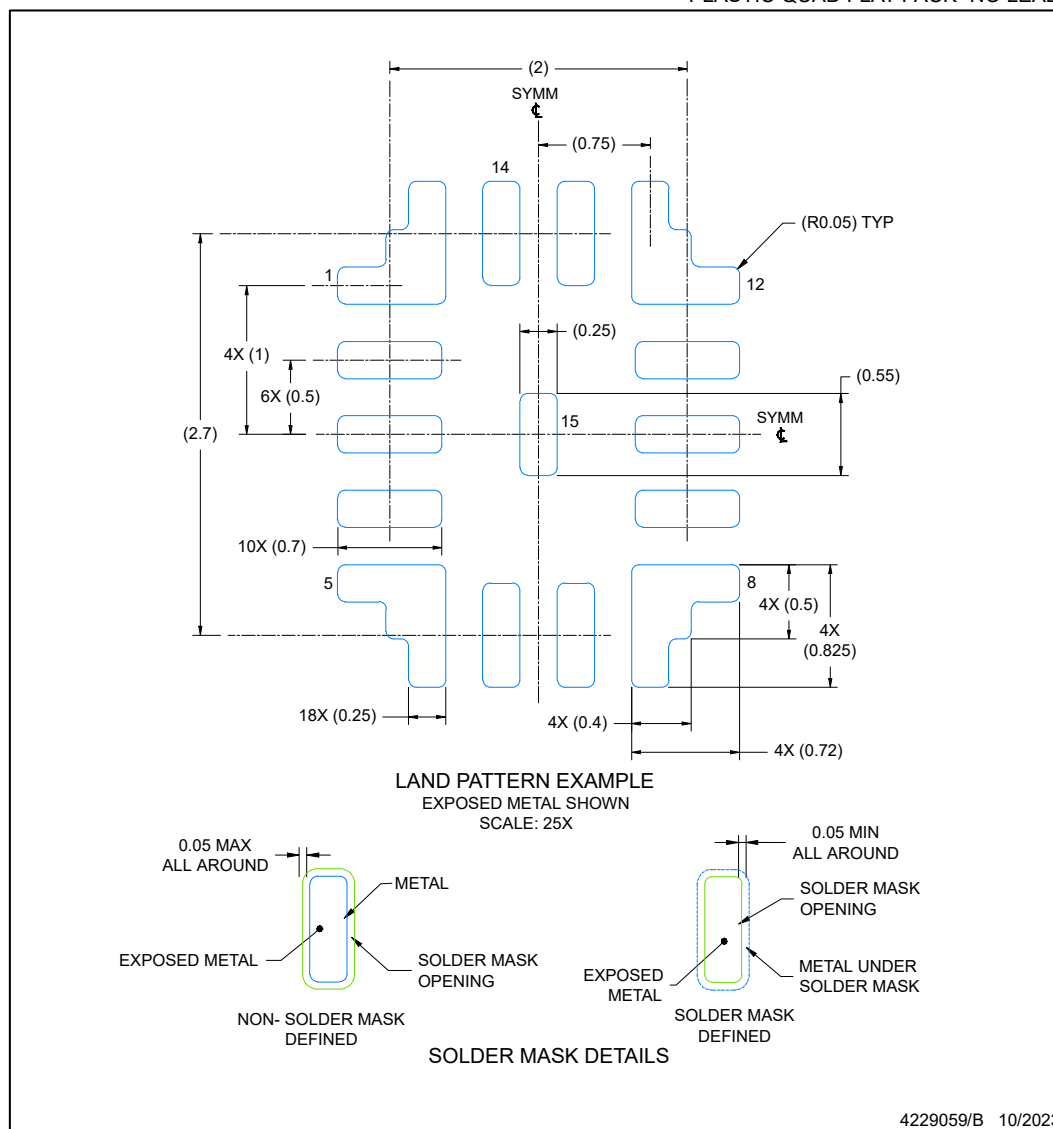


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT**RCF0015A****QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

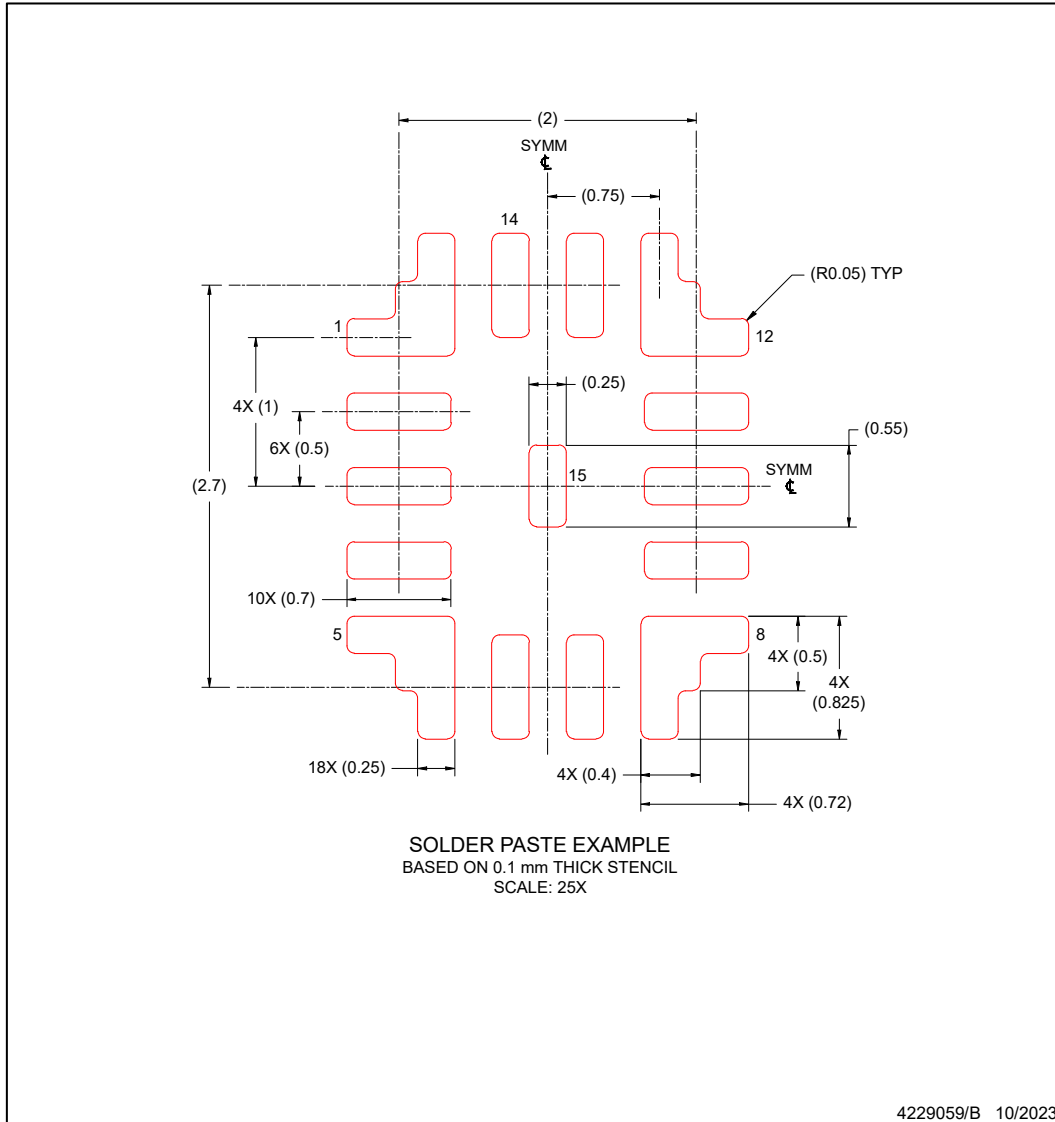
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RCF0015A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M8864AA0SRDJRG4	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM864AA0S
M8864AA0SRDJRG4.A	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM864AA0S
M8866AA0HRDMRG4	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0H
M8866AA0HRDMRG4.A	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0H
M8866AA0SRDJRG4	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0S
M8866AA0SRDJRG4.A	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0S
TPSM82864AA0HRDMR	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-			-40 to 125	TM864AA0H
TPSM82864AA0HRDMR.A	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM864AA0H
TPSM82864AA0SRDJR	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-			-40 to 125	TM864AA0S
TPSM82864AA0SRDJR.A	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM864AA0S
TPSM82866AA0HRDMR	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-			-40 to 125	TM866AA0H
TPSM82866AA0HRDMR.A	Active	Production	B0QFN (RDM) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0H
TPSM82866AA0PRCFR	Active	Production	QFN-FCMOD (RCF) 15	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	T8866A
TPSM82866AA0PRCFR.A	Active	Production	QFN-FCMOD (RCF) 15	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	T8866A
TPSM82866AA0PRCFR.B	Active	Production	QFN-FCMOD (RCF) 15	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM82866AA0SRDJR	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-			-40 to 125	TM866AA0S
TPSM82866AA0SRDJR.A	Active	Production	B0QFN (RDJ) 23	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	TM866AA0S
XPSM82866AA0PRCFR	Active	Preproduction	QFN-FCMOD (RCF) 15	2500 LARGE T&R	-			-40 to 125	
XPSM82866AA0PRCFR.A	Active	Preproduction	QFN-FCMOD (RCF) 15	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

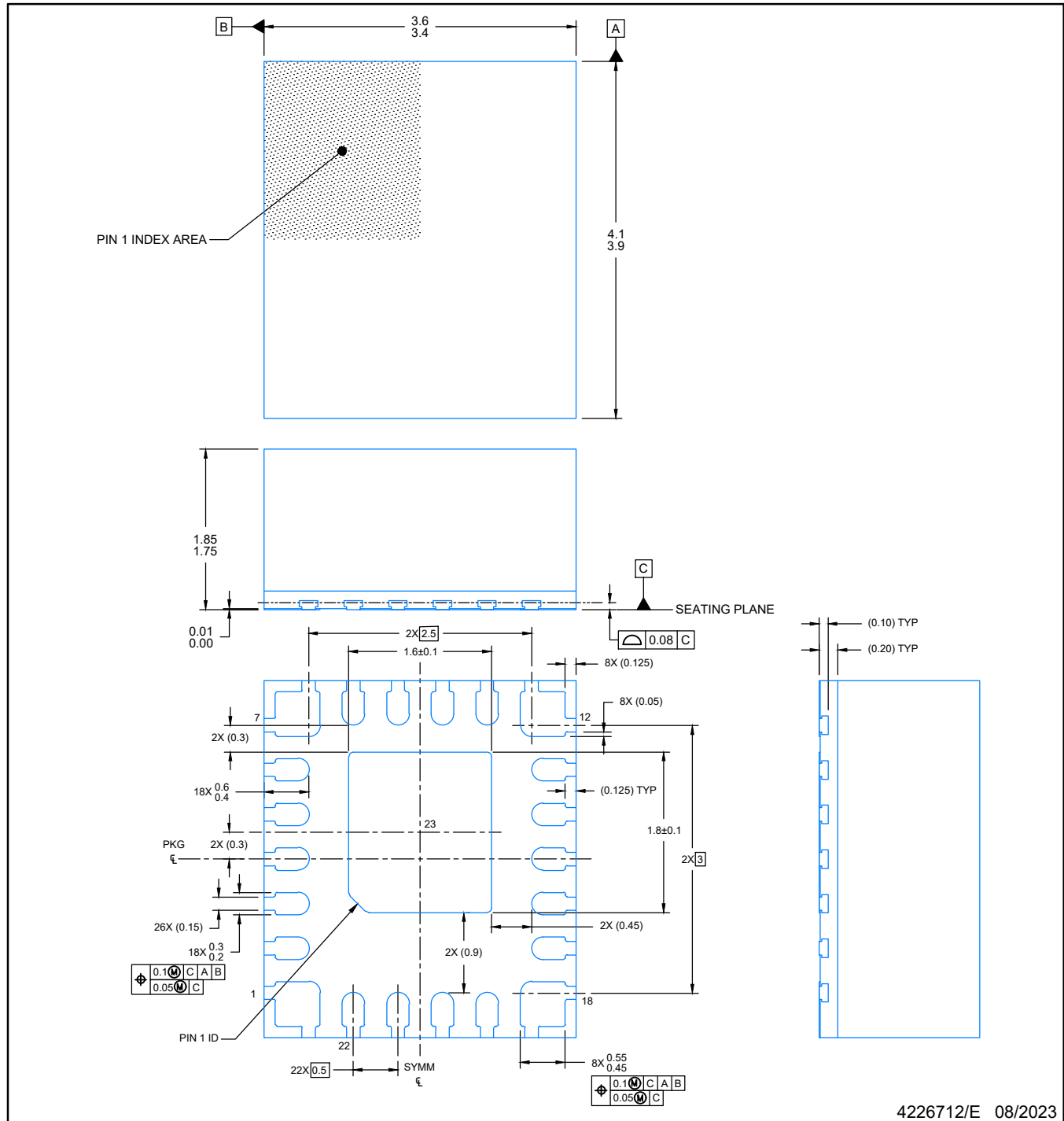
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM82866AA0PRCFR	QFN-FCMOD	RCF	15	2500	330.0	12.4	2.6	3.3	2.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM82866AA0PRCFR	QFN-FCMOD	RCF	15	2500	367.0	367.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

B0QFN - 1.85 mm max height

24-PIN PACKAGE

PKG

SYM

2X (2.5)

22X (0.5)

26X (0.25)

8X (0.5)

22

18

18X (0.7)

2X (0.3)

2X (3)

7

(R0.05) TYP

12

(Ø0.2) TYP

1.6

3.2

3.7

1.8

0.35

0.95

0.55

0.1

0.2

0.25

0.5

0.7

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

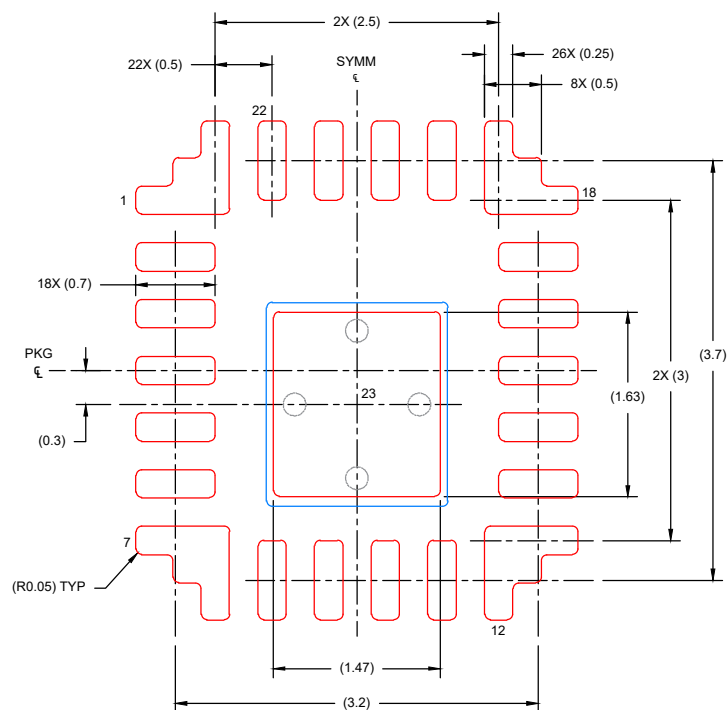
24

The diagram illustrates two PCB manufacturing processes:

- NON- SOLDER MASK DEFINED:** This process shows a rectangular area where the metal is exposed. The dimensions are specified as 0.05 MAX ALL AROUND. The labels include METAL, EXPOSED METAL, and SOLDER MASK OPENING.
- SOLDER MASK DEFINED:** This process shows a rectangular area where the metal is covered by solder mask. The dimensions are specified as 0.05 MAX ALL AROUND. The labels include SOLDER MASK OPENING, METAL UNDER SOLDER MASK, and EXPOSED METAL.

4226712/E 08/2023

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD:
83% PRINTED SOLDER COVERAGE BY AREA

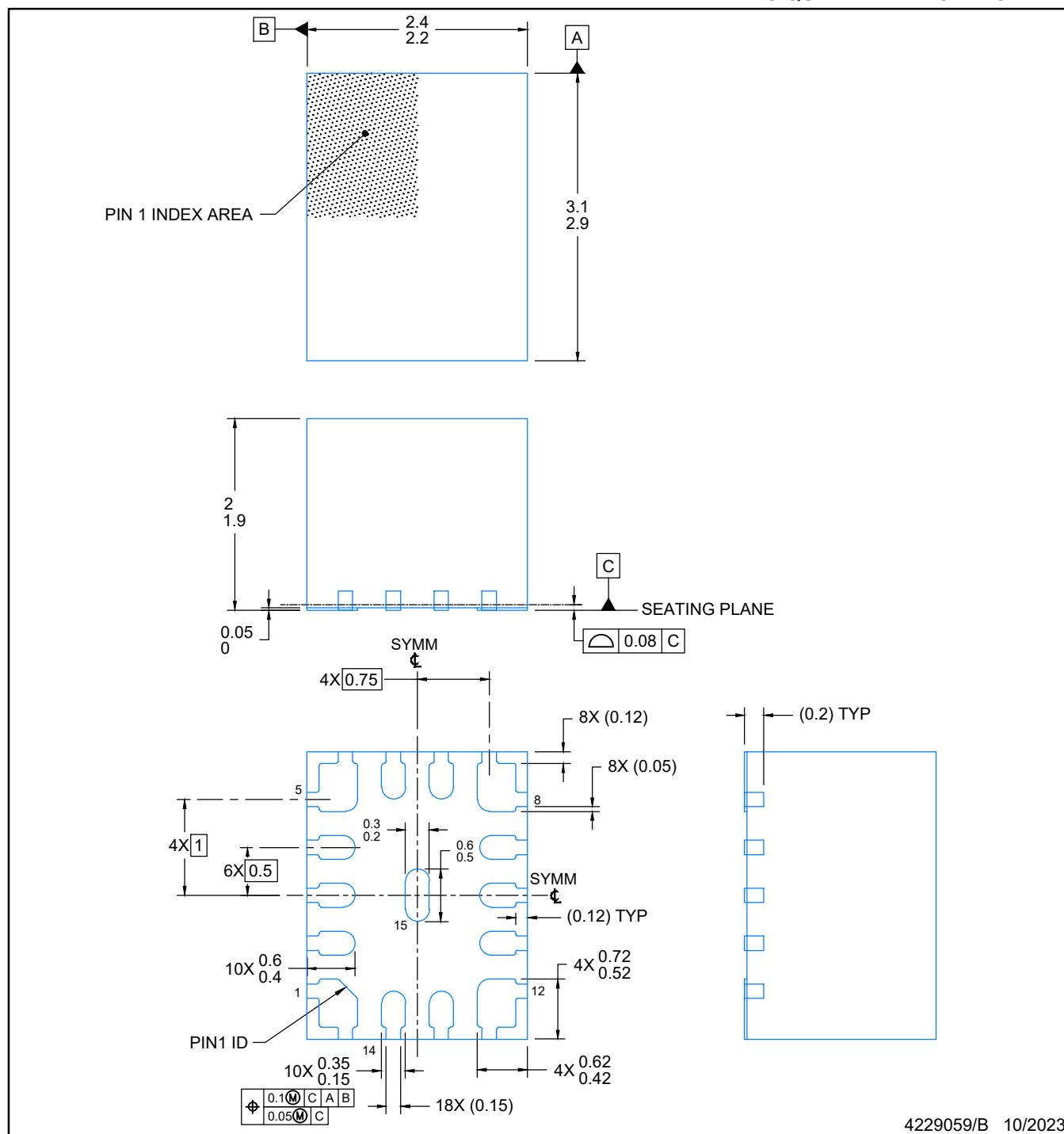
SCALE: 15X

4226712/E 08/2023

NOTES: (continued)

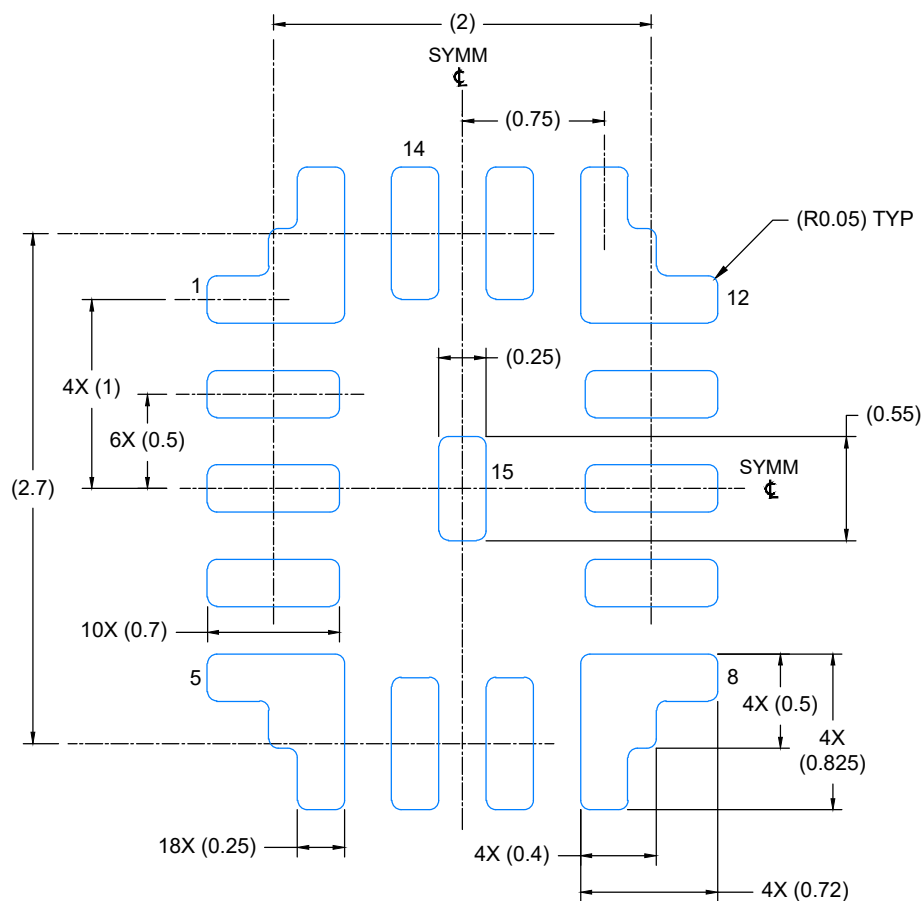
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

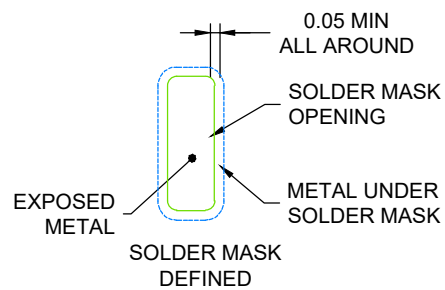
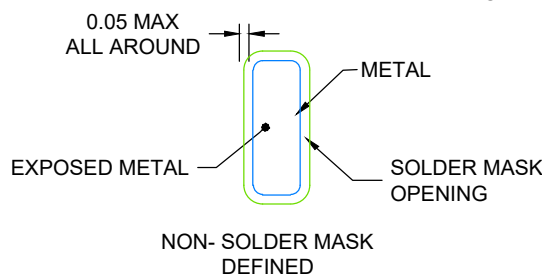
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 25X

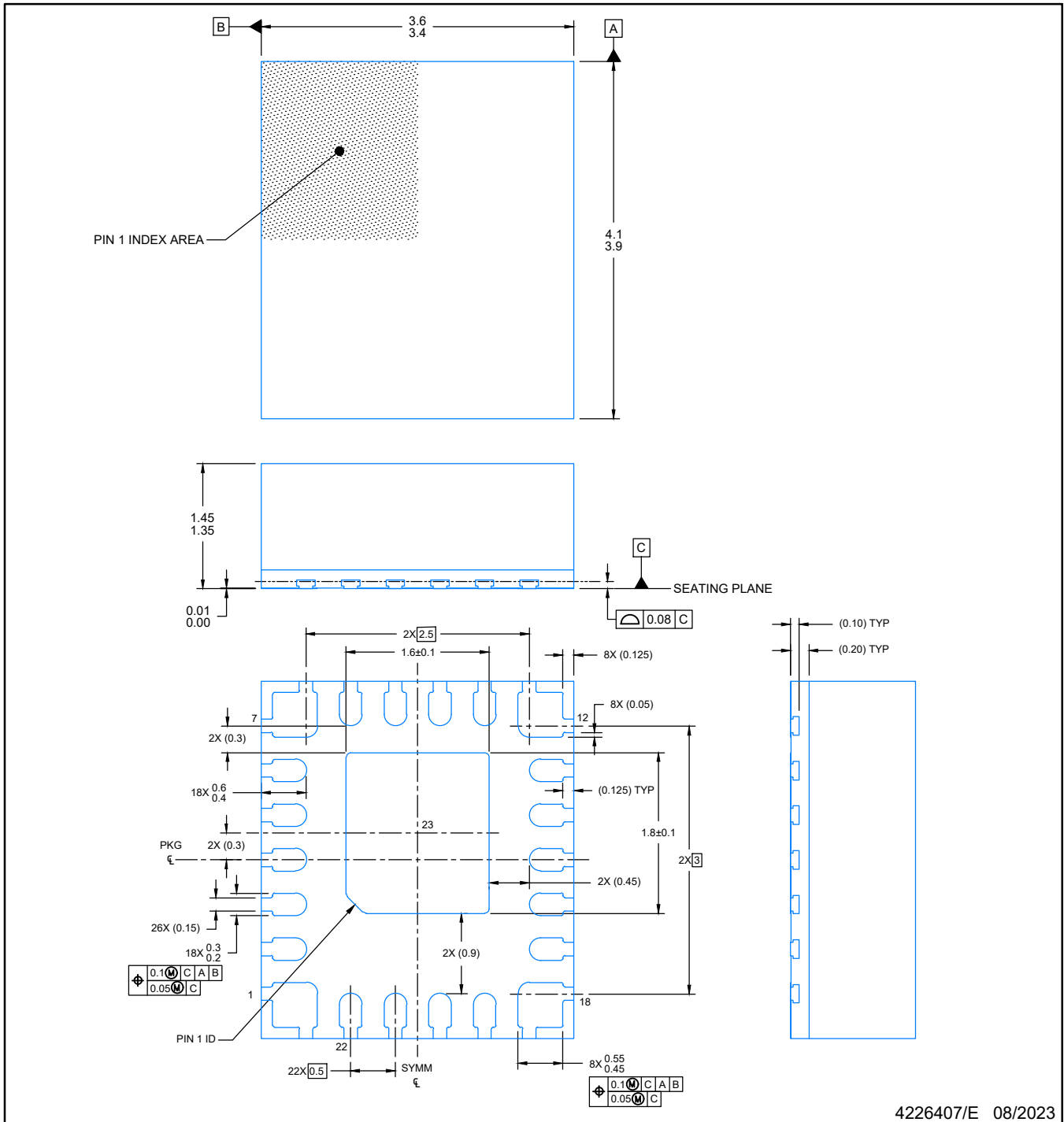


SOLDER MASK DETAILS

4229059/B 10/2023

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

B0QFN - 1.45 mm max height

24-PIN PACKAGE

PKG

SYM

2X (2.5)

22X (0.5)

26X (0.25)

8X (0.5)

22

18

18X (0.7)

2X (0.3)

2X (3)

7

(R0.05) TYP

12

(Ø0.2) TYP

1.6

3.2

3.7

1.8

0.35

0.95

0.55

0.1

0.2

0.25

0.5

0.7

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

85

86

87

88

89

90

91

92

93

94

95

96

97

98

99

100

101

102

103

104

105

106

107

108

109

110

111

112

113

114

115

116

117

118

119

120

121

122

123

124

125

126

127

128

129

130

131

132

133

134

135

136

137

138

139

140

141

142

143

144

145

146

147

148

149

150

151

152

153

154

155

156

157

158

159

160

161

162

163

164

165

166

167

168

169

170

171

172

173

174

175

176

177

178

179

180

181

182

183

184

185

186

187

188

189

190

191

192

193

194

195

196

197

198

199

200

201

202

203

204

205

206

207

208

209

210

211

212

213

214

215

216

217

218

219

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235

236

237

238

239

240

241

242

243

244

245

246

247

248

249

250

251

252

253

254

255

256

257

258

259

260

261

262

263

264

265

266

267

268

269

270

271

272

273

274

275

276

277

278

279

280

281

282

283

284

285

286

287

288

289

290

291

292

293

294

295

296

297

298

299

300

301

302

303

304

305

306

307

308

309

310

311

312

313

314

315

316

317

318

319

320

321

322

323

324

325

326

327

328

329

330

331

332

333

334

335

336

337

338

339

340

341

342

343

344

345

346

347

348

349

350

351

352

353

354

355

356

357

358

359

360

361

362

363

364

365

366

367

368

369

370

371

372

373

374

375

376

377

378

379

380

381

382

383

384

385

386

387

388

389

390

391

392

393

394

395

396

397

398

399

400

401

402

403

404

405

406

407

408

409

410

411

412

413

414

415

416

417

418

419

420

421

422

423

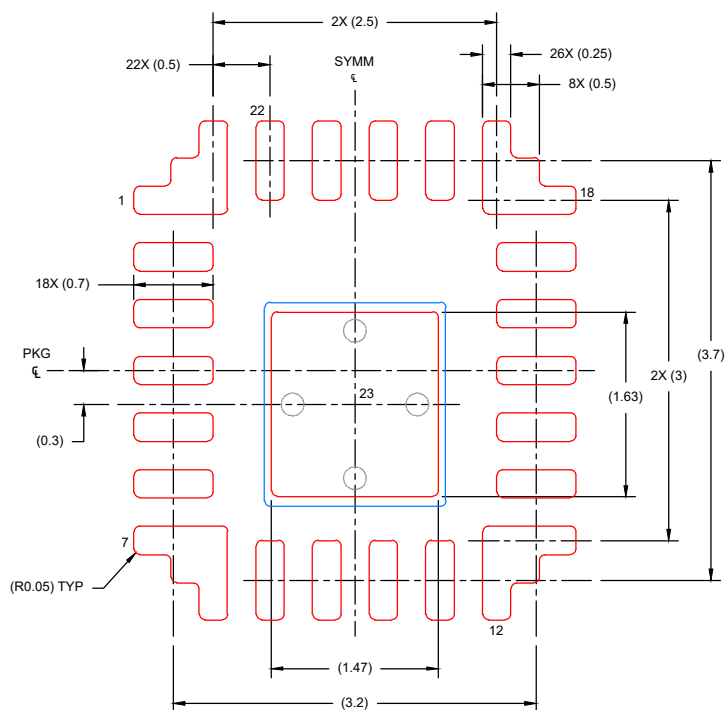
424

The diagram illustrates two types of microstructures: Non-Solder Mask Defined and Solder Mask Defined.

- Non-Solder Mask Defined:** This structure features a central **EXPOSED METAL** pad. It is surrounded by a **SOLDER MASK OPENING** (indicated by a green outline) and an outer **METAL** layer (indicated by a blue outline). A dimension line indicates a **0.05 MAX ALL AROUND** gap between the metal pad and the surrounding metal layer.
- Solder Mask Defined:** This structure features a central **EXPOSED METAL** pad. It is surrounded by a **SOLDER MASK OPENING** (indicated by a green outline) and an outer **METAL UNDER SOLDER MASK** layer (indicated by a blue outline). A dimension line indicates a **0.05 MAX ALL AROUND** gap between the metal pad and the surrounding metal layer.

4226407/E 08/2023

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD:
83% PRINTED SOLDER COVERAGE BY AREA

SCALE: 15X

4226407/E 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月