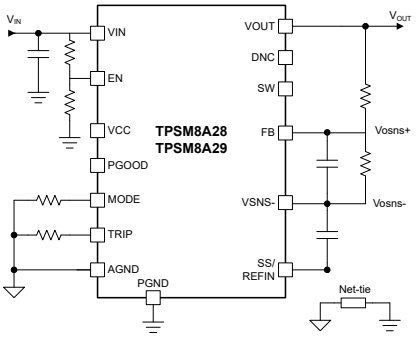
TPSM8A28、TPSM8A29 具有差分遥感功能的 2.7V 至 16V 输入、12A、 15A 降压电源模块

1 特性

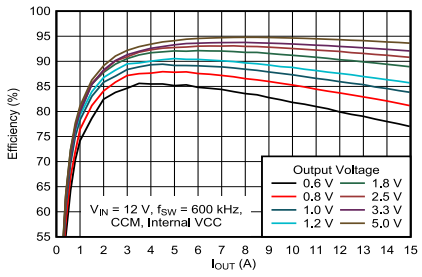
- TPSM8A28：输入电压范围为 3V 至 16V，电流高达 12A
- TPSM8A29：输入电压范围为 4V 至 16V，电流高达 15A
- 输入范围为 2.7V 至 16V 时，外部偏压范围为 4.75 V 至 5.3 V
- 输出电压范围：0.6V 至 5.5V
- 集成 MOSFET、电感器和基本无源器件
- 在 D-CAP3™ 控制模式下可提供快速负载阶跃响应
- 支持所有陶瓷输出电容器
- 0.6V 基准电压，±1% 容差（在 –40°C 至 +125°C 的结温范围内）
- 可选 FCCM 或自动跳跃 Eco-mode™ 可实现较高的轻负载效率
- 通过 R_{TRIP} 实现可编程电流限制
- 引脚可选开关频率：600kHz、800kHz、1MHz
- 可实现高输出精度的差分遥感功能
- 可编程软启动时间
- 外部基准输入，用于跟踪
- 预偏置启动功能
- 开漏电源正常状态输出
- 在发生 OC 和 UV 故障时进入断续模式，在发生 OV 故障时进入闭锁模式
- 6.5mm × 7.5mm × 4.0mm，RDG 封装
- 完全符合 RoHS 标准，无需豁免

2 应用

- 数据中心交换机
- 核心路由器
- 单板计算机
- 光学模块



简化版原理图



效率图

3 说明

TPSM8A28 和 TPSM8A29 降压电源模块具有小尺寸和高效率。此模块系列包含集成电感器和基本无源器件，不需要外部补偿，可更大程度地减小解决方案尺寸。

特性包括差分遥感功能、高性能集成 MOSFET、高精度 0.6V 电压基准、D-CAP3™ 控制模式、可选跳跃模式和可编程软启动。

TPSM8A28 和 TPSM8A29 无铅、完全符合 RoHS 标准，无需豁免。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPSM8A28	B3QFN-RDG	6.5mm × 7.5mm
TPSM8A29	B3QFN-RDG	6.5mm × 7.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2021) to Revision A (November 2021)	Page
• 将 TPSM8A29 从“预告信息”更改为“量产数据”并添加了 TPSM8A28	1

5 Pin Configuration and Functions

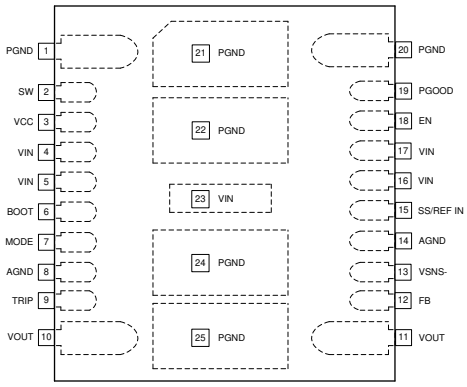


图 5-1. 25-Pin B3QFN RDG Package (Top View)

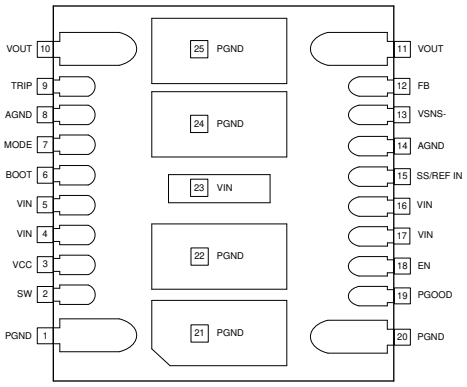


图 5-2. 25-Pin B3QFN RDG Package (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PGND	1, 20, 21, 22, 24, 25	G	Power ground of internal low-side MOSFET
SW	2	O	Output switching terminal of the power converter. No external connection needed. Do not connect.
VCC	3	I/O	Internal 4.5-V LDO output. Float or connect to an external power supply between 4.75 V and 5.3 V to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. A 1-μF bypass capacitor is built in. No external bypass capacitors are required.
VIN	4, 5, 16, 17, 23	P	Power-supply input pins for the integrated power MOSFET pair and the internal LDO. Place the decoupling input capacitors from the VIN pins to PGND pins as close as possible.
BOOT	6	I/O	Supply rail for the high-side gate driver. A boot capacitor is integrated inside module. No external connection is needed. Do not connect.
MODE	7	I	The MODE pin sets Forced continuous-conduction mode (FCCM) or Skip-mode operation. It also selects the operating frequency by connecting a resistor from the MODE pin to AGND pin. ±1% tolerance resistor is recommended. See 表 7-1 for details.
AGND	8, 14	G	Ground pin. Reference point for the internal control circuits
TRIP	9	I/O	Current limit setting pin. Connect a resistor to AGND to set the current limit trip point. ±1% tolerance resistor is highly recommended. See 节 7.3.9 for details on the OCL setting.
VOUT	10, 11	O	These pins are connected to the output terminal of inductor. Connect these pins to output bypass capacitors.
FB	12	I	Output voltage feedback input. A resistor divider from the V_{OUT} to VSNS – (tapped to FB pin) sets the output voltage.
VSNS –	13	I	The return connection for a remote voltage sensing configuration. It is also used as ground for the internal reference. Short to AGND for a single-end sense configuration.
SS/REFIN	15	I/O	Dual-function pin. Soft-start function: Connecting a capacitor to the VSNS – pin programs the soft-start time. Minimum soft-start time (1.5 ms) is fixed internally. REFIN function: The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. The internal reference voltage can be overridden by an external DC voltage source on this pin for tracking application.
EN	18	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating the EN pin before start-up disables the converter. The recommended operating condition for EN pin is maximum 5.5 V. *Do not* connect the EN pin to the VIN pin directly.
PGOOD	19	O	Open-drain power-good status signal. When the FB voltage moves outside the specified limits, PGOOD goes low after a 2-μs delay.

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage(2)	VIN		–0.3	18	V
	SW	DC	–0.3	18	
		Transient < 10 ns	–3.0	22	
		Transient < 2 ns	–3.0	22	
	BOOT		–0.3	24	
	VSNS –		–0.3	+0.3	
	TRIP, MODE, SS/REFIN, FB, EN		–0.3	6	
Output voltage	PGOOD		–0.3	6	
	VCC		–0.3	6	
Mechanical shock	Mil-STD-883H, Method 2002.5, 1 msec, 1/2 sine, mounted			500	G
Mechanical vibration	Mil-STD-883H, Method 2007.3, 20 to 2000 Hz			20	G
Operating junction temperature, T_J			–40	125	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN with valid external bias on VCC	2.7	16	V
	VIN with internal LDO, TPSM8A28	3.0	16	
	VIN with internal LDO, TPSM8A29	4.0	16	
	External reference to SS/REFIN	0.5	1.2	
	External bias range for VCC	4.75	5.3	
	VIN to enable the converter with internal LDO	3.3		
	TRIP, MODE, FB, EN	–0.1	5.5	
	VSNS – (refer to AGND)	–50	50	mV
Output voltage	PGOOD	–0.1	5.5	V
	VCC	4.5	5.3	
Input current	PGOOD	0	10	mA
Junction temperature, T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8A28 TPSM8A29 RDG (B3QFN) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, VCC = Internal 4.5V LDO, both TPSM8A29 and TPSM8A28 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{Q_VIN}	VIN operating nonswitching supply current	V_{EN} = 2 V, V_{FB} = 0.65 V, V_{IN} = 12 V, no external bias on the VCC pin		680	850	µA
I_{SD_VIN}	VIN shutdown supply current	V_{EN} = 0 V, V_{IN} =12 V, no external bias on the VCC pin		9.5	20	µA
I_{Q_VCC}	VCC quiescent current	T_J = 25°C, V_{EN} = 2 V, V_{FB} = 0.65 V, V_{IN} = 5 V, 5.0 V external bias on the VCC pin		680	820	µA
I_{SD_VCC}	VCC shutdown current	T_J = 25°C, V_{EN} = 0 V, V_{IN} = 0 V, 5.0 V external bias on the VCC pin		75	85	µA
REFERENCE VOLTAGE						
V_{INTREF}	Internal REF voltage	T_J = 25°C		600		mV
	Internal REF voltage tolerance	T_J = 0°C to 70°C	597		603	mV
	Internal REF voltage tolerance	T_J = –40°C to 125°C	594		606	mV
I_{FB}	FB input current	V_{FB} = V_{INTREF}		50	100	nA
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{IN} = 12 V, VCC = internal LDO, Vsw = 0.5 V, power conversion disabled		70		Ω
SWITCHING FREQUENCY						
f_{SW}	VO switching frequency, FCCM operation	V_{IN} = 12 V, V_{OUT} = 1.2 V, R_{MODE} = 0 Ω to AGND	490	620	750	kHz
		V_{IN} = 12 V, V_{OUT} = 1.2 V, R_{MODE} = 30.1 kΩ to AGND	720	800	880	
		V_{IN} = 12 V, V_{OUT} = 1.2 V, R_{MODE} = 60.4 kΩ to AGND	840	1000	1250	
$t_{ON(min)}$	Minimum on time	T_J = 25°C(1)		70	85	ns
$t_{OFF(min)}$	Minimum off time	T_J = 25°C, HS FET gate falling to rising(1)			220	ns
ENABLE						
V_{ENH}	EN enable threshold voltage (rising)		1.17	1.22	1.27	V
V_{ENL}	EN disable threshold voltage (falling)		0.97	1.02	1.07	V
V_{ENHYST}	EN hysteresis voltage			0.2		V
V_{ENLEAK}	EN input leakage current	V_{EN} = V		0.5	5	µA
	EN internal pulldown resistance	EN pin to AGND. EN floating disables the converter.		6500		kΩ
INTERNAL VCC LDO						
VCC	Internal LDO output voltage	V_{IN} = 12 V, I_{LOAD} = 2 mA	4.32	4.5	4.68	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, VCC = Internal 4.5V LDO, both TPSM8A29 and TPSM8A28 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC_{UVLO}	VCC undervoltage-lockout (UVLO) threshold voltage	VCC rising	2.80	2.87	2.94	V
		VCC falling	2.62	2.7	2.77	V
VCC_{UVLO}	VCC undervoltage-lockout (UVLO) threshold voltage	VCC hysteresis		0.17		V
VCC_{DO}	LDO low-droop dropout voltage	V_{IN} = 3.0 V, I_{VCC_LOAD} = 2 mA, T_J = 25°C		62	75	mV
	LDO overcurrent limit	All VINs, all temperature		105	158	mA
STARTUP						
t_{SS}	Soft-start time	V_O rising from 0 V to 95% of final setpoint, $C_{SS/REFIN}$ = open	1	1.5		ms
	SS/REFIN sourcing current	$V_{SS/REFIN}$ = 0 V		36		µA
	SS/REFIN sinking current	$V_{SS/REFIN}$ = 1 V		12		µA
	EN to first switching delay, internal LDO	The delay from EN goes high to the first SW rising edge with internal LDO configuration. CVCC = 2.2 µF. CSS/REFIN = 220 nF		0.93	2	ms
	EN to first switching delay, external VCC bias	The delay from EN goes high to the first SW rising edge with external VCC bias configuration. VCC bias must reach regulation before EN ramp up. CSS/REFIN = 220 nF.		550	900	µs
PGOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	FB rising, PGOOD low to high	89%	92.5%	95%	
		FB rising, PGOOD high to low	113%	116%	119%	
		FB falling, PGOOD high to low	77%	80%	83%	
V_{PGTH}	OOB (out-of-bounds) threshold	FB rising, PGOOD stays high	103%	105.5%	108%	
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.4 V, V_{IN} = 12 V, VCC = Internal LDO			25	mA
I_{PG}	PGOOD low-level output voltage	I_{PGOOD} = 5.5 mA, V_{IN} = 12 V, VCC = internal LDO			400	mV
t_{PG_delay}	PGOOD delay time	Delay for PGOOD from low to high		1.0	1.4	ms
		Delay for PGOOD from high to low		0.5	5	µs
I_{PG_lkg}	PGOOD leakage current when pulled high	T_J = 25°C, V_{PGOOD} = 3.3 V, V_{FB} = V_{INTREF}			5	µA
	PGOOD clamp low-level output voltage	V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 100-kΩ resistor		710	850	mV
		V_{IN} = 0 V, VCC = 0 V, V_{EN} = 0 V, PGOOD pulled up to 3.3 V through a 10-kΩ resistor		850	1000	mV
	Minimum VCC for valid PGOOD output				1.5	V
OVERCURRENT PROTECTION						
R_{TRIP}	TRIP pin resistance range	TPSM8A28	4.02		14.7	kΩ
R_{TRIP}	TRIP pin resistance range	TPSM8A29	0		14.7	kΩ
I_{OCL}	Current limit threshold, TPSM8A29 only	Valley current on LS FET, 0 kΩ ≤ R_{TRIP} ≤ 3.3 kΩ TPSM8A29 only	14.8	18.4	21.7	A
I_{OCL}	Current limit threshold	Valley current on LS FET, R_{TRIP} = 4.02 kΩ	12.0	14.2	16.3	A
I_{OCL}	Current limit threshold	Valley current on LS FET, R_{TRIP} = 4.99 kΩ	9.9	12.0	14.1	A
I_{OCL}	Current limit threshold	Valley current on LS FET, R_{TRIP} = 10 kΩ	3.9	6.0	8.1	A
K_{OCL}	K_{OCL} for R_{TRIP} equation			60000		A Ω
I_{NOCL}	Negative current limit threshold	All VINs	–12	–10	–8	A

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, VCC = Internal 4.5V LDO, both TPSM8A29 and TPSM8A28 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ZC}	Zero-cross detection current threshold, open loop	V_{IN} = 12 V, VCC = Internal LDO		400		mA
UVLO						
VIN_{UVLO}	VIN UVLO threshold voltage	Rising	2.1	2.4	2.7	V
		Falling	1.55	1.85	2.15	V
V_{OVP}	Overvoltage-protection (OVP) threshold voltage		113%	116%	119%	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Temperature rising		165		°C
	Thermal shutdown hysteresis(1)			30		°C

(1) Specified by design. Not production tested.

6.6 Typical Characteristics

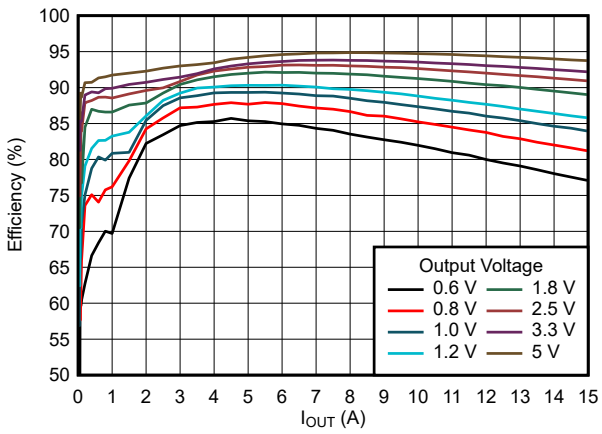


图 6-1. Efficiency vs Output Current, 12 V_{IN}, 600 KHz, Skip Mode, Internal VCC LDO

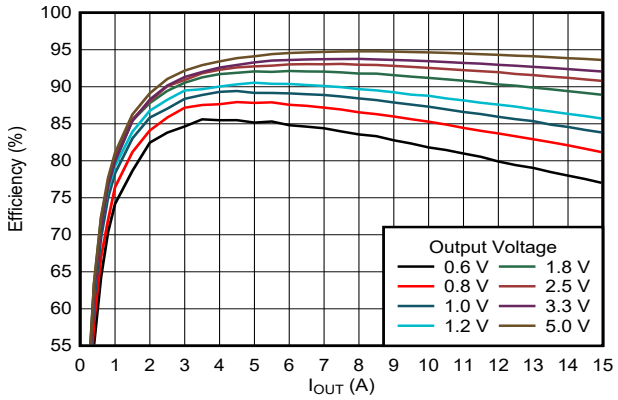


图 6-2. Efficiency vs Output Current, 12 V_{IN}, 600 KHz, FCCM, Internal VCC LDO

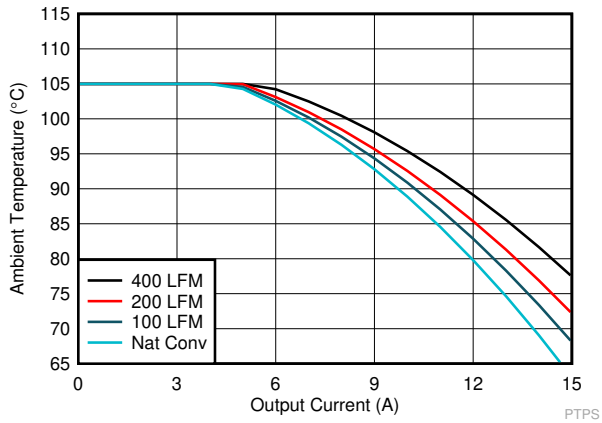


图 6-3. SOA, 12 V 1$Vout_{IN}$, 600 KHz, FCCM, Internal VCC LDO

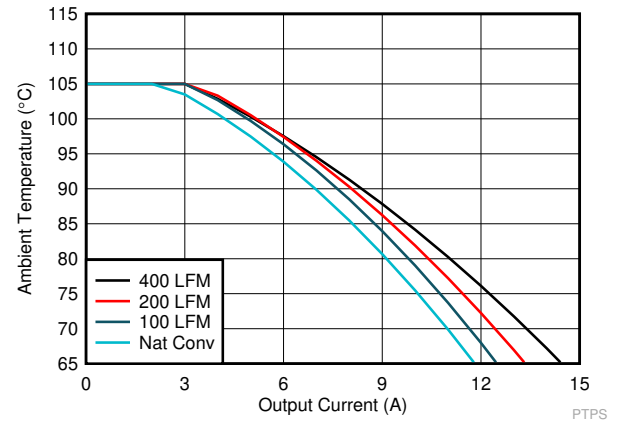


图 6-4. SOA, 12 V 3.3$Vout_{IN}$, 600 KHz, FCCM, Internal VCC LDO

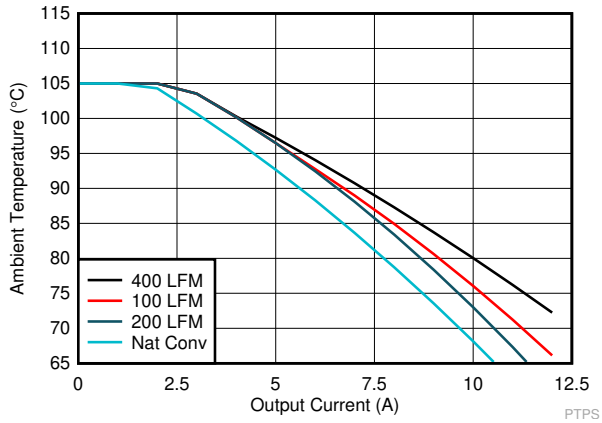


图 6-5. SOA, 12 V 5.0$Vout_{IN}$, 600 KHz, FCCM, Internal VCC LDO

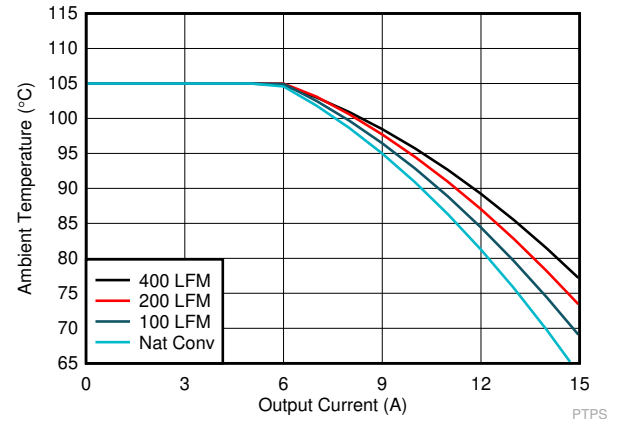


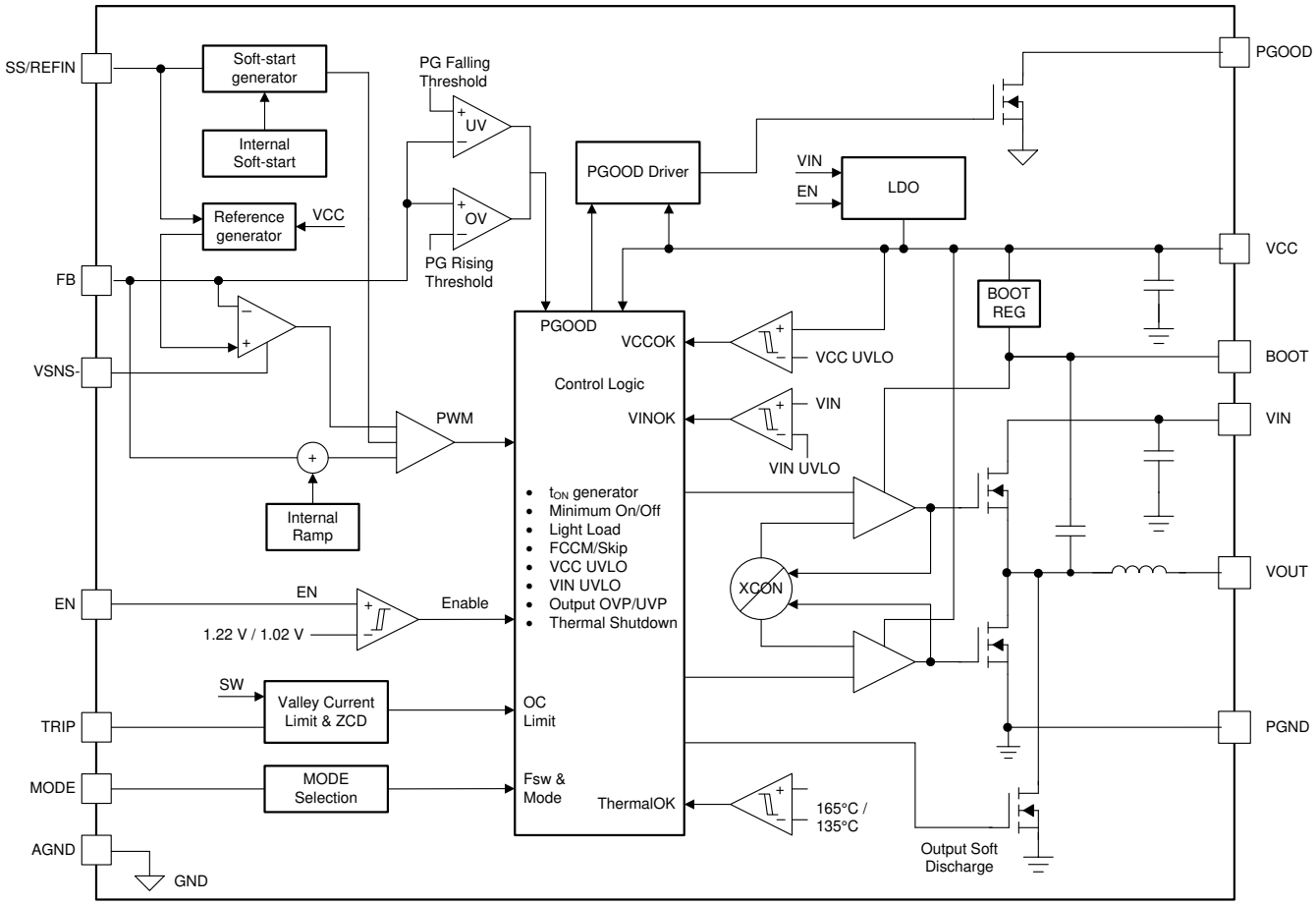
图 6-6. SOA, 5Vin 1.0$Vout_{IN}$, 600 KHz, FCCM, Internal VCC LDO

7 Detailed Description

7.1 Overview

The TPSM8A28 and TPSM8A29 power modules feature high effcieincy and small footprint. These devices are suitable for low voltage point-of-load applications up to 15 A. The conversion input voltage ranges from 2.7 V to 16 V, and the external VCC input voltage ranges from 4.75 V to 5.3 V, and output voltage ranges from 0.6 V to 5.5 V. These power modules uses D-CAP3™ mode control combined with adaptive on-time architecture. The D-CAP3™ mode uses emulated current information to control the modulation and tracks the preset switching frequency over a wide range of input and output voltages. Advantages of this control scheme is that it does not require a phase-compensation network outside, which makes the device easy-to-use and also allows low external component count. Further advantage of this control scheme is that it supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low-ESR polymer capacitor). It also adjusts switching frequency as needed during load-step transient.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal VCC LDO and Using External Bias on VCC Pin

The TPSM8A28 and TPSM8A29 power modules have internal 4.5-V LDO that takes input from VIN rail and output to VCC. When the V_{IN} voltage rises above the VIN_{UVLO} rising threshold, and the EN voltage rises above the enable threshold (typically 1.22 V), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

The VCC pin has an internal bypass capacitor integrated inside the module and does not require external bypassing. An external bias that is above the output voltage of the internal LDO can override the internal LDO. This enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

The following are considerations when using an external bias on the VCC pin:

- When the external bias is applied on the VCC pin early enough (for example, before EN signal comes in), the internal LDO is always forced off and the internal analog circuits has a stable power supply rail at their power enable.
- (Not recommended) If the external bias is applied on the VCC pin late (for example, after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. It is important to understand that an external discharge path on the VCC pin, which can pull a current higher than the current limit of the internal LDO from the VCC pin, can potentially turn off VCC LDO thereby shutting down the converter output.
- A good power-up sequence is when at least the VIN UVLO rising threshold or EN rising threshold is satisfied later than the VCC UVLO rising threshold. For example, VIN applied first, then the external bias applied, and then EN signal goes high.

7.3.2 Enable

When the EN pin voltage rises above the enable threshold voltage (typically 1.22 V) and VIN rises above the VIN UVLO rising threshold, the device enters its internal power-up sequence. The EN to first switching delay is specified in the Start-Up section in the Electrical Characteristics table.

When using the internal VCC LDO, the internal power-up sequence includes three sequential steps. During the first period, the VCC voltage is charged up on the VCC bypass capacitor by a 11-mA current source. The length of this VCC LDO start-up time varies with the capacitance on the VCC pin. However, if V_{IN} voltage ramps up very slowly, the VCC LDO output voltage is limited by theVIN voltage level, so the VCC LDO start-up time can be extended longer. Since the VCC LDO start-up time is relatively long, the internal V_{INTREF} build-up happens and finishes during this period. Once the VCC voltage crosses above the VCC UVLO rising threshold (typically 2.87 V), the device moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection, and control loop initialization are finished within this 285- μ s delay. The soft-start ramp starts when the 285- μ s power-on delay finishes. During the soft-start ramp power stage, switching does not happen until the SS/REFIN pin voltage reaches 50 mV. This introduces a SS delay, which varies with the external capacitance on the SS/REFIN pin.

图 7-1 shows an example where the VIN UVLO rising threshold is satisfied earlier than the EN rising threshold. In this scenario, the VCC UVLO rising threshold becomes the gating signal to start the internal power-up sequence, and the sequence between VIN and EN does not matter.

When using an external bias on the VCC pin, the internal power-up sequence still includes three sequential steps. The first period is much shorter since the VCC voltage is built up already. A 100-μs period allows the internal references start up and stabilize. This 100-μs period includes not only the 0.6-V V_{INTREF}, but also all of the other reference voltages for various functions. The device then moves to the second step, power-on delay. The MODE pin setting detection, SS/REFIN pin detection, and control loop initialization are finished within this

285- μ s delay. The soft-start ramp starts when the 285- μ s power-on delay finishes. During the soft-start ramp power stage, switching does not happen until the SS/REFIN pin voltage reaches 50 mV. This introduced a SS delay, which varies with the external capacitance on the SS/REFIN pin.

图 7-2 shows an example where both the VIN UVLO rising threshold and EN rising threshold are satisfied later than the VCC UVLO rising threshold. In this scenario, the VIN UVLO rising threshold or EN rising threshold, whichever is satisfied later, becomes the gating signal to start the internal power-up sequence.

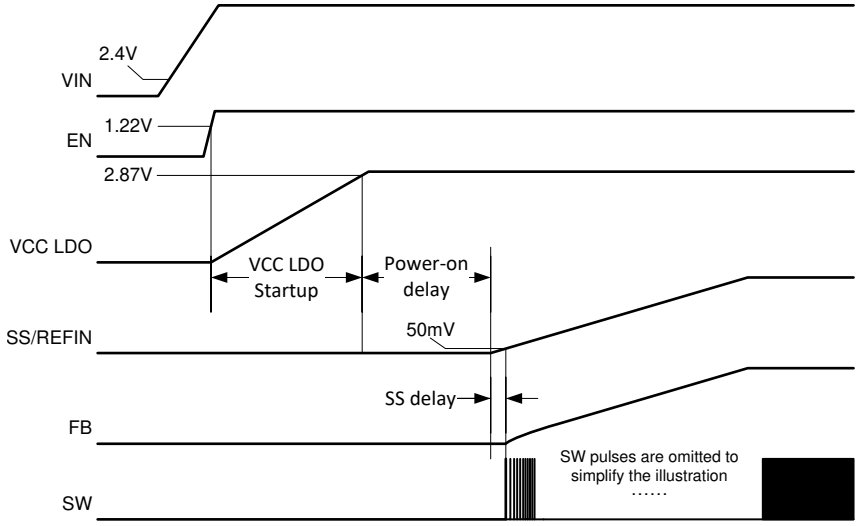


图 7-1. Internal Power-up Sequence Using Internal LDO

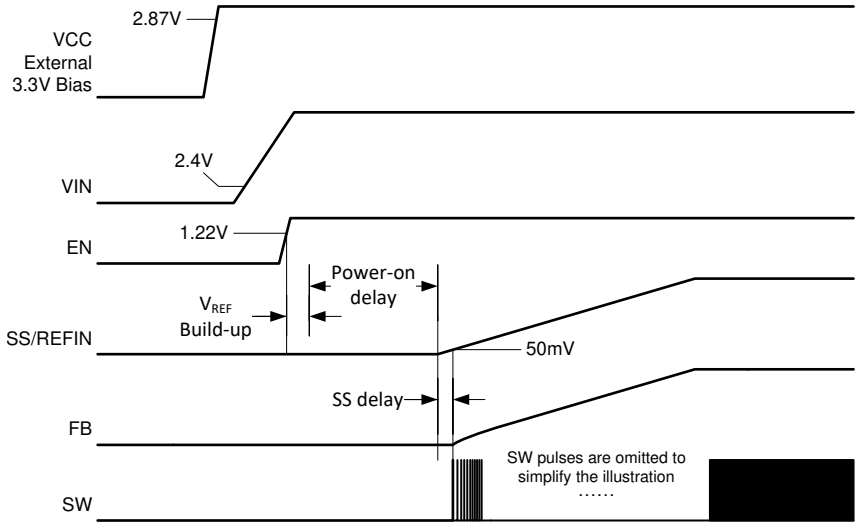


图 7-2. Internal Power-up Sequence Using External Bias

The EN pin has an internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 5 µs. For example, when applying a 3.3-V voltage source on the EN pin, which jumps from 0 V to 3.3 V with ideal rising edge, the internal EN signal reaches 2.086 V after 5 µs, which is 63.2% of applied 3.3-V voltage level.

A internal pulldown resistor is implemented between the EN pin and AGND pin. To avoid impact to the EN rising/falling threshold, this internal pulldown resistor is set to 6.5 M Ω . With this pulldown resistor, floating the EN pin before start-up keeps the device under disabled state. During nominal operation when the power stage switches, this large internal pulldown resistor may not have enough noise immunity to hold the EN pin low.

The recommended operating condition for EN pin is maximum 5.5 V. *Do not* connect the EN pin to the VIN pin directly.

7.3.3 Output Voltage Setting

The output voltage is programmed by the voltage divider resistors, R_{FB_HS} and R_{FB_LS}. Connect R_{FB_HS} between the FB pin and the positive node of the load, and connect R_{FB_LS} between the FB pin and the VSNS – pin. The recommended R_{FB_LS} value is 10 kΩ, ranging from 1 kΩ to 20 kΩ. Determine R_{FB_HS} by using 方程式 1.

$$R_{FB\_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB\_LS} \quad (1)$$

The FB accuracy is determined by two elements. The first element is the accuracy of the internal 600-mV reference, which is applied to the SS/REFIN pin unless an external V_{REF} is applied. Both TPSM8A28 and TPSM8A29 offer ±0.5% V_{INTREF} accuracy from a 0°C to 85°C temperature range, and ±1.0% V_{INTREF} accuracy from a -40°C to 125°C temperature range. The second element is the SS/REFIN-to-FB accuracy, which tells the user how accurately the control loop regulates the FB node to the SS/REFIN pin. The TPSM8A29 offers ±0.6% SS/REFIN-to-FB accuracy from a -40°C to 125°C temperature range. For example, when operating from a 0°C to 85°C temperature range, the total FB accuracy is ±1.1%, which includes the impact from the chip junction temperature and also the variation from part to part.

To improve the overall V_{OUT} accuracy, using ±1% accuracy or better resistor for FB voltage divider is highly recommended.

Regardless of remote sensing or single-end sensing connection, the FB voltage divider, R_{FB_HS} and R_{FB_LS}, must be always placed as close as possible to the device.

7.3.3.1 Remote Sense

The TPSM8A28 and TPSM8A29 modules feature remote sense function through the FB and VSNS – pins. Remote sense function compensates a potential voltage drop on the PCB traces, helping maintain V_{OUT} tolerance under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing of the output voltage at a remote location. The connections from the FB voltage divider resistors to the remote location must be a pair of PCB traces with at least 12-mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1 µF or higher. The ground connection of the remote sensing signal must be connected to the VSNS – pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor, R_{FB_LS}, terminated at the VSNS – pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. It is recommended to shield the pair of remote sensing lines with ground planes above and below.

Single-ended V_O sensing is often used for local sensing. For this configuration, connect the higher FB resistor, R_{FB_HS}, to a high-frequency local bypass capacitor of 0.1 µF or higher, and short VSNS – to AGND.

The recommended VSNS – operating range (refer to AGND pin) is –50 mV to +50 mV.

7.3.4 Internal Fixed Soft Start and External Adjustable Soft Start

The TPSM8A28 and TPSM8A29 power modules allow both internal fixed soft start and external adjustable soft start. The internal soft-start time is 1.5 ms. The soft-start time can be increased by adding a soft-start (SS) capacitor between the SS/REFIN and VSNS – pins. The total SS capacitor value can be determined by 方程式 2. The device follows the longer SS ramp among the internal SS time and the SS time determined by the external SS capacitors.

The device does not require a capacitor from the SS/REFIN pin to AGND, so it is not recommended to place a capacitor from the SS/REFIN pin to AGND. If both $C_{SS/REFIN}$-to-VSNS – and $C_{SS/REFIN}$-to-AGND capacitors exist, place $C_{SS/REFIN}$-to-VSNS – more closely to the shortest trace back to the VSNS – pin.

The SS/REFIN pin is discharged internally during the internal power-on delay to make sure the soft-start ramp always starts from zero.

$$C_{SS}(nF)=\frac{t_{SS}(ms)\times 36(\mu A)}{V_{INTREF}(V)} \quad (2)$$

7.3.5 External REFIN for Output Voltage Tracking

The TPSM8A28 and TPSM8A29 provide analog input pin (SS/REFIN) to accept an external reference (that is, a DC voltage source). The device always looks at the voltage on this SS/REFIN pin as the reference for the control loop. When an external voltage reference is applied between the SS/REFIN pin and VSNS – pin, it acts as the reference voltage, so the FB voltage follows this external voltage reference exactly. The same ±0.6% SS/REFIN-to-FB accuracy from a -40°C to 125°C temperature range applies here too.

In the middle of internal power-on delay, a detection circuit senses the voltage on the SS/REFIN pin to tell whether an active DC voltage source is applied. Before the detection happens, the SS/REFIN pin tries to discharge any energy on the SS/REFIN capacitors through an internal 120-Ω resistor to AGND, lasting 125 µs. Then, within a 32-µs window, the detection circuit compares the SS/REFIN pin voltage with an internal reference equal to 89% of V_{INTREF}. This discharge operation makes sure a SS capacitor with left-over energy is not wrongly detected as a voltage reference. If the external voltage reference failed to supply sufficient current and hold a voltage level higher than 89% of V_{INTREF}, the SS/REFIN detection circuit provides a wrong detection result.

If the detection result is that the SS/REFIN pin voltage holds higher than 89% of V_{INTREF}, which tells an active DC voltage source is used as external reference, the device always uses the SS/REFIN pin voltage instead of the internal V_{INTREF} as the reference for PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold. On this configuration, since the SS/REFIN pin senses a DC voltage and no soft-start ramp on this pin, the internal fixed soft start is used for start-up. Once the internal soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish because the soft-start ramp goes beyond V_{INTREF}.

If the detection result is that SS/REFIN pin voltage falls below 89% of V_{INTREF}, which tells no external reference is connected, the device first uses the internal fixed V_{INTREF} as the reference for PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold. On this configuration, given the SS/REFIN pin sees a soft-start ramp on this pin, the slower ramp amongst the internal fixed soft start and the external soft start determines the start-up of FB. Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish. The external soft-start done signal goes high when FB reaches a threshold equal to V_{INTREF} – 50 mV. The device waits for the PGOOD status transition from low to high, then starts using the SS/REFIN pin voltage instead of the internal V_{INTREF} as the reference for PGOOD threshold, V_{OUT} OVP, and V_{OUT} UVP threshold.

On this external REFIN configuration, applying a stabilized DC external reference to SS/REFIN pin before the EN high signal is recommended. During the internal power-on delay, the external reference must be capable of holding the SS/REFIN pin equal to or higher than 89% of V_{INTREF}, so that the device can correctly detect the external reference and choose the right thresholds for power good, V_{OUT} OVP, and V_{OUT} UVP. After the power-good status transits from low to high, the external reference can be set in a range of 0.5 V to 1.2 V. To overdrive the SS/REFIN pin during nominal operation, the external reference has to be able to sink more than 36-µA current if the external reference is lower than the internal V_{INTREF}, or source more than 12-µA current if the external reference is higher than the internal V_{INTREF}. When driving the SS/REFIN pin by an external reference through a resistor divider, the resistance of the divider must be low enough to provide the sinking or sourcing current capability.

If the external voltage source must transition up and down between any two voltage levels, the slew rate must be no more than 1 mV/µs.

7.3.6 Frequency and Operation Mode Selection

The TPSM8A29 provides forced CCM operation for tight output ripple applications and auto-skip Eco-mode for high light-load efficiency. The TPSM8A29 allows users to select the switching frequency and operation mode by connecting a resistor from the MODE pin to the AGND pin. 表 7-1 lists the resistor values for the switching

frequency and operation mode selection. TI recommends ±1% tolerance resistors with a typical temperature coefficient of ±100 ppm/°C.

The MODE state is set and latched during the internal power-on delay period. Changing the MODE pin resistance after the power-on delay does not change the status of the device. The internal circuit sets the MODE pin status to 600 kHz / Skip mode if the MODE pin is left open during the power-on delay period.

To make sure the internal circuit detects the desired option correctly, *do not* place any capacitor on the MODE pin.

表 7-1. MODE Pin Selection

MODE PIN CONNECTIONS	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)
Short to VCC	Skip-mode	600
243-kΩ ± 10% to AGND	Skip-mode	800
121-kΩ ± 10% to AGND	Skip-mode	1000
60.4-kΩ ±10% to AGND	Forced CCM	1000
30.1-kΩ ±10% to AGND	Forced CCM	800
Short to AGND	Forced CCM	600

7.3.7 D-CAP3™ Control

The TPSM8A28 and TPSM8A29 use D-CAP3™ mode control to achieve fast load transient while maintaining the ease-of-use feature. The D-CAP3™ control architecture includes an internal ripple generation network, enabling the use of very low ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low-ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP3™ control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. The amplitude of the ramp is determined by V_{IN}, V_{OUT}, operating frequency, and the R-C time-constant of the internal ramp circuit. At different switching frequency settings (see 表 7-1), the R-C time-constant varies to maintain a relatively constant ramp amplitude. Also, the device uses internal circuitry to cancel the DC offset caused by the injected ramp, and significantly reduce the DC offset caused by the output ripple voltage, especially under light-load condition.

For any control topologies supporting no external compensation design, there is a minimum range, maximum range, or both, of the output filter it can support. The output filter used is a low-pass L-C circuit. This L-C filter has double pole that is described in 方程式 3.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole of 方程式 3 is located no higher than 1/30th of operating frequency. Choose very small output capacitance leads to relatively high frequency L-C double pole, which allows the overall loop gain to stay high until the L-C double frequency. Make sure the zero from the internal ripple generation network has relatively high frequency as well. The loop with very small output capacitance can have too high of crossover frequency, which is not desired. Use 表 7-2 to help locate the internal zero based on the selected switching frequency.

表 7-2. Locating the Zero

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) LOCATION (kHz)
600	84.5
800	84.5
1000	106

In general, where reasonable (or smaller) output capacitance is desired, the output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = f_Z \quad (4)$$

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100th of the operating frequency. With this starting point, verify the small signal response on the board using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

The actual maximum output capacitance can go higher as long as the phase margin is greater than 50 degrees. However, small signal measurement (bode plot) must be done to confirm the design.

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10 µF, X5R, and 6.3 V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4 µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

For higher output voltage at or above 2 V, additional phase boost can be required in order to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on time (t_{ON})) setting in a fixed on-time topology based operation. A feedforward capacitor placed in parallel with R_{FB_HS} wasfound to be very effective to boost the phase margin at loop crossover. Refer to *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor Application Report* for details.

Besides boosting the phase, a feedforward capacitor feeds more V_{OUT} node information into the FB node by the AC coupling. This feedforward during load transient event enables the control loop a faster response to V_{OUT} deviation. However, this feedforward during steady state operation also feeds more V_{OUT} ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double pulse behavior. To determine the final feedforward capacitor value, impacts to phase margin, load transient performance, and ripple and nosie on FB must be all considered. Using Frequency Analysis equipment to measure the crossover frequency and the phase margin is recommended.

7.3.8 Low-Side FET Zero-Crossing

A zero-crossing circuit is used to perform the zero inductor-current detection during Skip-mode operation. The function compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. The zero-crossing threshold is set to a positive value to avoid negative inductor current. As a result, the TPSM8A28 and TPSM8A29 power modules deliver better light-load efficiency.

7.3.9 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on time of the high-side FET, the switch current increases at a linear rate determined by the following:

- input voltage
- output voltage
- the on time
- the output inductor value

During the on time of the low-side FET, this current decreases linearly. The average value of the switch current equals to the load current.

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on time of the low-side FET by measuring the low-side FET drain-to-source current. If the measured drain-to-source current of the low-side FET is above the current limit threshold, the low-side FET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device. During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (80%), the UVP comparator detects it and shuts down the device after a wait time of 68 µs. The device then enters a hiccup sleep period for approximately 14 ms. After this waiting period, the device attempts to start up again/remains latched off state (both high-side and low-side FETs are latched off) until a reset of VIN or a re-toggling on the EN pin. 图 7-3 shows the cycle-by-cycle valley current limit behavior as well as the wait time before the device shuts down.

If an OCL condition happens during start-up, the device still has cycle-by-cycle current limit based on low-side valley current. After soft start is finished, the UV event, which is caused by the OC event, shuts down the device and enters Hiccup mode with a wait time of 68 µs.

The resistor, R_{TRIP}, connected from the TRIP pin to AGND sets current limit threshold. ±1% tolerance resistor is highly recommended because a worse tolerance resistor provides less accurate OCL threshold.

To protect the device from unexpected connection on the TRIP pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on LS FET when TRIP pin has too small resistance to AGND, or is accidently shorted to ground.

$$R_{TRIP} = \frac{6 \times 10^4}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN}-V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} = \frac{K_{OCL}}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN}-V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}}} \quad (5)$$

where

- I_{OCLIM} is overcurrent limit threshold for load current in A
- R_{TRIP} is TRIP resistor value in Ω
- V_{IN} is input voltage value in V
- V_O is output voltage value in V
- L is output inductor value in µH
- f_{SW} is switching frequency in MHz

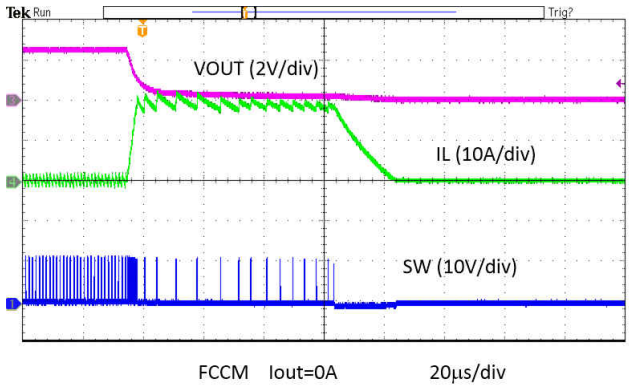


图 7-3. Overcurrent Protection

7.3.10 Low-Side FET Negative Current Limit

The device has a fixed, cycle-by-cycle negative current limit. Similar with the positive overcurrent limit, the inductor current is monitored during the on time of the low-side FET. To prevent too large negative current flowing through low-side FET, when the low-side FET detects –10-A current (typical threshold), the device turns off low-side FET and then turns on high-side FET for a proper on time (determined by $V_{IN}/V_O/f_{SW}$). After high-side FET on time expires, the low-side FET turns on again.

The device must not trigger the –10-A negative current limit threshold during nominal operation, unless a too small inductor value is chosen or the inductor becomes saturated. This negative current limit is used to discharge output capacitors during an output OVP or an OOB event. See 节 7.3.12 and 节 7.3.13 for details.

7.3.11 Power Good

TPSM8A28 and TPSM8A29 have gower-good output that output high when the converter output voltage is within specification. The power-good output is an open-drain output and must be pulled up to VCC pin or an external voltage source (< 5.5 V) through a pullup resistor (typically 30.1 kΩ). The recommended power-good pullup resistor value is 1 kΩ to 100 kΩ.

Once both the internal and external soft-start ramp finishes, the power-good signal becomes high after a 1.06-ms internal delay. The whole internal soft-start ramp takes 2 ms to finish. The external soft-start done signal goes high when FB reaches a threshold equal to V_{INTREF} – 50 mV. If the FB voltage drops to 80% of the V_{INTREF} voltage or exceeds 116% of the V_{INTREF} voltage, the power-good signal latches low after a 2-µs internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of VIN.

If the input supply fails to power up the device, for example VIN and VCC both stays at zero volts, the power-good pin clamps low by itself when this pin is pulled up through an external resistor.

Once the VCC voltage level rises above the minimum VCC threshold for valid PGOOD output (maximum 1.5 V), internal power-good circuit is enabled to hold the PGOOD pin to the default status. By default, PGOOD is pulled low and this low-level output voltage is no more than 400 mV with 5.5-mA sinking current. The power-good function is fully activated after the soft-start operation is completed.

7.3.12 Overvoltage and Undervoltage Protection

The TPSM8A28 and TPSM8A29 devices monitor a resistor-divided feedback voltage to detect overvoltage and undervoltage events. When the FB voltage becomes lower than 80% of the V_{INTREF} voltage, the UVP comparator detects and an internal UVP delay counter begins counting. After the 68-µs UVP delay time, the device enters Hiccup mode and re-starts with a sleep time of 14 ms. The UVP function enables after the soft-start period is complete.

When the FB voltage becomes higher than 116% of the V_{INTREF} voltage, the OVP comparator detects and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit I_{NOCL}. Upon reaching the negative current limit, the low-side FET is turned off, and the high-side FET is turned on again for a proper on time (determined by $V_{IN}/V_O/f_{SW}$). The device operates in this cycle until the output voltage is pulled lower than the UVP threshold voltage for 68 µs. After the 68-µs UVP delay time, both the high-side FET and the low-side FET are latched OFF. The fault is cleared with a reset of VIN or by retoggling the EN pin.

During the 68-µs UVP delay time, if output voltage becomes higher than the UV threshold, thus it is not qualified for the UV event, the timer is reset to zero. When the output voltage triggers the UV threshold again, the timer of the 68 µs re-starts.

7.3.13 Out-Of-Bounds (OOB) Operation

TPSM8A28 and TPSM8A29 devices have out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 5% above the V_{INTREF} voltage. OOB protection does not trigger an overvoltage fault, so the device is on non-latch mode after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced CCM mode. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor

thus helps the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated for the safe operation of the internal FETs.

7.3.14 Output Voltage Discharge

When the device is disabled through EN, it enables the output voltage discharge mode. This mode forces both high-side and low-side FETs to latch off, but turns on the discharge FET, which is connected from SW to PGND, to discharge the output voltage. Once the FB voltage drops below 100 mV, the discharge FET is turned off.

The output voltage discharge mode is activated by any of below fault events:

- EN pin goes low to disable the converter.
- Thermal shutdown (OTP) is triggered.
- VCC UVLO (falling) is triggered.
- VIN UVLO (falling) is triggered.

7.3.15 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the VIN_{UVLO} falling threshold voltage but the VCC pin voltage is still higher than the VCC_{UVLO} rising threshold voltage, the device stops switching and discharges SS/REFIN pin. Once the VIN voltage increases beyond the VIN_{UVLO} rising threshold voltage, the device re-initiates the soft start and switches again. VIN UVLO is a non-latch protection.

7.3.16 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges the SS/REFIN pin. When the temperature falls approximately 30°C below the threshold value, the device turns back on with a re-initiated soft start. Thermal shutdown is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip Eco-Mode Light Load Operation

While the MODE pin is pulled to VCC directly or connected to AGND pin through a resistor larger than 121 kΩ, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{O(LL)}$ (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in 方程式 6.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (6)$$

where

- f_{SW} is the switching frequency

Using only ceramic capacitors is recommended for Skip mode.

7.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the AGND pin through a resistor less than 60.4 kΩ, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency.

7.4.3 Powering the Device From a 12-V Bus

Both TPSM8A28 and TPSM8A29 can be powered by a single 12-V bus. In this configuration, the internal LDO is powered by a 12-V bus and generates a 4.5-V output to bias the internal analog circuitry and also powers up the gate drives. The VIN range under this configuration for TPSM8A29 is 4 V to 16 V for up to 15-A load current. VIN range for TPSM8A28 is 3 V to 16 V for up to 12 A. 图 7-4 shows an example for this single V_{IN} configuration.

VIN and EN are the two signals to enable the part. For a start-up sequence, any sequence between the VIN and EN signals can power the device up correctly.

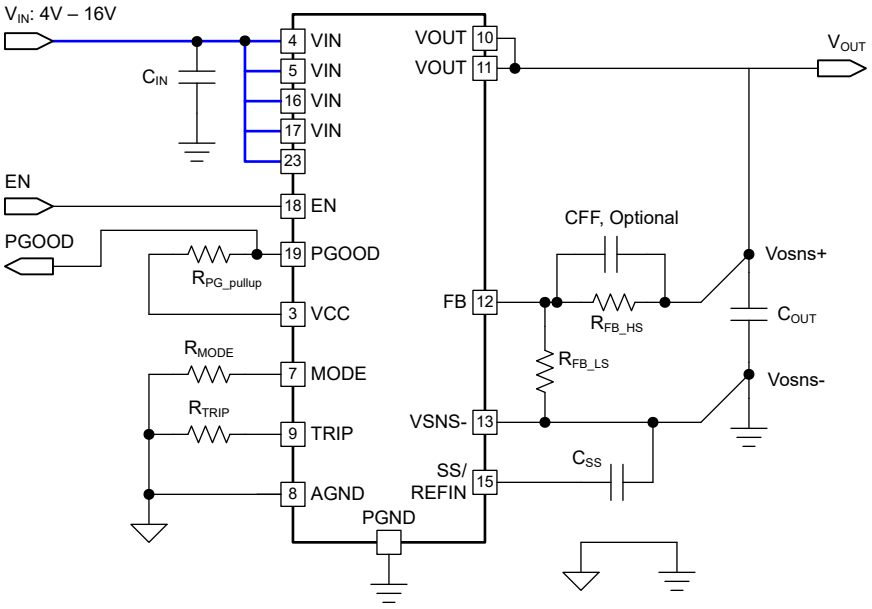


图 7-4. Single VIN Configuration With 12-V Bus

7.4.4 Powering the Device From a 5.0-V Bus

The TPSM8A29 can deliver up to a 15-A load current when powering from a 5-V bus, 12 A for TPSM8A28. To make sure the internal analog circuitry and the gate drives are powered up properly, the VCC pin must be shorted to the VIN pins with a low impedance trace. A trace with at least 24-mil width is recommended. Due to the maximum rating limit on the VCC pin, the VIN input range under this configuration is 4.75 V to 5.3 V. The input voltage must stay higher than both VIN UVLO and VCC UVLO, otherwise the device shuts down immediately. 图 7-5 shows an example for this single VIN configuration.

VIN and EN are the two signals to enable the part. For start-up sequence, any sequence between the VIN and EN signals can power the device up correctly.

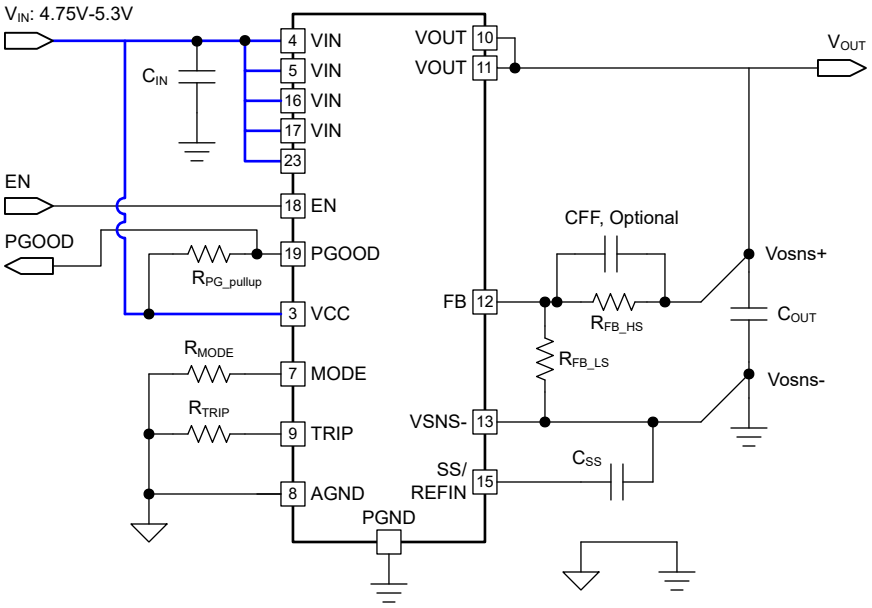


图 7-5. Single VIN Configuration With 5.0-V Bus

7.4.5 Powering the Device From a Split-Rail Configuration

The TPSM8A28 and TPSM8A29 devices can be configured to split-rail by using an independent power supply that applies a valid bias on to VCC pin. Connecting a valid VCC bias to the VCC pin overrides the internal LDO, thus saves power loss on that linear regulator and helps to improve overall system level efficiency. 5.0-V rail is the common choice as VCC bias. With a stable VCC bias, the VIN input range under this configuration can be as low as 2.7 V and up to 16 V for both TPSM8A28 and TPSM8A29.

图 7-6 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to Skip mode, the VCC pins decreases current draw from the external bias when the frequency decreases under light-load condition. The typical VCC external bias current under FCCM operation is listed in the Electrical Characteristics table to help the user prepare the capacity of the external bias.

Under split rail configuration, VIN, VCC bias, and EN are the signals to enable the part. For start-up sequence, it is recommended that at least one of VIN UVLO rising threshold and EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical start-up sequence example is: VIN applied first, then the external bias applied, and then EN signal goes high.

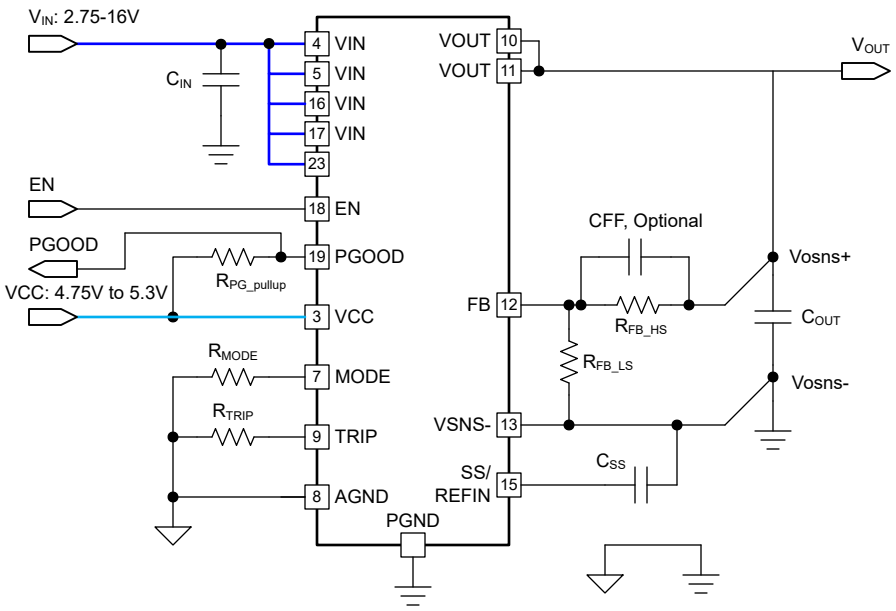


图 7-6. Split Rail Configuration With External VCC Bias

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPSM8A28 and TPSM8A29 power modules feature an integrated power inductor and some basic passives. The devices are small and highly efficient, suitable for low output voltage point-of-load applications up to 15 A. These devices features proprietary D-CAP3™ mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an ideal fashion. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage ranges from 2.7 V to 16 V, and the VCC input voltage ranges from 4.75 V to 5.3 V. The D-CAP3™ control mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require an external phase-compensation network, which makes the device easy to use and also allows for a low external component count. Another advantage of this control scheme is that it supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low-ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

8.2 Typical Application

The schematic shows a typical application for the TPSM8A29. This example describes the design procedure of converting an input voltage range of 9.6 V to 14.4 V to a 1-V output, up to 15-A load current.

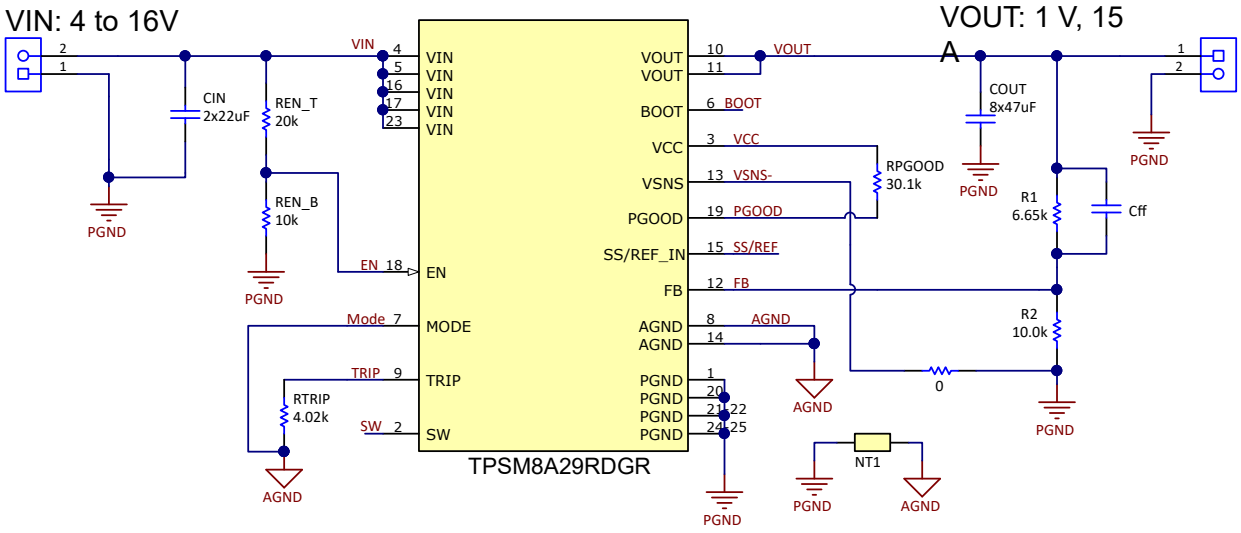


图 8-1. Application Circuit Diagram

8.2.1 Design Requirements

This design uses the parameters listed in 表 8-1. A switching frequency of 600 kHz was chosen to maximize efficiency. See 表 7-1 for all switching frequency and operating mode configurations.

表 8-1. Design Example Specifications

DESIGN PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Voltage range		9.6	12	14.4	V
V_{OUT}	Output voltage			1.0		V
ILOAD	Output load current				15	A
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 15 A		10		mV_{PP}
V_{TRANS}	Output voltage undershoot and overshoot after load step	I_{OUT} = 50% to 100% step, 5 A/µs slew rate		±50		mV
I_{OVER}	Output overcurrent			15		A
t_{SS}	Soft-start time			1.5		ms
f_{SW}	Switching frequency			600		kHz
	Operating mode			FCCM		
T_A	Operating temperature			25		°C

8.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP3™ mode. Select the external components using the following steps.

8.2.2.1 Output Voltage Setting Point

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in 方程式 7. Connect R1 between the FB pin and the output, and connect R2 between the FB pin and VSNS – . The recommended R2 value is 10 kΩ, but it can also be set to another value between the range of 1 kΩ to 20 kΩ. Determine R1 by using 方程式 7. For 1.0 V_{OUT}, a value of 6.65 kΩ is chosen.

$$R1 = \frac{V_{OUT} - V_{INTREF}}{V_{INTREF}} \times R2 = \frac{1\,V - 0.6\,V}{0.6\,V} \times 10\,k\Omega = 6.65\,k\Omega \quad (7)$$

8.2.2.2 Choose the Inductor

An optimized 0.6- µH inductor is integrated inside the module.

8.2.2.3 Set the Current Limit (TRIP)

The R_{TRIP} resistor sets the valley current limit. 方程式 8 calculates the recommended current limit target. 方程式 9 calculates the R_{TRIP} resistor to set the current limit. The typical valley current limit target is 15.0 A, and the closest standard value for R_{TRIP} is 4.02 kΩ.

$$I_{LIMVALLEY} = I_{OUT} - \frac{1}{2} \times \frac{\left(V_{IN(MIN)} - V_{OUT}\right) \times V_{OUT}}{0.6\,\mu H \times V_{IN(MIN)} \times fsw} = 15\,A - \frac{1}{2} \times \frac{(9.6\,V - 1\,V) \times 1\,V}{0.6\,\mu H \times 9.6\,V \times 600\,kHz} = 13.756\,A \quad (8)$$

$$R_{TRIP} = \frac{60000}{I_{LIMVALLEY}} = \frac{60000}{15\,A} = 4.0\,k\Omega \quad (9)$$

With the current limit set, 方程式 10 calculates the typical maximum output current at current limit. 方程式 11 calculates the typical peak current at current limit. For worst case calculations, the tolerance of the inductance (20%) and the current limit must be included.

$$I_{OUTLIM} = I_{LIMVALLEY} - \frac{1}{2} \times \frac{\left(V_{IN(MIN)} - V_{OUT}\right) \times V_{OUT}}{0.6\,\mu H \times V_{IN(MIN)} \times fsw} = 15\,A - \frac{1}{2} \times \frac{(9.6\,V - 1\,V) \times 1\,V}{0.6\,\mu H \times 9.6\,V \times 600\,kHz} = 16.24\,A \quad (10)$$

$$I_{L(PEAK)} = I_{LIMVALLEY} - \frac{1}{2} \times \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{0.6\ \mu H \times V_{IN(MAX)} \times fsw} = 15\ A - \frac{1}{2} \times \frac{(14.4\ V - 1\ V) \times 1\ V}{0.6\ \mu H \times 14.4\ V \times 600\ kHz} = 16.29\ A \quad (11)$$

8.2.2.4 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor.

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First, the minimum output capacitance must be calculated based on these three requirements. 方程式 12 calculates the minimum capacitance to keep the LC double pole below 1/30th the f_{SW} to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero.

$$C_{OUT\_STABILITY} > \left(\frac{30}{2\pi \times fsw}\right)^2 \times \frac{1}{0.6\ \mu H} = \left(\frac{30}{2\pi \times 600\ kHz}\right)^2 \times \frac{1}{0.6\ \mu H} = 105.5\ \mu F \quad (12)$$

$$C_{OUT\_RIPPLE} > \frac{\left(\frac{V_{IN(MAX)} - Vout}{V_{IN(MAX)}}\right) \times \left(\frac{Vout}{0.6\ \mu H \times fsw}\right)}{8 \times V_{ripple} \times fsw} = \frac{\left(\frac{14.4\ V - 1V}{14.4\ V}\right) \times \left(\frac{1V}{0.6\ \mu H \times 600kHz}\right)}{8 \times 10\ mV \times 600kHz} = 53.8\ \mu F \quad (13)$$

方程式 13 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 10 mV. This calculation is for FCCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors. 方程式 14 and 方程式 15 calculate the minimum capacitance to meet the transient response requirement of ±50 mV for a 7.5-A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

$$C_{OUT\_UNDERSHOOT} > \frac{0.6\ \mu H \times {I_{STEP}}^2 \times \left(\frac{Vout}{V_{IN(MIN)} \times fsw} + toff\right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN(MIN)} - V_{OUT}}{V_{IN(MIN)} \times fsw} - toff\right)} = \frac{0.6\ \mu H \times {7.5}^2 \times \left(\frac{1V}{9.6\ V \times 600kHz} + 220ns\right)}{2 \times 50mV \times 1V \times \left(\frac{9.6\ V - 1\ V}{9.6\ V \times 600kHz} - 220ns\right)} \quad (14)$$

$$= 104.4\ \mu F$$

$$C_{OUT\_OVERSHOOT} > \frac{0.6\ \mu H \times {I_{STEP}}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.6\ \mu H \times {7.5}^2}{2 \times 50mV \times 1V} = 337.5\ \mu F \quad (15)$$

The output capacitance needed to meet the overshoot requirement is the highest value, so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance. 方程式 16 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}. It can be possible to use more output capacitance but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 8 × 47-μF ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to approximately 95% of their nominal value giving an effective total capacitance of approximately 357 μF. This effective capacitance meets the minimum and maximum requirements.

$$C_{OUT\_STABILITY} < \left(\frac{50}{\pi \times fsw}\right)^2 \times \frac{1}{0.6\ \mu H} = \left(\frac{50}{\pi \times 600\ kHz}\right)^2 \times \frac{1}{0.6\ \mu H} = 1172.7\ \mu F \quad (16)$$

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non-ceramic capacitors, as a starting point, the ESR must be below the values calculated in 方程式 17 to meet the ripple requirement and 方程式 18 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{\left(\frac{V_{IN(MAX)} - Vout}{V_{IN(MAX)}}\right) \times \left(\frac{Vout}{0.6\ \mu H \times fsw}\right)} = \frac{10\ mV}{\left(\frac{14.4\ V - 1\ V}{14.4\ V}\right) \times \left(\frac{1\ V}{0.6\ \mu H \times 600\ kHz}\right)} = 3.86\ m\Omega \quad (17)$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{50\ mV}{7.5\ A} = 6.67\ m\Omega \quad (18)$$

8.2.2.5 Choose the Input Capacitors (C_{IN})

The device requires input bypass capacitors between the VIN and PGND pins to bypass the power stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout will allow. At least 10-µF of ceramic capacitance is required. Two 0.1-µF and one 1-nF capacitors are integrated inside to the module package, eliminating the need for typical high frequency bypass capacitors. However, they can be used if desired. The high frequency bypass capacitors minimizes high frequency voltage overshoot across the power-stage. The ceramic capacitors must be high-quality dielectric of X6S or better for their high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with 方程式 19. A recommended target input voltage ripple is 5% the minimum input voltage, 480 mV in this example. The calculated input capacitance is 4.86 µF, and the minimum input capacitance of 10 µF exceeds this. This example meets these two requirements with 2 × 22-µF ceramic capacitors. An input capacitor must be used on both sides of the module during layout, close to pins 5 and 16.

$$C_{IN} > \frac{Vout \times Iout \times \left(1 - \frac{Vout}{V_{IN(MIN)}}\right)}{fsw \times V_{IN(MIN)} \times V_{IN\_RIPPLE}} = \frac{1\ V \times 15\ A \times \left(1 - \frac{1\ V}{9.6\ V}\right)}{600\ kHz \times 9.6\ V \times 480\ mV} = 4.86\ \mu F \quad (19)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by 方程式 20 and is 4.588 A in this example. The ceramic input capacitors have a current rating greater than this.

$$I_{CIN(RMS)} = \sqrt{\frac{Vout}{V_{IN(MIN)}} \times \left(\left(\frac{V_{IN(MIN)} - Vout}{V_{IN(MIN)}}\right) \times {I_{OUT}}^2 + \frac{\left(\left(\frac{V_{IN(MIN)} - Vout}{V_{IN(MIN)}}\right) \times \left(\frac{Vout}{0.6\ \mu H \times fsw}\right)\right)^2}{12}\right)} = \quad (20)$$

$$I_{CIN(RMS)} = \sqrt{\frac{1\ V}{9.6\ V} \times \left(\left(\frac{9.6\ V - 1\ V}{9.6\ V}\right) \times {15\ A}^2 + \frac{\left(\left(\frac{9.6\ V - 1\ V}{9.6\ V}\right) \times \left(\frac{1\ V}{0.6\ \mu H \times 600\ kHz}\right)\right)^2}{12}\right)} = 4.588\ A \quad (21)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, the selection process in this article is recommended.

8.2.2.6 Soft-Start Capacitor (SS/REFIN Pin)

The capacitor placed on the SS/REFIN pin can be used to extend the soft-start time past the internal 1.5-ms soft start. The required external capacitance can be calculated with 方程式 2. The module incorporates a 1-nF capacitor between the SS/REFIN pin and VSNS-. This example uses a minimum default soft-start time of 1.5 ms.

8.2.2.7 EN Pin Resistor Divider

A resistor divider on the EN pin can be used to increase the input voltage the converter begins its startup sequence. To set the start voltage, first select the bottom resistor (R_{EN_B}). The recommended value is between 1 kΩ and 100 kΩ. There is an internal pulldown resistance with a nominal value of 6 MΩ. This must be included for the most accurate calculations. This is especially important when the bottom resistor is a higher value, near

100 kΩ. This example uses a 10-kΩ resistor and this combined with the internal resistance in parallel results in an equivalent bottom resistance of 9.98 kΩ. The top resistor value for the target start voltage is calculated with 方程式 22. In this example, the nearest standard value of 20 kΩ is selected for R_{EN_T}. When selecting a start voltage in a wide input range application, be cautious that the EN pin absolute maximum voltage of 6 V is not exceeded.

$$R_{EN\_T} = \frac{R_{EN\_B} \times V_{start}}{V_{ENH}} - R_{EN\_B} = \frac{10\ k\Omega \times 3.7\ V}{1.22\ V} - 10\ k\Omega = 20\ k\Omega \quad (22)$$

The start and stop voltages with the selected EN resistor divider can be calculated with 方程式 23 and 方程式 24, respectively.

$$V_{start} = V_{ENH} \times \frac{R_{EN\_T} + R_{EN\_B}}{R_{EN\_B}} = 1.22\ V \times \frac{20\ k\Omega + 10\ k\Omega}{10\ k\Omega} = 3.66\ V \quad (23)$$

$$V_{stop} = V_{ENL} \times \frac{R_{EN\_T} + R_{EN\_B}}{R_{EN\_B}} = 1.02\ V \times \frac{20\ k\Omega + 10\ k\Omega}{10\ k\Omega} = 3.06\ V \quad (24)$$

8.2.2.8 VCC Bypass Capacitor

A 1.0-μF bypass capacitor is integrated inside the module. No external bypass is required.

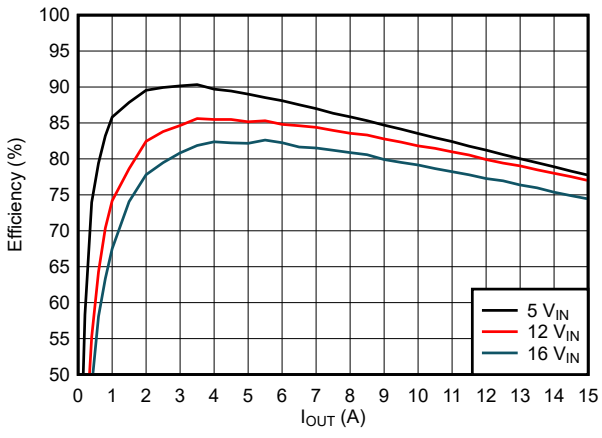
8.2.2.9 BOOT Capacitor

A 0.1-μF boot capacitor is integrated inside the module, no additional boot capacitor is necessary.

8.2.2.10 PGOOD Pullup Resistor

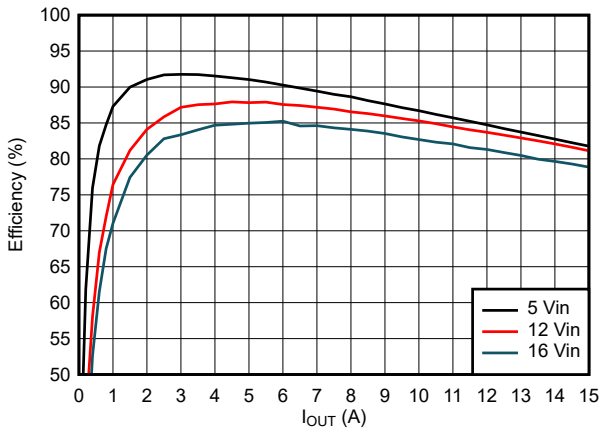
The PGOOD pin is open-drain so a pullup resistor is required when using this pin. The recommended value is between 1 kΩ and 100 kΩ.

8.2.3 Application Curves



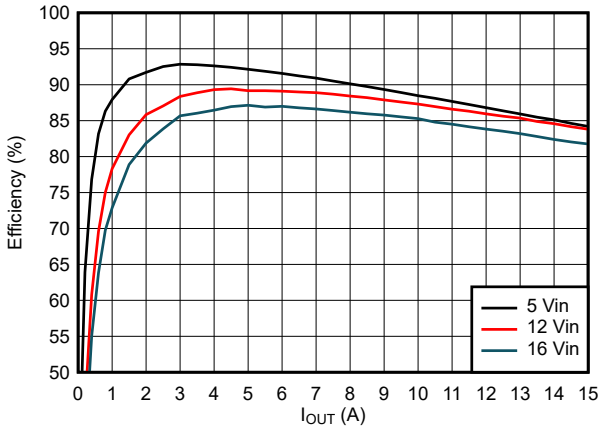
V_{OUT} = 0.6 V f_{sw} = 600 kHz Internal bias FCCM

图 8-2. Efficiency



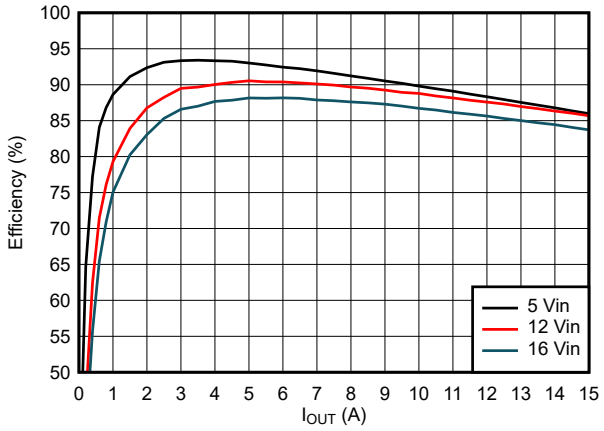
V_{OUT} = 0.8 V f_{sw} = 600 kHz Internal bias FCCM

图 8-3. Efficiency



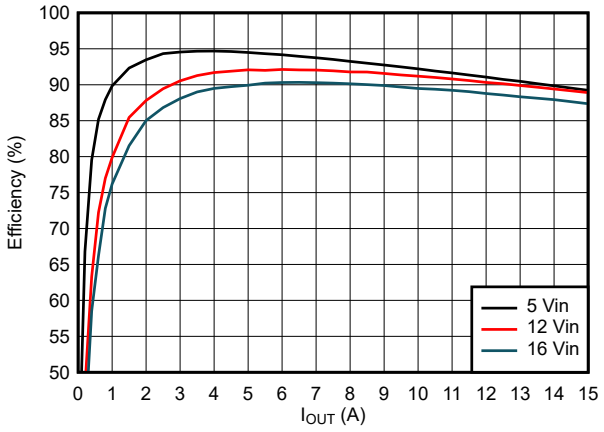
V_{OUT} = 1.0 V f_{sw} = 600 kHz Internal bias FCCM

图 8-4. Efficiency



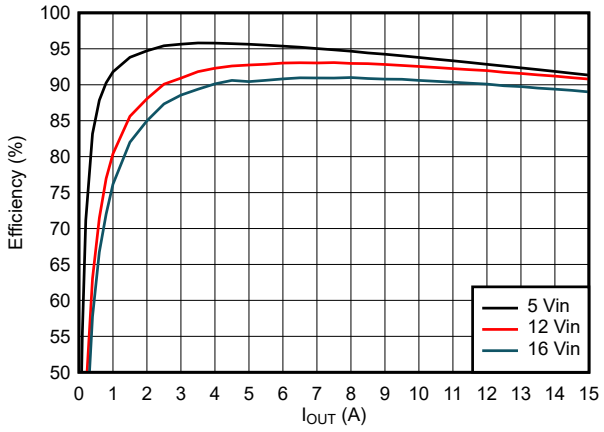
V_{OUT} = 1.2 V f_{sw} = 600 kHz Internal bias FCCM

图 8-5. Efficiency



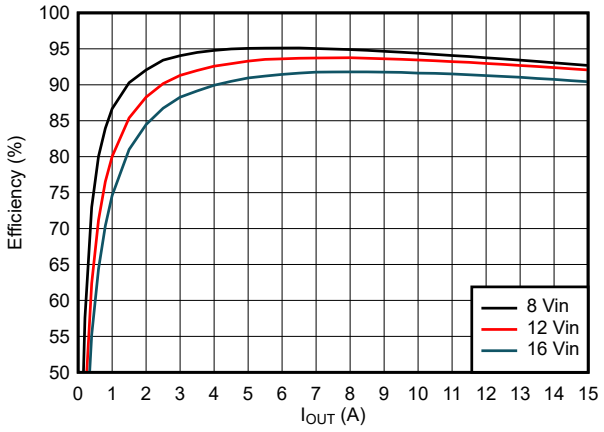
V_{OUT} = 1.8 V f_{sw} = 600 kHz Internal bias FCCM

图 8-6. Efficiency



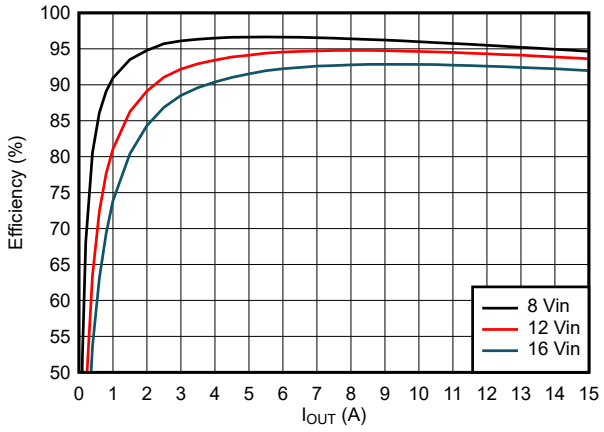
V_{OUT} = 2.5 V f_{sw} = 600 kHz Internal bias FCCM

图 8-7. Efficiency



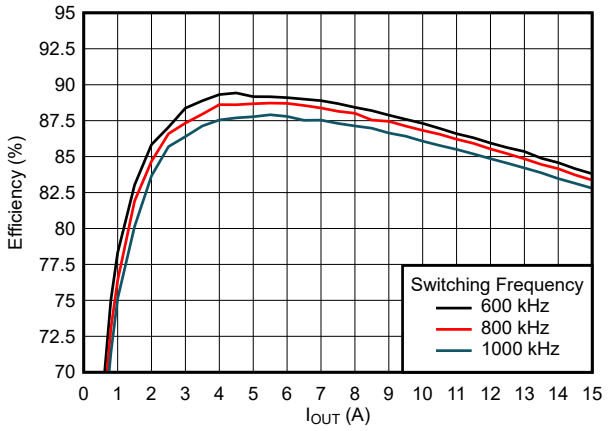
V_{OUT} = 3.3 V f_{sw} = 600 kHz Internal bias FCCM

图 8-8. Efficiency



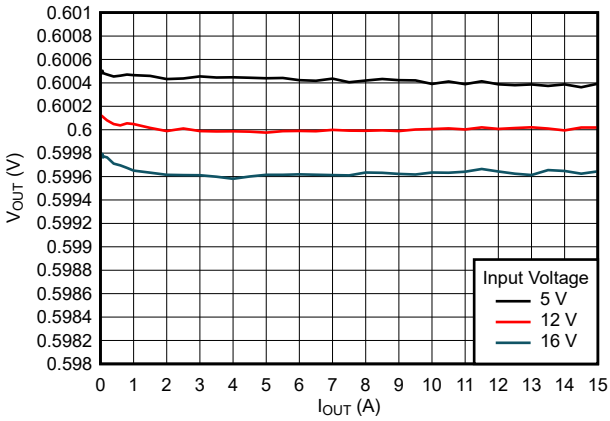
V_{OUT} = 5 V f_{sw} = 600 kHz Internal bias FCCM

图 8-9. Efficiency



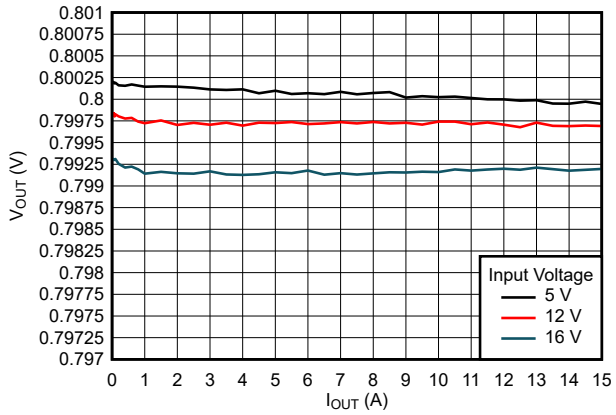
V_{IN} = 12 V V_{OUT} = 1 V Internal bias FCCM

图 8-10. Efficiency



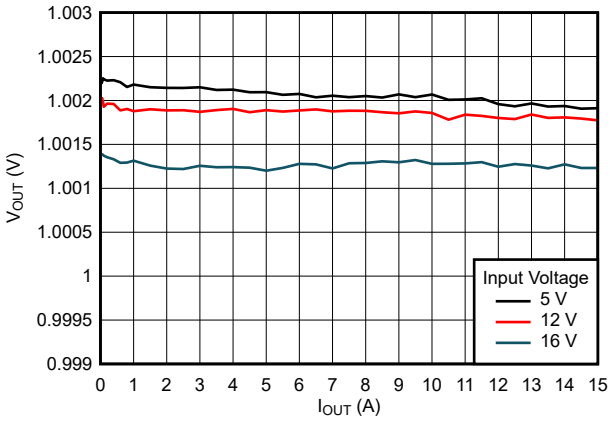
V_{OUT} = 0.6 V f_{SW} = 600 kHz Internal bias FCCM

图 8-11. Load Regulation



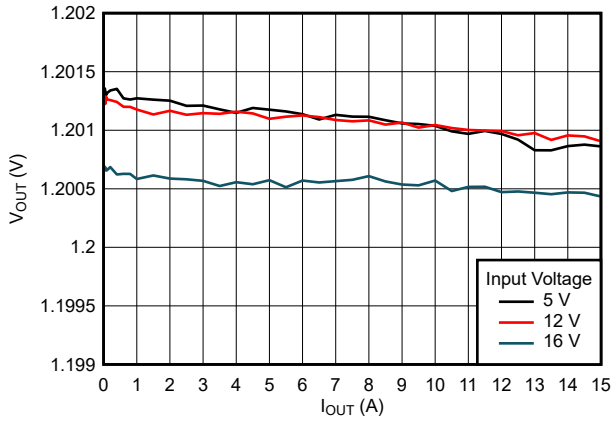
V_{OUT} = 0.8 V f_{SW} = 600 kHz Internal bias FCCM

图 8-12. Load Regulation



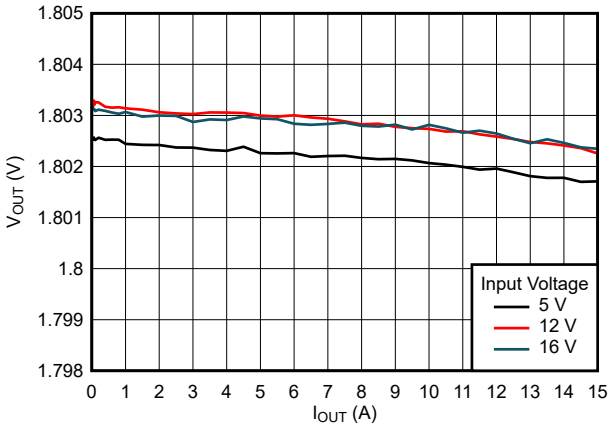
V_{OUT} = 1.0 V f_{SW} = 600 kHz Internal bias FCCM

图 8-13. Load Regulation



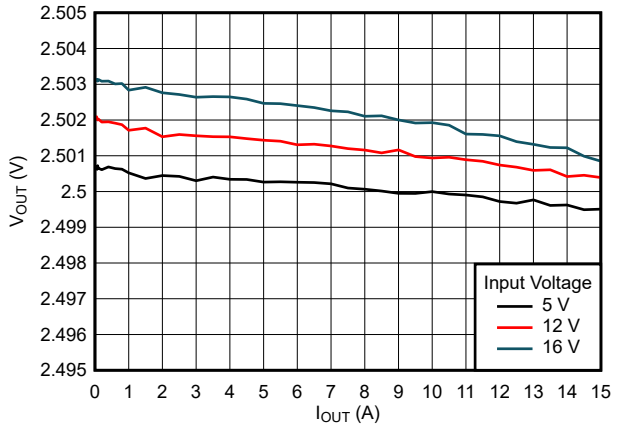
V_{OUT} = 1.2 V f_{SW} = 600 kHz Internal bias FCCM

图 8-14. Load Regulation



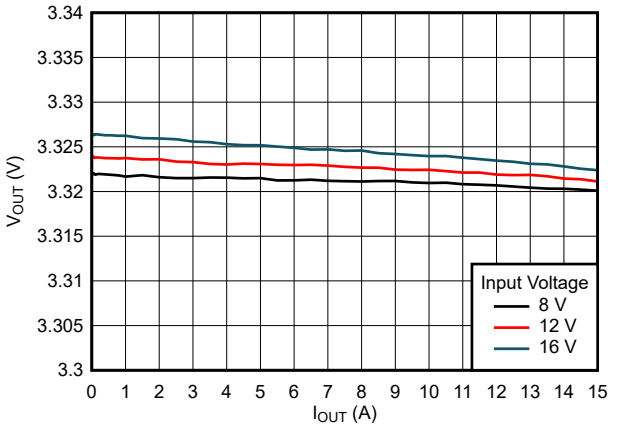
V_{OUT} = 1.8 V f_{SW} = 600 kHz Internal bias FCCM

图 8-15. Load Regulation



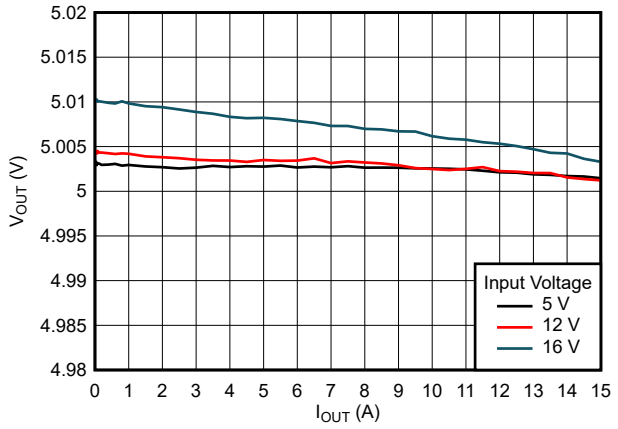
V_{OUT} = 2.5 V f_{SW} = 600 kHz Internal bias FCCM

图 8-16. Load Regulation



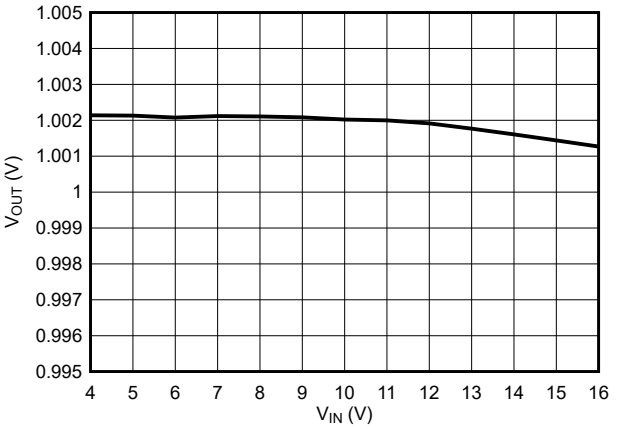
V_{OUT} = 3.3 V f_{SW} = 600 kHz Internal bias FCCM

图 8-17. Load Regulation



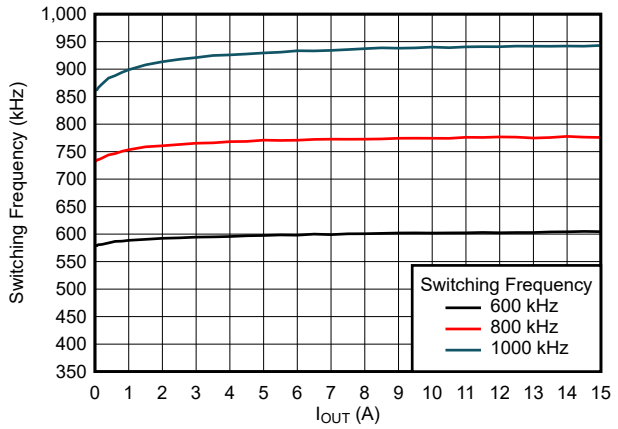
V_{OUT} = 5 V f_{SW} = 600 kHz Internal bias FCCM

图 8-18. Load Regulation



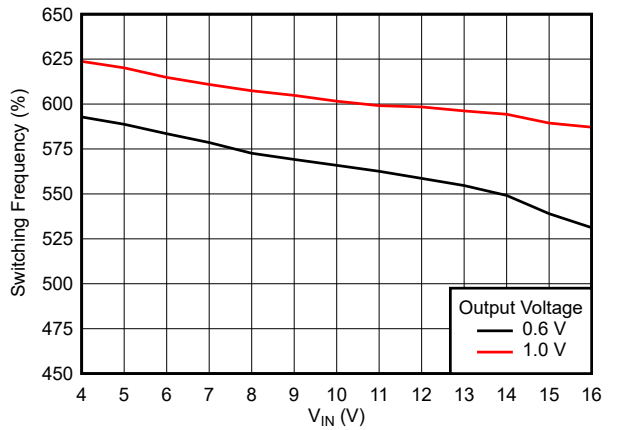
V_{OUT} = 1.0 V I_{OUT} = 5 A Internal bias f_{SW} = 600 kHz FCCM

图 8-19. Line Regulation



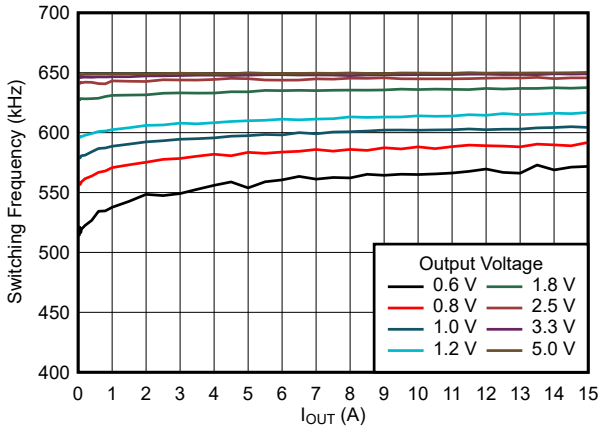
V_{IN} = 12 V V_{OUT} = 1.0 V Internal bias FCCM

图 8-20. Switching Frequency



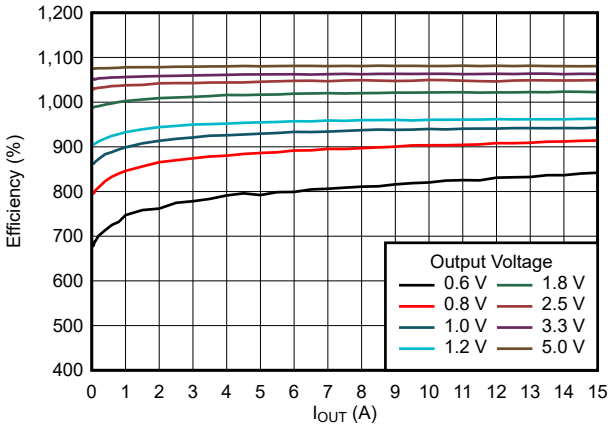
I_{OUT} = 5 A f_{SW} = 600 kHz Internal bias FCCM

图 8-21. Switching Frequency



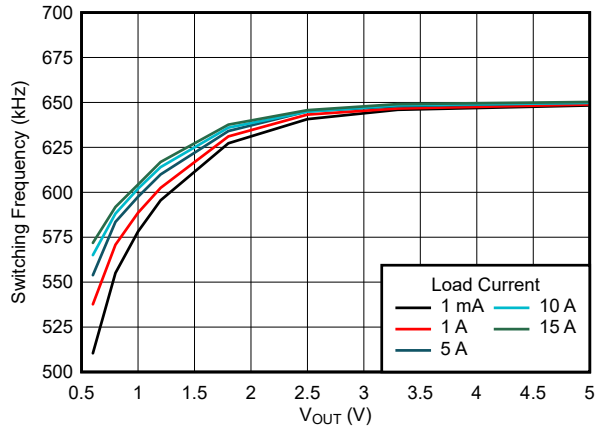
V_{IN} = 12 A f_{SW} = 600 kHz Internal bias FCCM

图 8-22. Switching Frequency



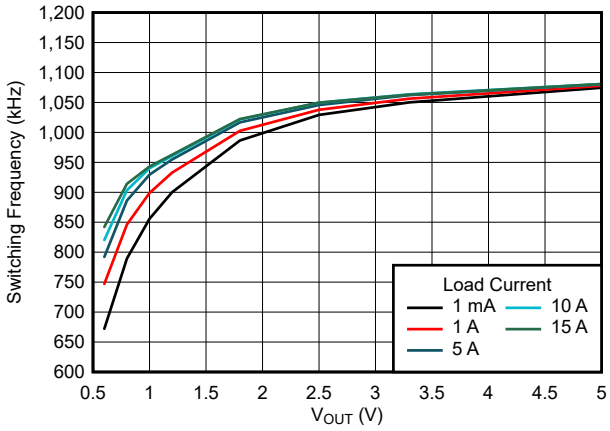
V_{IN} = 12 V f_{SW} = 1000 kHz Internal bias FCCM

图 8-23. Switching Frequency



V_{IN} = 12 V f_{SW} = 600 kHz Internal bias FCCM

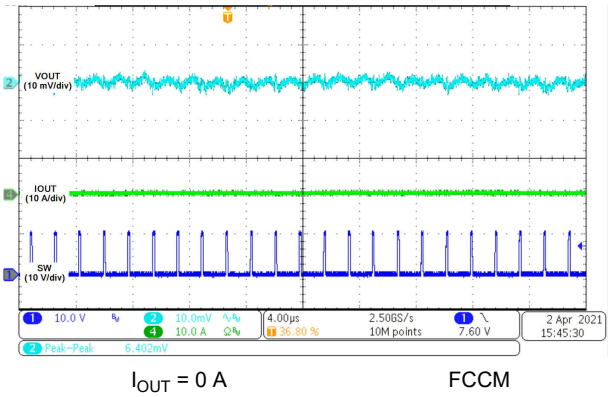
图 8-24. Switching Frequency



V_{IN} = 12 V f_{SW} = 1000 kHz Internal bias FCCM

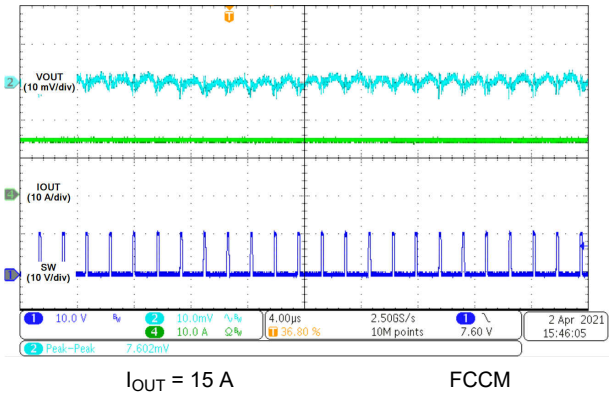
图 8-25. Switching Frequency

In the following images, all measurements taken with V_{IN} = 12 V, V_{OUT} = 1 V, f_{SW} = 600 kHz, internal bias, T_{AMB} = 25°C



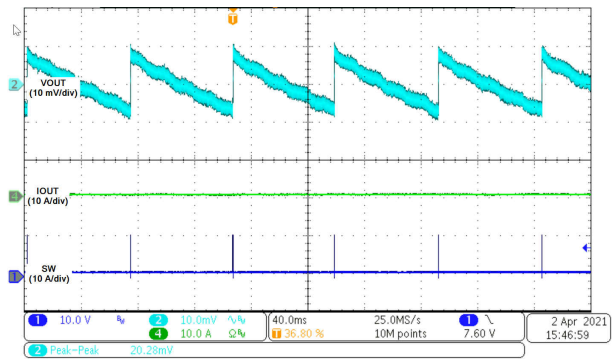
I_{OUT} = 0 A FCCM

图 8-26. Output Voltage Ripple, V_{RIPPLE} = 6.4 mV



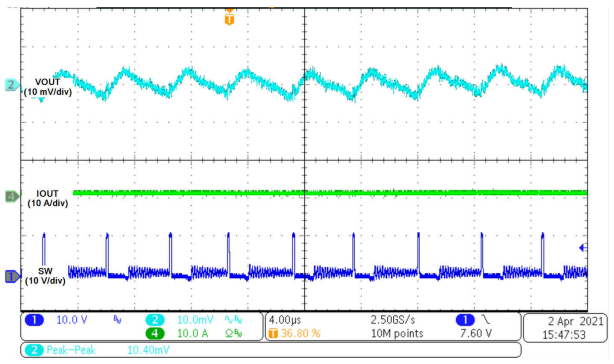
I_{OUT} = 15 A FCCM

图 8-27. Output Voltage Ripple, V_{RIPPLE} = 7.6 mV



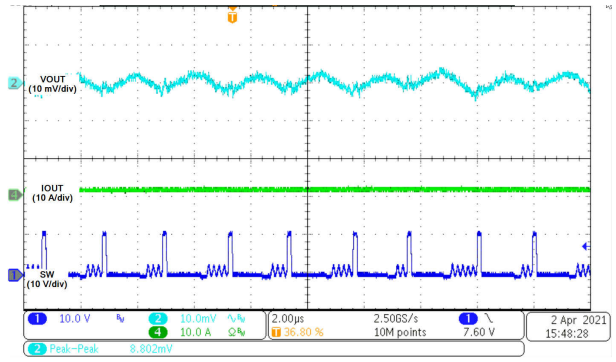
I_{OUT} = 0 A DCM

图 8-28. Output Voltage Ripple, V_{RIPPLE} = 20.3 mV



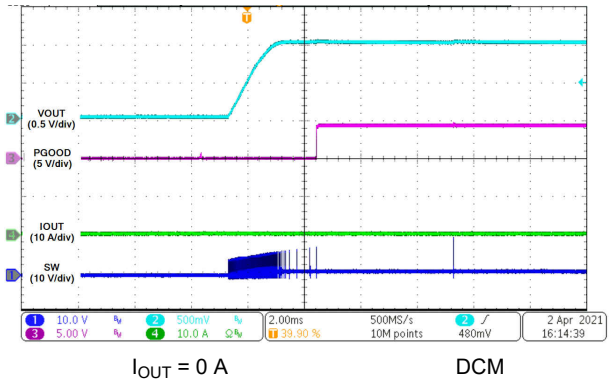
I_{OUT} = 0.5 A DCM

图 8-29. Output Voltage Ripple, V_{RIPPLE} = 10.4 mV



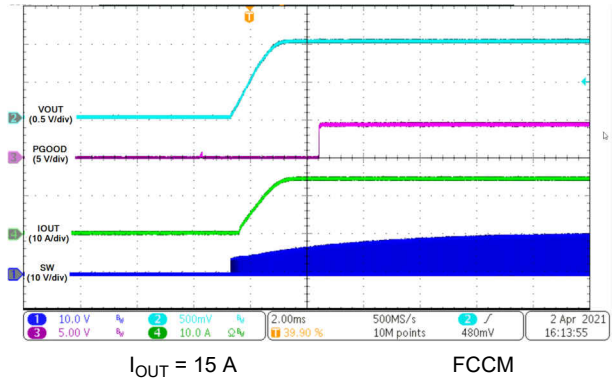
I_{OUT} = 1 A DCM

图 8-30. Output Voltage Ripple, V_{RIPPLE} = 8.8 mV



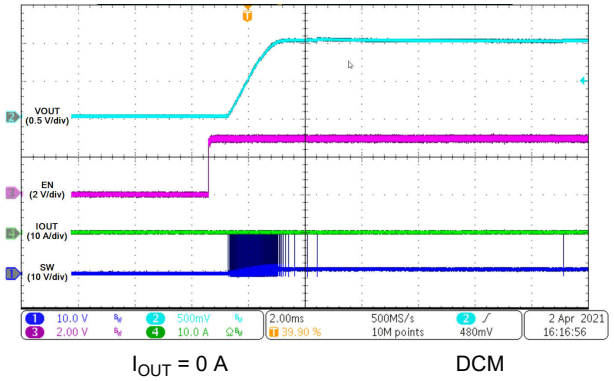
I_{OUT} = 0 A DCM

图 8-31. Startup Through V_{IN} (Enable Floating)



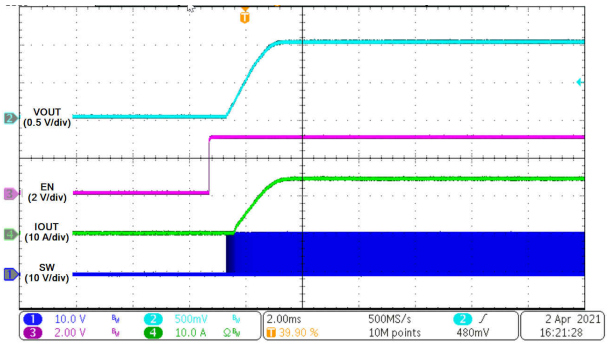
I_{OUT} = 15 A FCCM

图 8-32. Startup Through V_{IN} (Enable Floating)



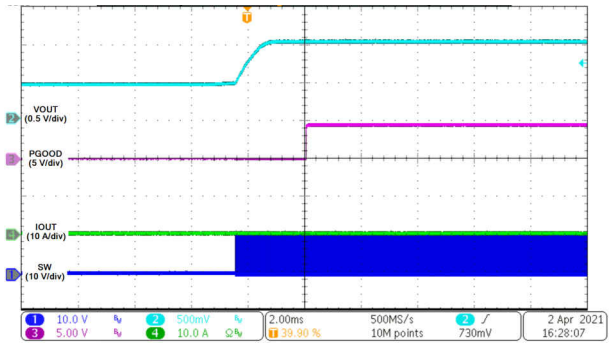
I_{OUT} = 0 A DCM

图 8-33. Startup Through Enable



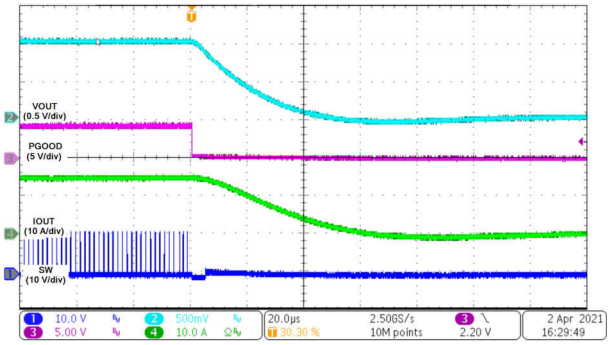
I_{OUT} = 15 A FCCM

图 8-34. Startup Through Enable



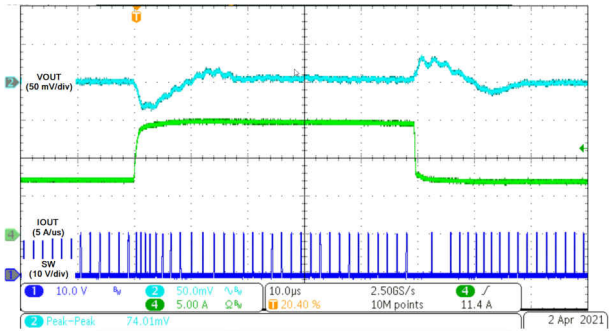
I_{OUT} = 0 A FCCM

图 8-35. Startup Through Enable into Prebiased Load



I_{OUT} = 15 A FCCM

图 8-36. Shutdown Through Enable



I_{STEP} = 7.5 A - 15 A - 7.5 A 5 A/ µ s

图 8-37. Transient Response, V_{PP} = 74 mV

9 Power Supply Recommendations

The devices are designed to operate from a wide input voltage supply range between 2.7 V and 16 V when the VCC pin is powered by an external bias ranging from 4.75 V to 5.3 V. Both input supplies (VIN and VCC bias) must be well regulated. Proper bypassing of input supplies (VIN and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in 节 10.

10 Layout

10.1 Layout Guidelines

Before beginning a design using one of the devices, consider the following:

- Place the input and output capacitors on the top side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- At least thirteen PGND vias are required to be placed as close as possible to the PGND pins (pins 1, 20, 21, 22, 24, and 25). This minimizes parasitic impedance and also lowers thermal resistance.
- Always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location should be a pair of PCB traces with at least 12-mil trace width, and should implement Kelvin sensing across a high bypass capacitor of 0.1 μF or higher. The ground connection of the remote sensing signal must be connected to the VSNS– pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at the VSNS– pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines should stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. And it is recommended to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the higher FB resistor to a high-frequency local bypass capacitor of 0.1-μF or higher, and short VSNS– to AGND with shortest trace.
- Pin 8 (AGND pin) must be connected to a solid PGND plane at a single point. Use the common AGND via to connect the TRIP and MODE resistors to the inner ground plane if applicable. Pin 14 is also an AGND pin, and is connected internally to pin 8. No external connection between pins 8 and 14 is required, however, pin 8 must be used as the AGND connection.
- See 图 10-1 for the layout recommendation.

10.2 Layout Example

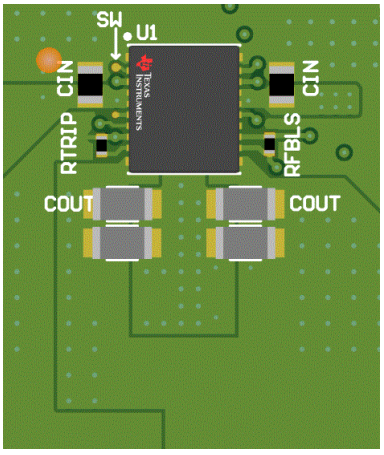


图 10-1. Recommended Layout Top Side

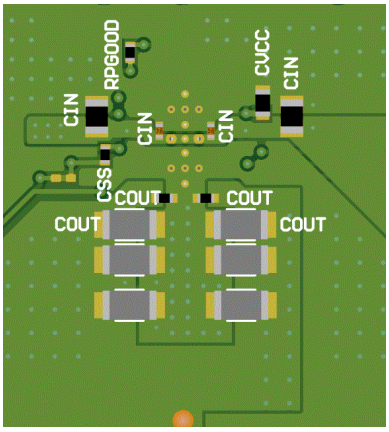


图 10-2. Recommended Layout Bottom Side

10.2.1 Thermal Performance on the TI EVM

Test conditions: f_{SW} = 600 kHz, V_{IN} = 12 V, V_{OUT} = 1 V, I_{OUT} = 15 A, C_{OUT} = 8 × 47 μF (1206/6.3V/X7R), IC: 82.5°C

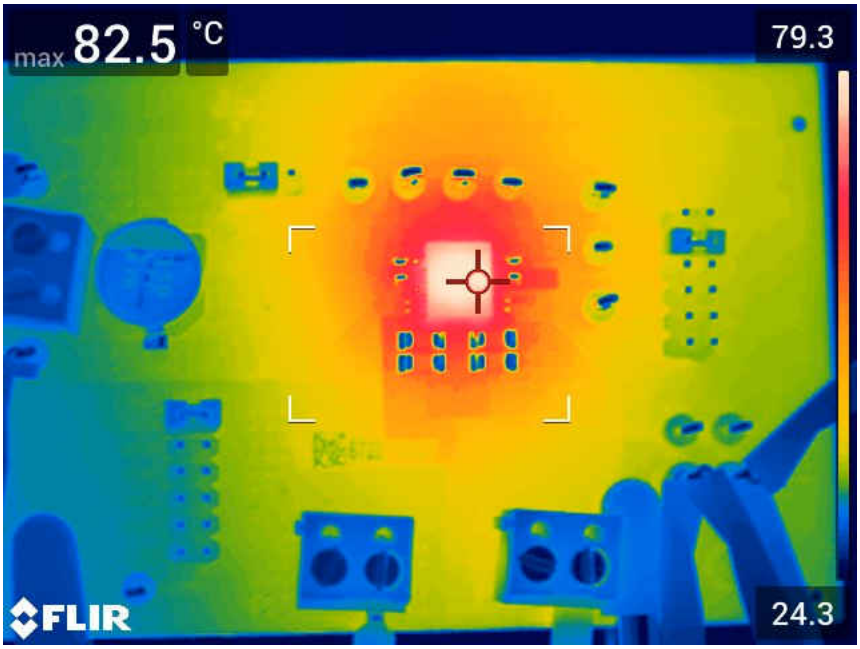


图 10-3. Thermal Image at 25°C Ambient, 12 Vin, 1 Vout, 15 A, 600 kHz

Test conditions:

f_{SW} = 600 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 12 A, C_{OUT} = 8 × 47 µF (1206/6.3V/X7R)

IC: 88.7°C

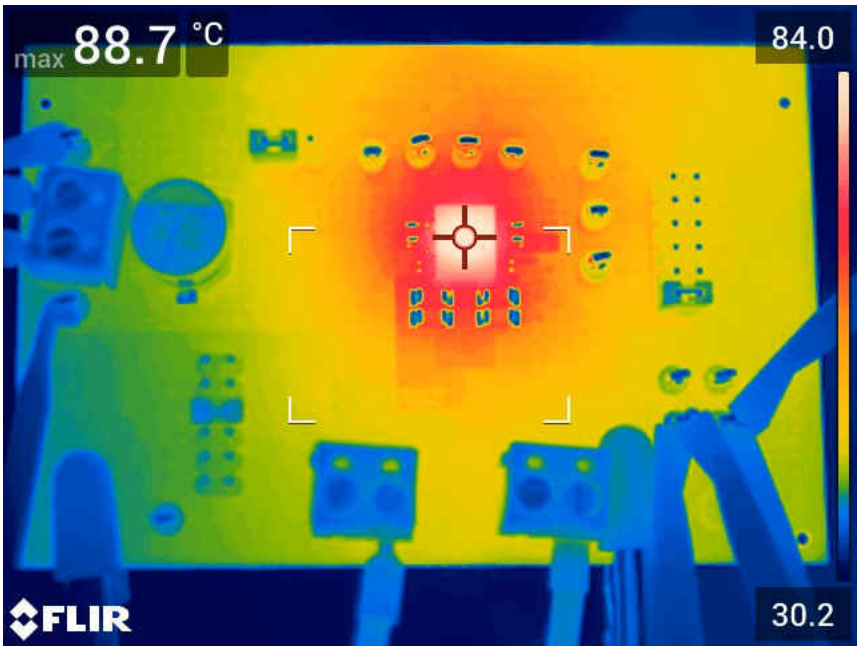


图 10-4. Thermal Image at 25°C Ambient, 12 Vin,5 Vout, 12 A, 600 kHz

10.3 EMI

The TPSM8A28 and TPSM8A29 are compliant with EN55011 Class-A radiated emissions. Figure 11-1 and Figure 11-2 show examples of radiated emissions plots. The graphs include the plots of the antenna in the horizontal and vertical positions.

The EMI plots were measured using the standard TPSM8A29EVM with Ferrite 61 type beads on the input wire.

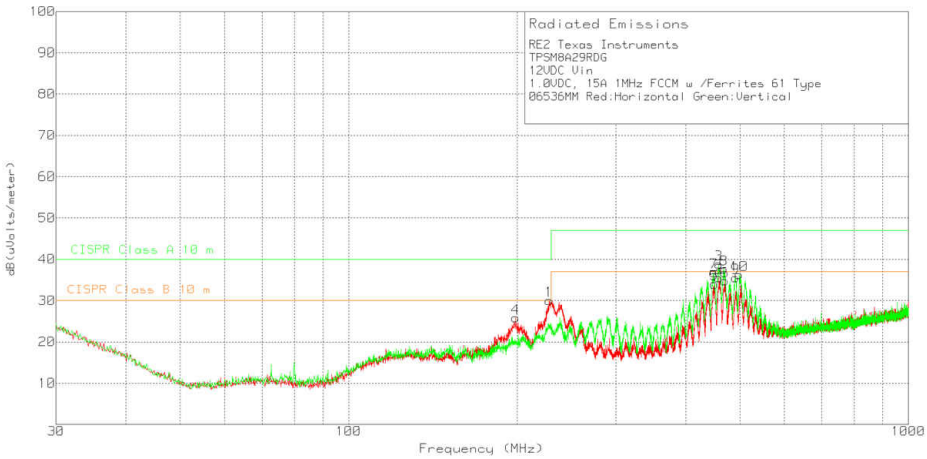


图 10-5. Radiated Emissions 12-V Input, 1.0-V Outputs, 15-A/Output Load

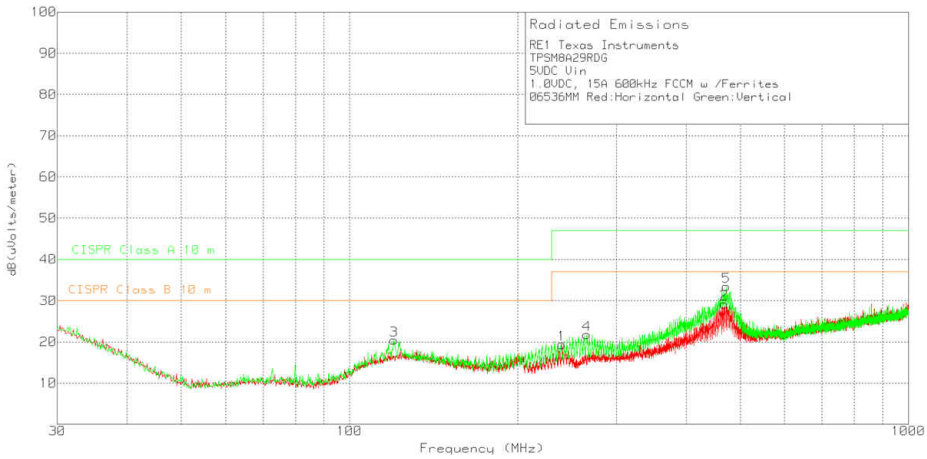


图 10-6. Radiated Emissions 5-V Input, 1-V Output, 15-A/Output Load

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.2 Documentation Support

11.2.1 Related Documentation

Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor Application Report

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM8A28RDGR	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A28
TPSM8A28RDGR.A	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A28
TPSM8A28RDGR.B	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM8A28RDGRG4	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A28
TPSM8A28RDGRG4.A	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A28
TPSM8A29RDGR	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A29
TPSM8A29RDGR.A	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A29
TPSM8A29RDGR.B	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM8A29RDGRG4	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A29
TPSM8A29RDGRG4.A	Active	Production	B3QFN (RDG) | 25	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 125	TPSM8A29

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

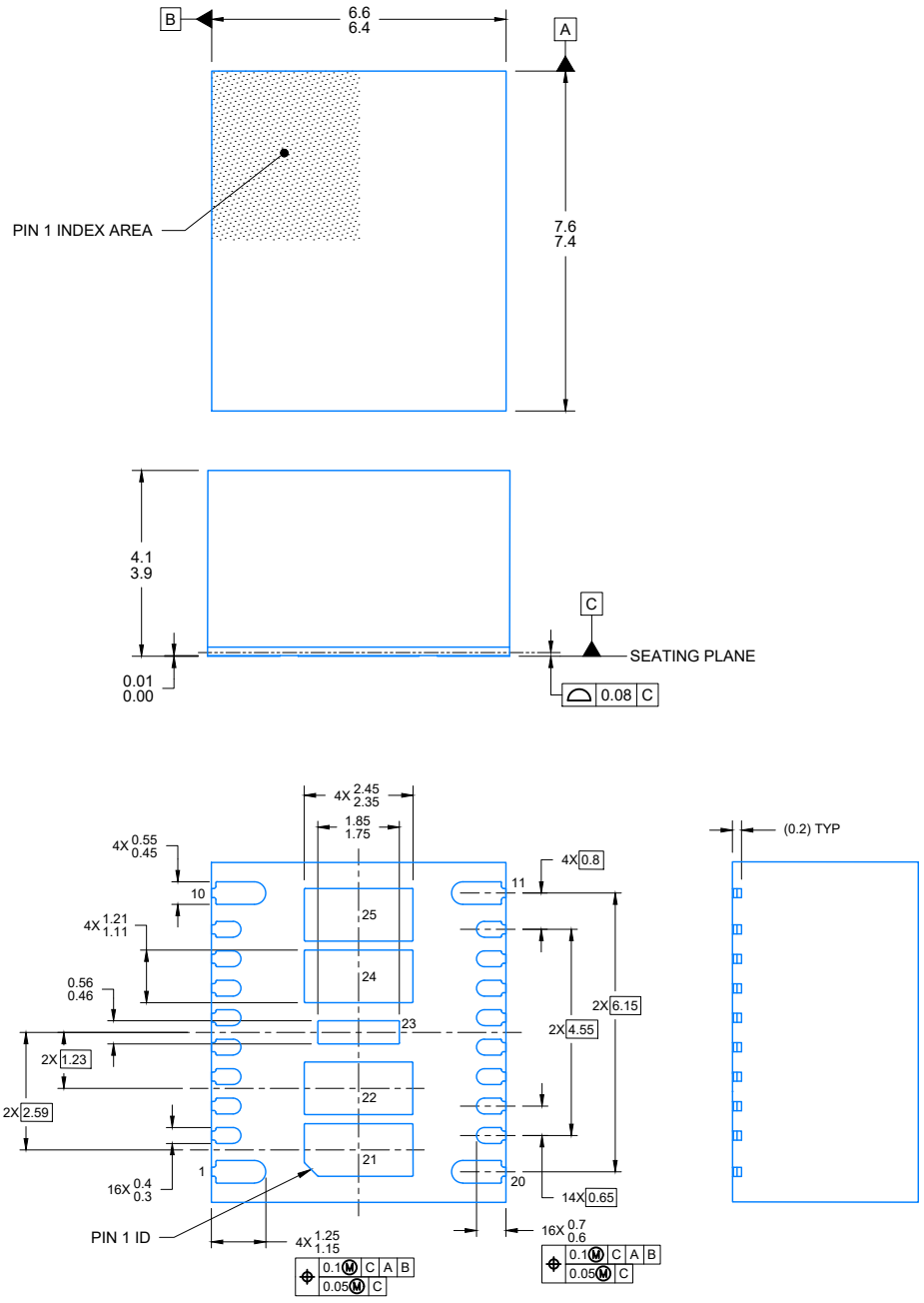
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RDG0025A

B3QFN - 4.1 mm max height

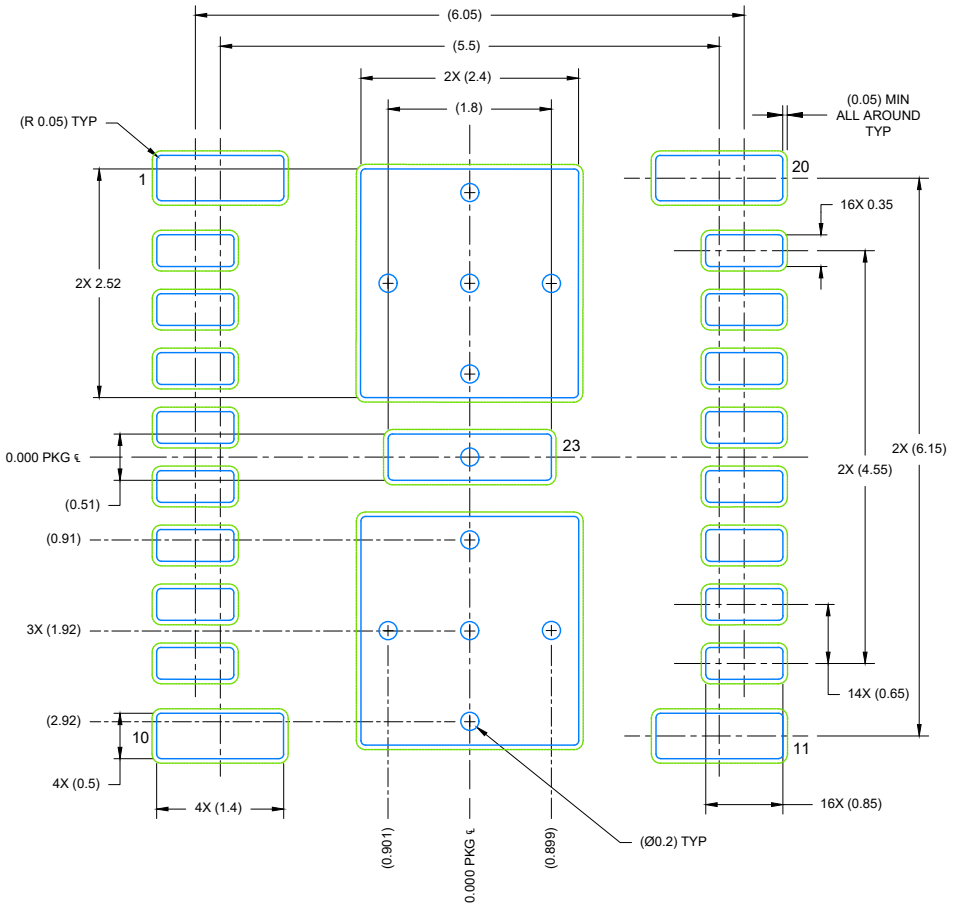
PLASTIC QUAD FLAT PACK- NO LEAD



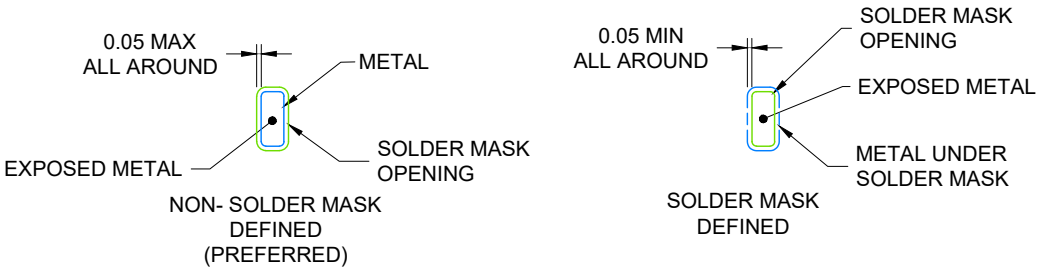
4226094/A 08/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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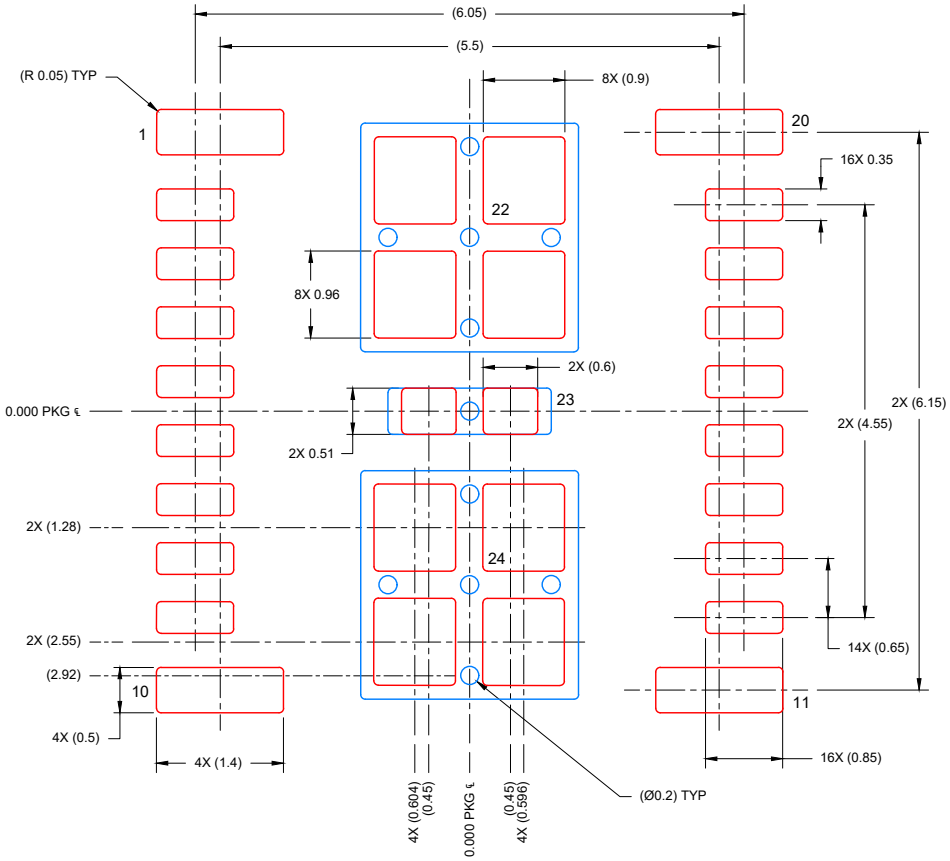
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE:
PIN 21 & 22 : 57%
PIN 23 : 67%
PIN 24 & 25 : 57%

SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月