TRS232E 具有 IEC61000-4-2 保护的双路 RS-232 驱动器和接收器

1 特性

- 符合或超出 TIA/RS-232-F 和 ITU 建议 V.28 的要求
- 通过带 1µF 电荷泵电容器的单个 5V 电源供电
- 速率高达 250kbit/s
- 两个驱动器和两个接收器
- ±30V 输入电平
- 低电源电流：8mA（典型值）
- 为 RS-232 总线引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC61000-4-2 接触放电
  - ±15kV IEC61000-4-2 气隙放电

2 应用

- TIA/RS-232-F
- 电池供电型系统
- 端子
- 调制解调器
- 计算机

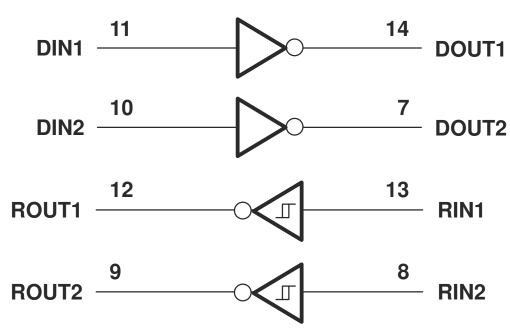
3 说明

TRS232E 是一款双路驱动器/接收器，它包含一个电容式电压发生器，可通过单个 5V 电源提 TIA/RS-232-F 电压电平。每个接收器都将 TIA/RS-232-F 输入转换为 5V TTL/CMOS 电平。该接收器的典型阈值为 1.3V，典型迟滞为 0.5V，可接受 ±30V 输入。每个驱动器都将 TTL/CMOS 输入电平转换为 TIA/RS-232-F 电平。德州仪器 (TI) LinASIC™ 库中的驱动器、接收器和电压发生器功能均以单元形式提供。

封装信息

器件型号	封装(1)	封装尺寸(2)
TRS232E	SOIC（D，16）	9.9mm x 6mm
	SOIC（DW，16）	10.4mm x 10.3mm
	PDIP（N，16）	19.3mm x 9.4mm
	TSSOP（PW，16）	5mm x 6.4mm

(1) 如需更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

Table of Contents

4 Pin Configuration and Functions

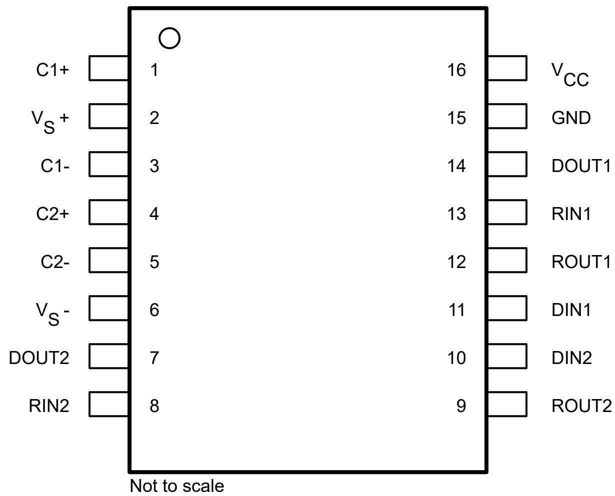


图 4-1. D, DW, N, NS or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
C1+	1	—	Positive lead of C1 capacitor
V_S+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
V_S-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CC}	Input supply voltage range[(2)]		–0.3	6	V
V_{S+}	Positive output supply voltage range		V_{CC} – 0.3	15	V
V_{S-}	Negative output supply voltage range		–0.3	–15	V
V_I	Input voltage range	Driver	–0.3	V_{CC} + 0.3	V
		Receiver		±30	
V_O	Output voltage range	DOUT	V_{S-} – 0.3	V_{S+} + 0.3	V
		ROUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	DOUT		Unlimited	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

PARAMETER	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
T_A	Operating free-air temperature	TRS232EC	0		70	°C
		TRS232EI	–40		85	

5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.7	60.6	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.	27.5	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [1] and 图 8-1)

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V,	All outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1 – C4 = 1 μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

5.6 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range[1]

PARAMETER			TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	R_L = 3kΩ to GND		5	7		V
V_{OL}	Low-level output voltage[3]	DOUT	R_L = 3kΩ to GND			–7	–5	V
r_o	Output resistance	DOUT	V_{S+} = V_{S-} = 0,	V_O = ±2V	300			Ω
I_{OS} [4]	Short-circuit output current	DOUT	V_{CC} = 5.5V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	DIN	V_I = 0				200	μA

(1) Test conditions are C1 – C4 = 1 μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

5.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3kΩ to 7kΩ, See 图 6-2			30	V/μs
SR(t)	Driver transition region slew rate	See 图 6-3		3		V/μs
	Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are C1 – C4 = 1 μF at V_{CC} = 5V ± 0.5V.

5.8 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range [(1)]

PARAMETER			TEST CONDITIONS		MIN	TYP[(2)]	MAX	UNIT
V_{OH}	High-level output voltage	ROUT	I_{OH} = –1mA		3.5			V
V_{OL}	Low-level output voltage[(3)]	ROUT	I_{OL} = 3.2mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V_{CC} = 5V		0.2	0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5V,	T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 1 μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

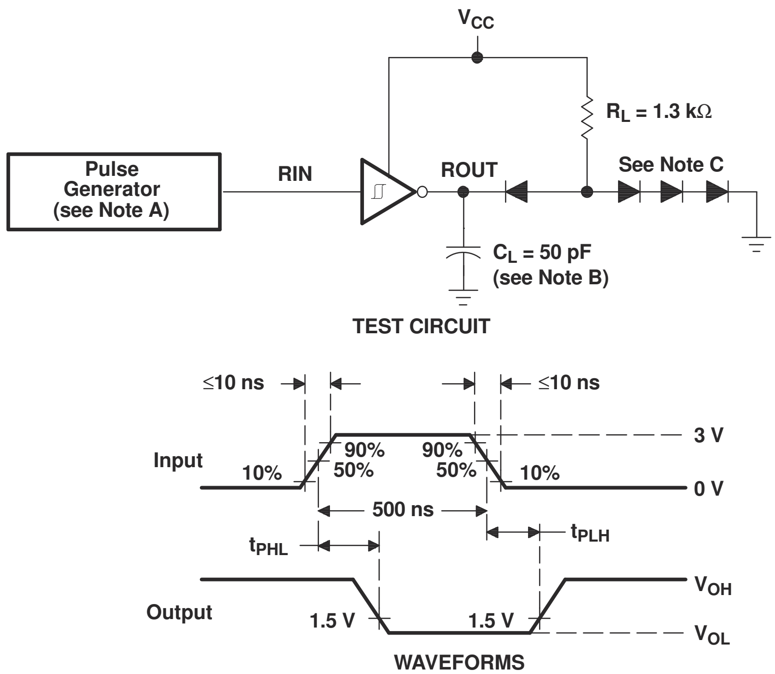
5.9 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see [(1)] and 图 6-1)

PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

(1) Test conditions are C1 – C4 = 1 μF at V_{CC} = 5V ± 0.5V.

6 Parameter Measurement Information

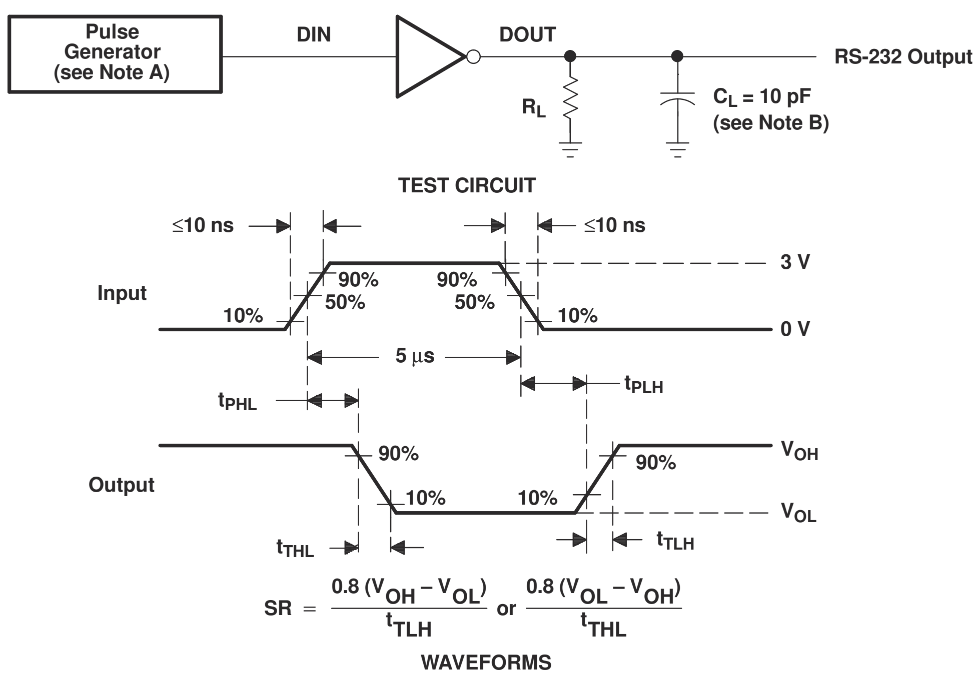


A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or equivalent.

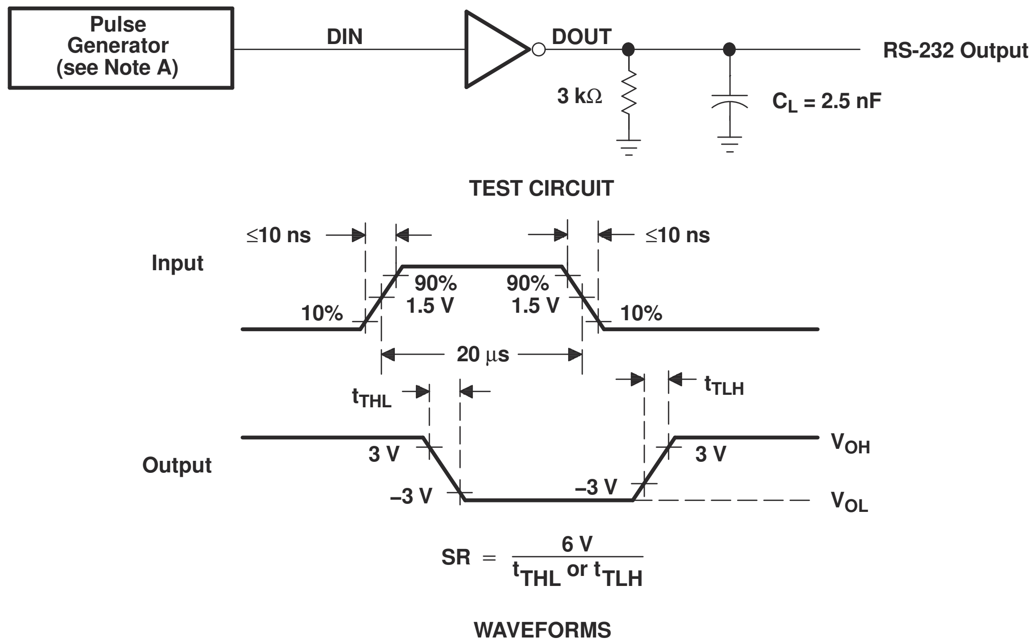
图 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

B. C_L includes probe and jig capacitance.

图 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5 µs Input)



A. The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

图 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20 μ s Input)

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Tables: Each Driver

INPUT(1) DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 7-2. Each Receiver

INPUT(1) RIN	OUTPUT ROUT
L	H
H	L

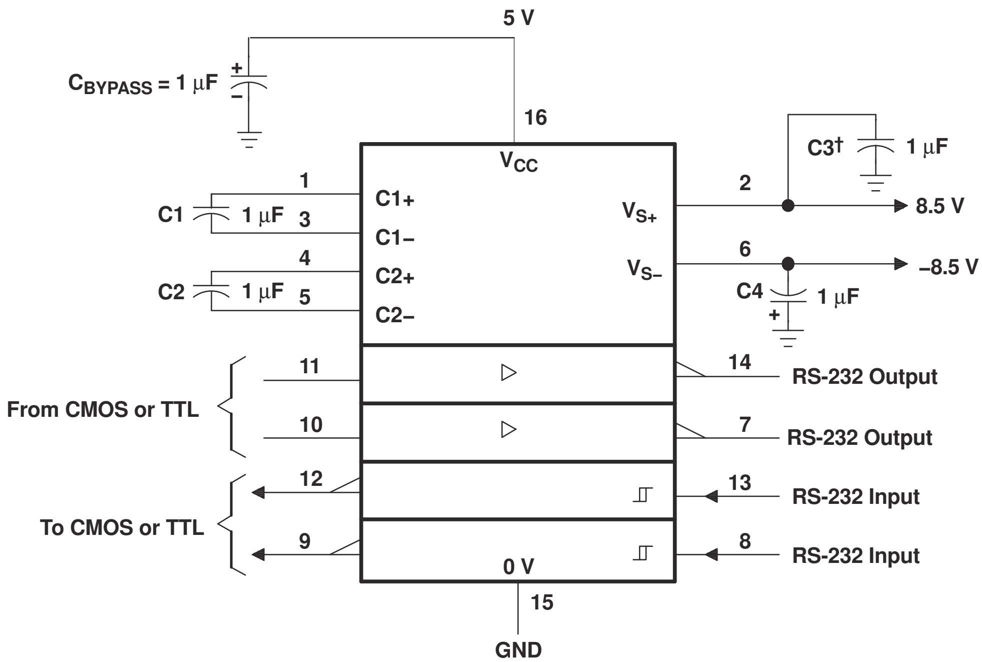
(1) H = high level, L = low level

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1 µ F capacitors shown, the TRS202E can operate with 0.1 µ F capacitors.

图 8-1. Typical Operating Circuit

9 Device Documentation and Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 商标

LinASIC™ and TI E2E™ are trademarks of Texas Instruments.
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9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2021) to Revision E (February 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision C (September 2008) to Revision D (March 2021)	Page
• 将*逻辑图* 移至第 1 页	1
• 删除了*订购信息* 表	1
• 添加了删除的*封装信息* 表	1
• 更改了*封装信息* 表	1
• Moved the *Function Tables* to the *Parameter Measurement Information* section	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS232ECD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECDWR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	TRS232EC	
TRS232ECPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	0 to 70	RU32EC	
TRS232EID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	TRS232EI	
TRS232EIDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	TRS232EI	
TRS232EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI	Samples
TRS232EIN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 85	TRS232EIN	
TRS232EIPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	RU32EI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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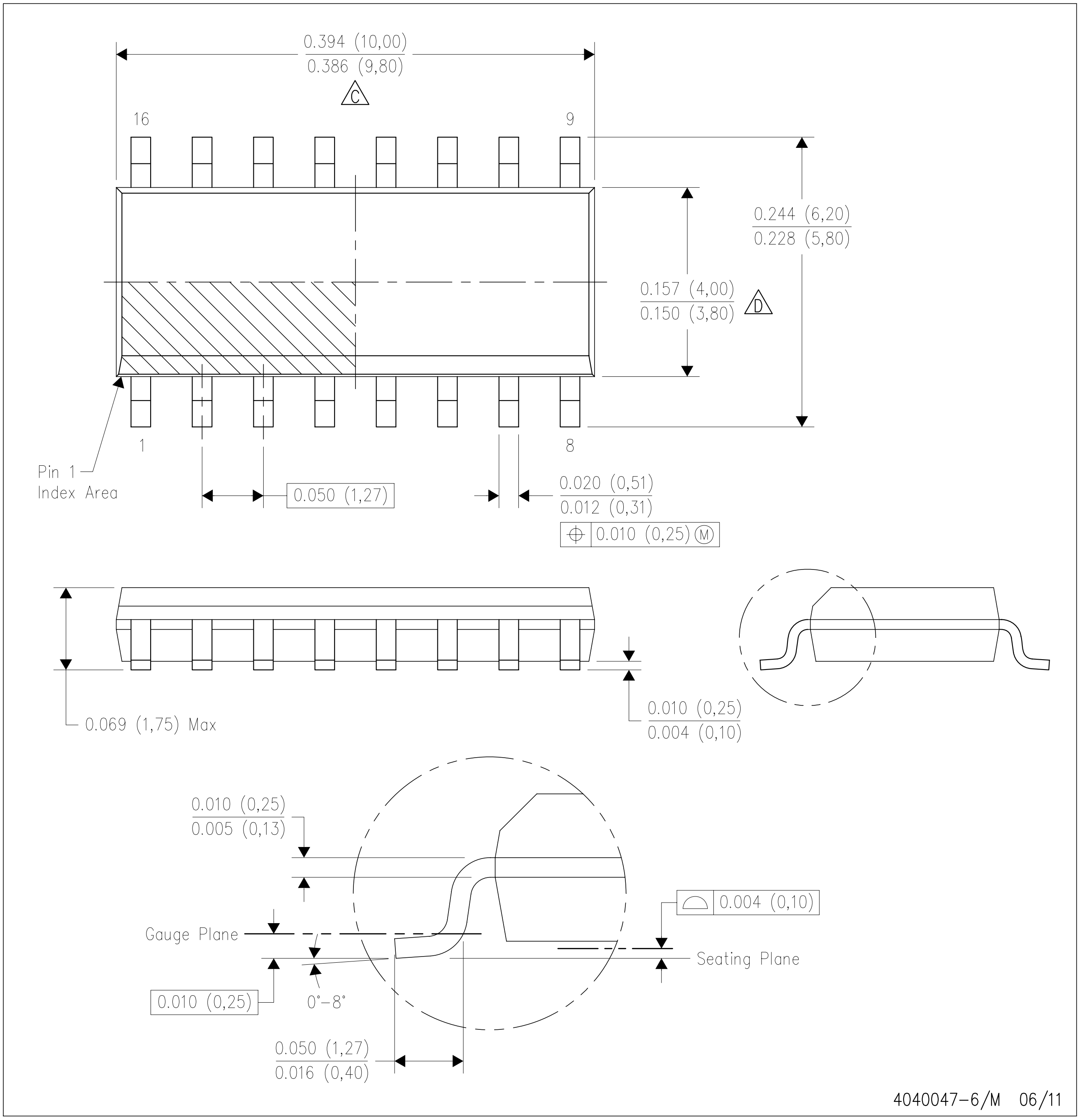
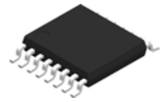
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



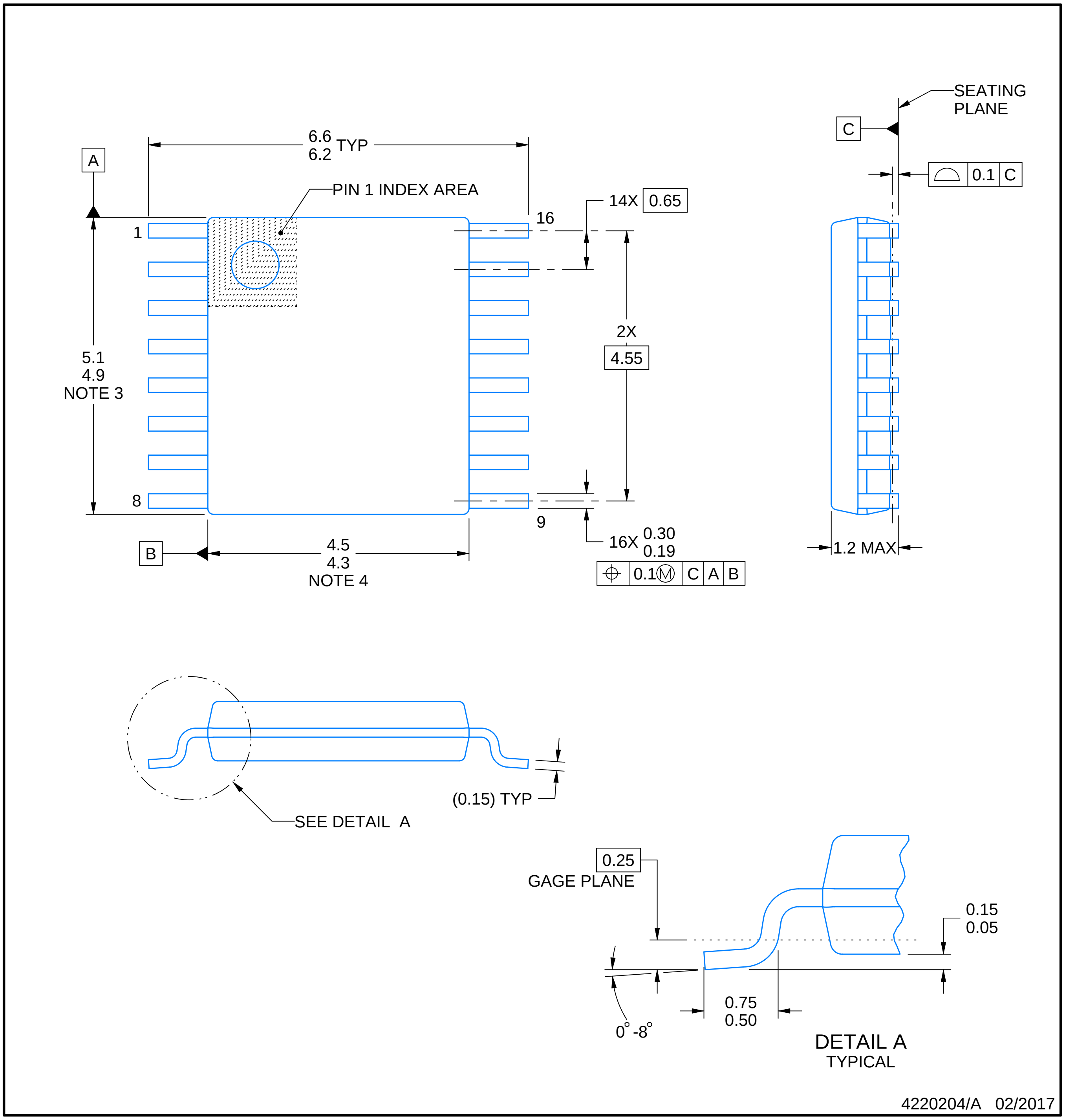
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.



PW0016A

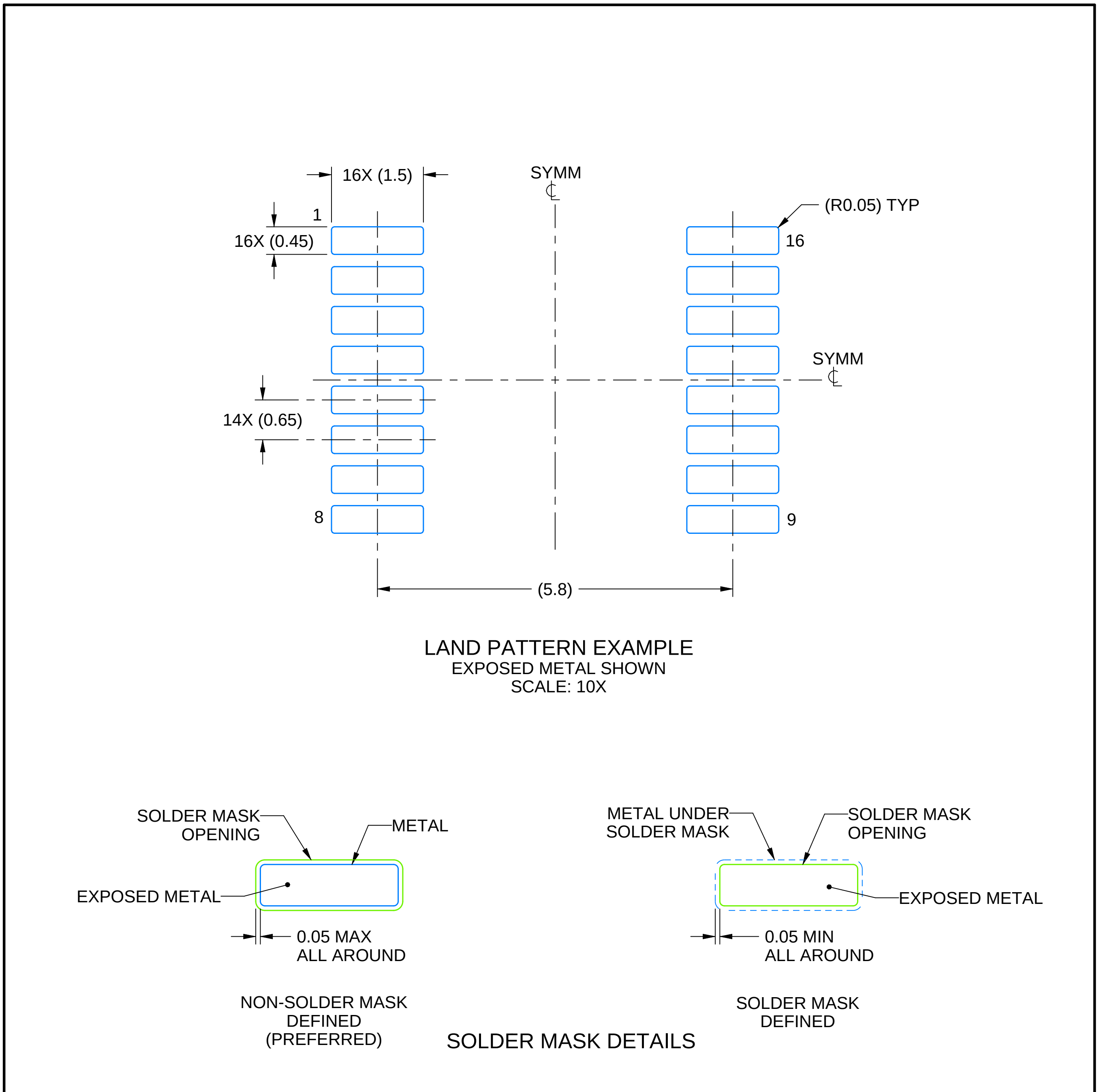
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

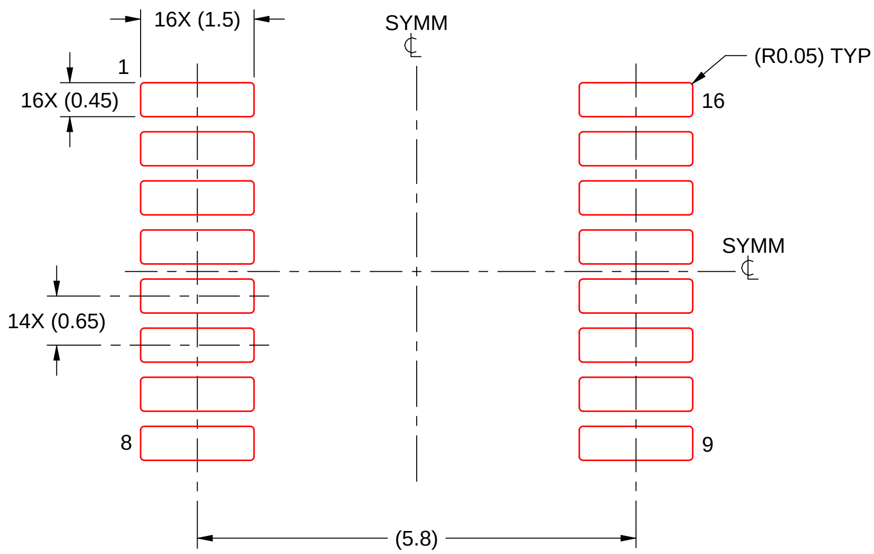
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



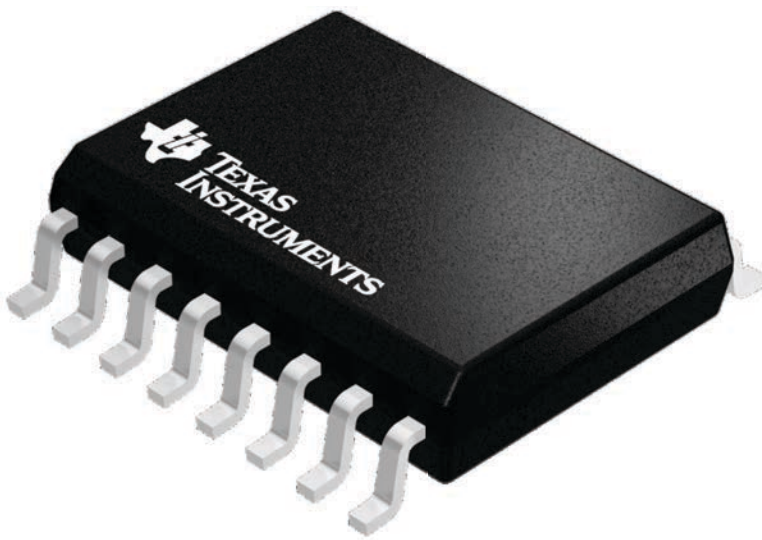
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

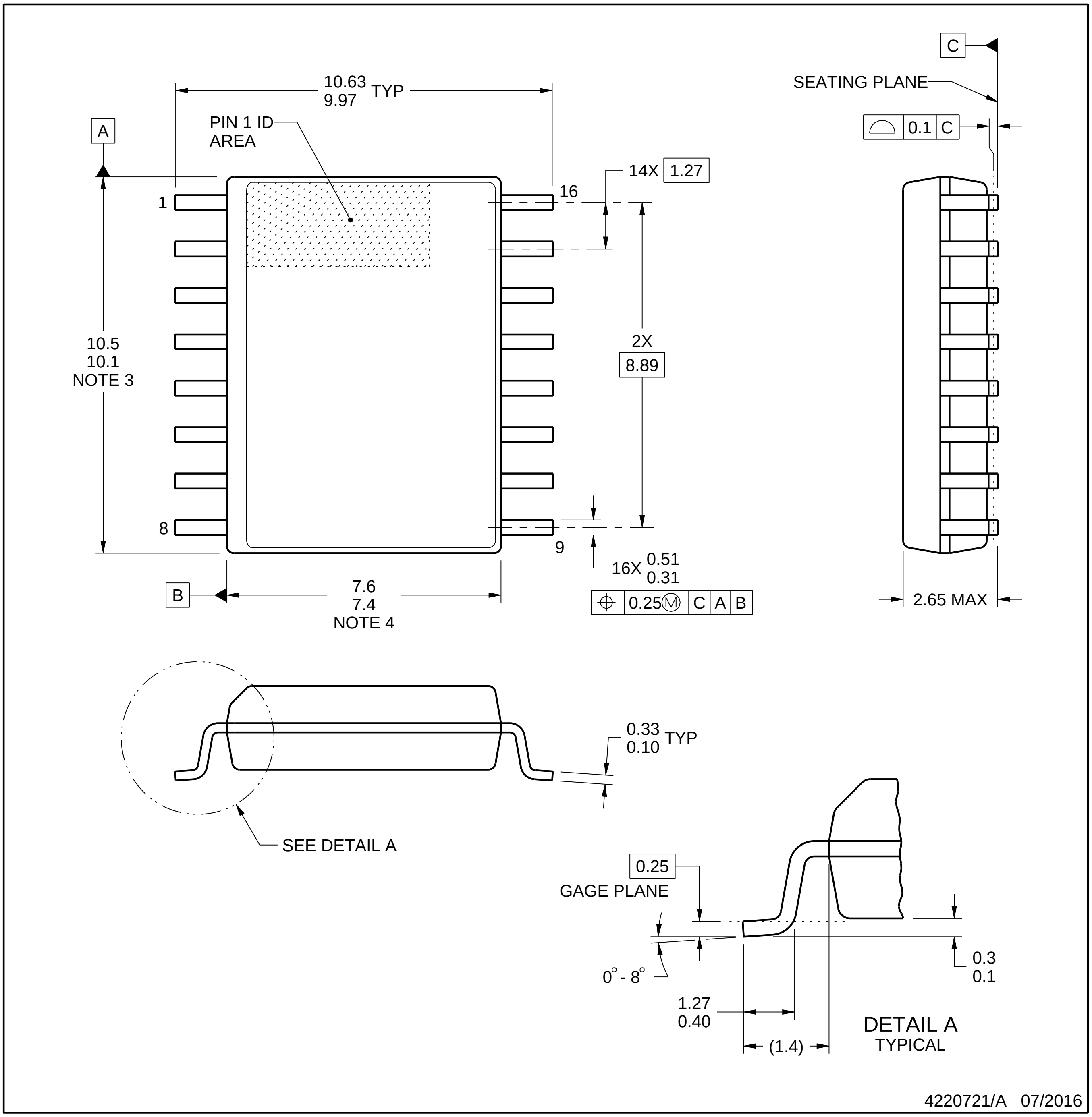
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

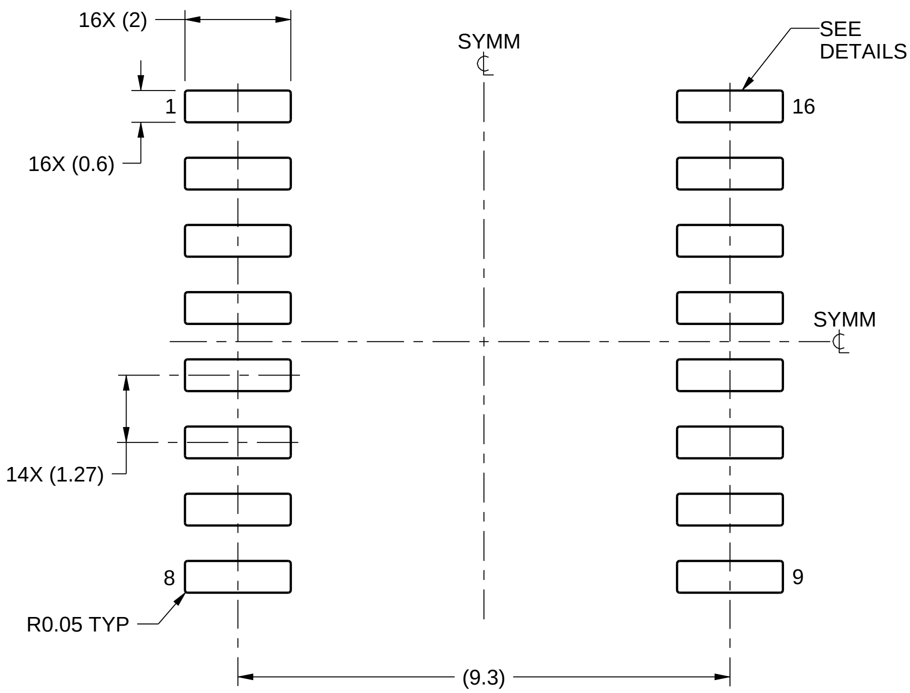
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



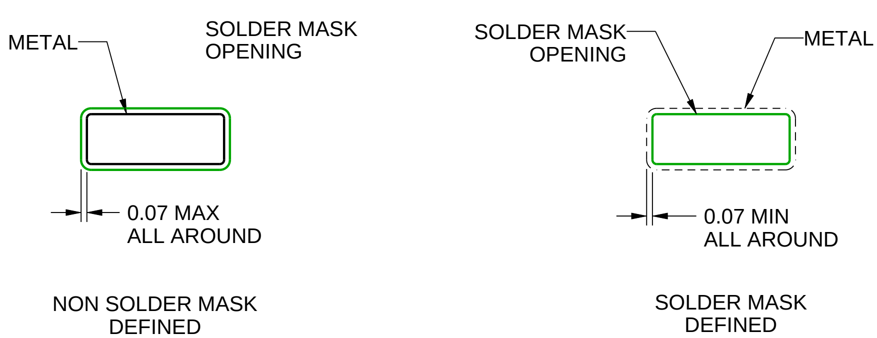


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

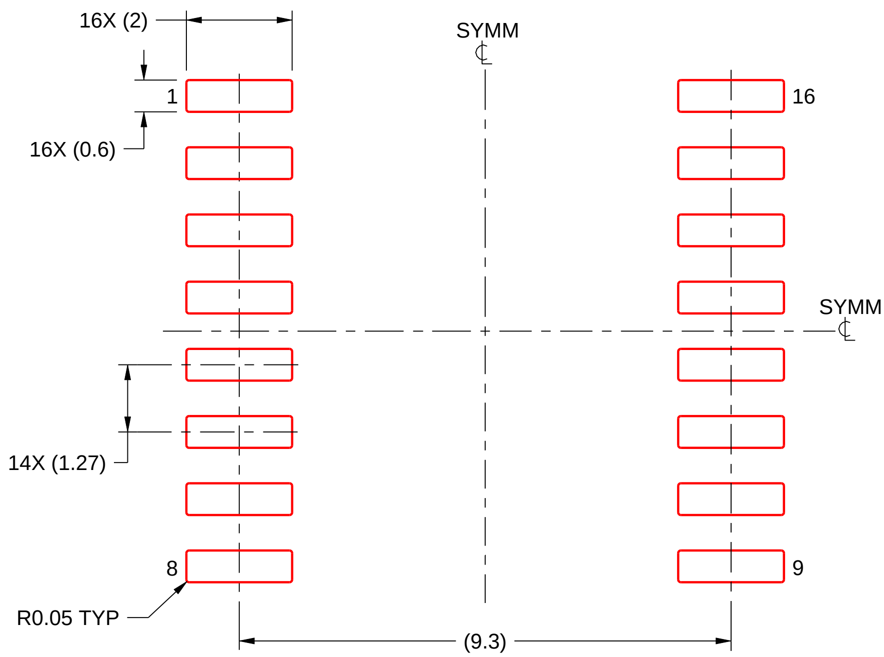


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

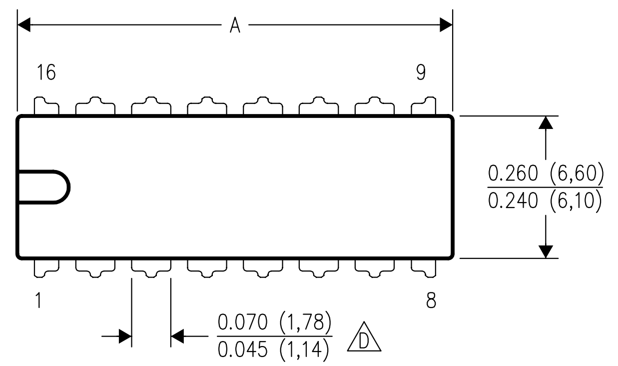
4220721/A 07/2016

NOTES: (continued)

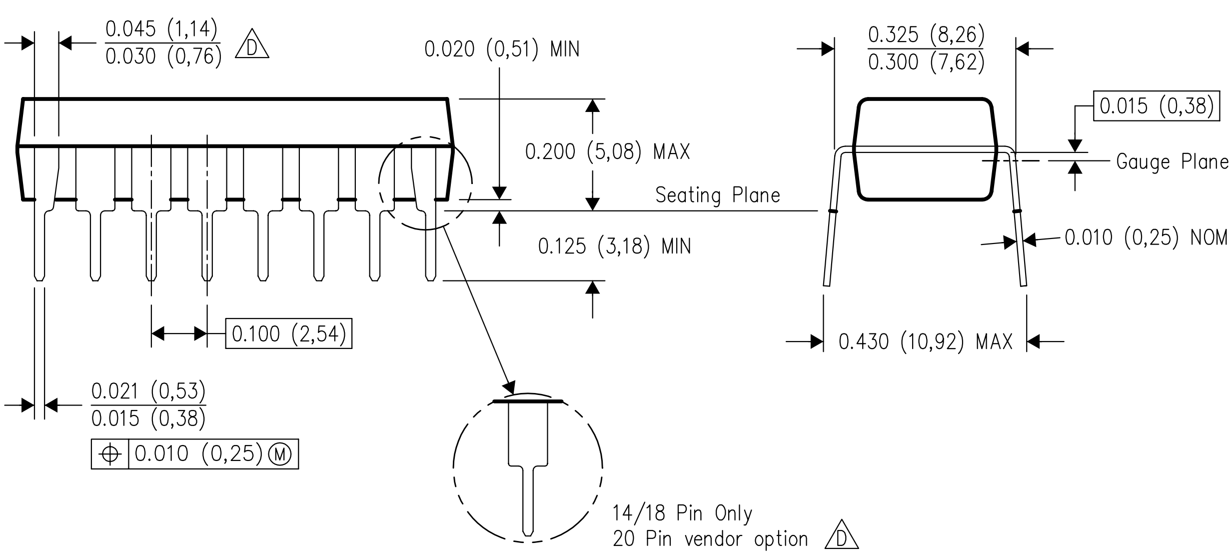
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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