

## 适用于 DDR3 应用的 12 通道，1:2 多路复用器 / 多路解复用器开关

 查询样品: **TS3DDR3812**

### 特性

- 与 DDR3 SDRAM 标准 (JESD79-3D) 兼容
- 1.675GHz 的宽带宽
- 低传播延迟 (典型值  $t_{pd} = 40ps$ )
- 低位到位偏斜 (典型值  $t_{sk(o)} = 6ps$ )
- 低而平坦的导通电阻 (典型值  $r_{ON} = 8\Omega$ )
- 低输入 / 输出电容 (典型值  $C_{ON} = 5.6pF$ )
- 低串扰 ( $X_{TALK} = -43dB$ , 这是在 250MHz 时的典型值)
- 3V 至 3.6V 的  $V_{CC}$  工作范围
- 数据 I/O 端口上的轨至轨开关 (0 至  $V_{CC}$ )
- 用于上部及下部 6 通道的分离开关控制逻辑
- 专用使能逻辑电路支持高阻抗 (Hi-Z) 模式
- $I_{关闭}$  保护防止断电状态 ( $V_{CC} = 0V$ ) 下的电流泄漏
- 静电放电 (ESD) 性能测试符合 JESD22 标准
  - 2000V 人体模型 (A114B, II 类)
  - 1000V 充电器件模型 (C101)
- 42 引脚 RUA 封装 (9mm × 3.5mm, 0.5mm 焊球间距)

### 应用范围

- DDR3 信号开关
- DIMM 模块
- 笔记本 / 台式机
- 服务器

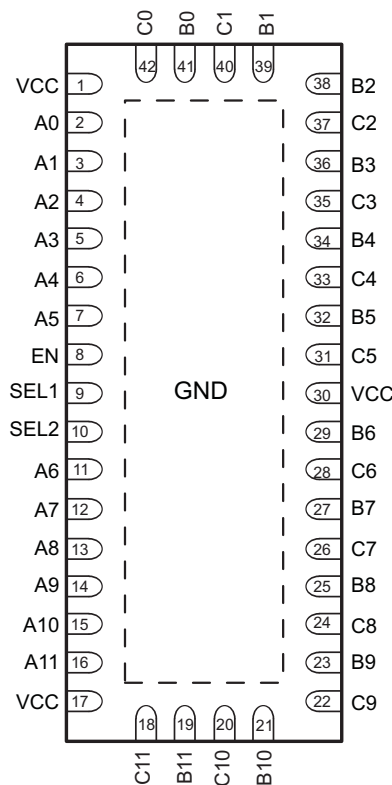
### 说明

TS3DDR3812 是一款专门针对 DDR3 应用而设计的 12 通道，1:2 多路复用器 / 多路解复用器开关。该产品采用 3 至 3.6V 电源供电，提供低而平坦的导通状态电阻以及低 I/O 电容，从而可实现 1.675GHz 的典型带宽。

通道  $A_0$  至  $A_{11}$  分为两个 6 位组，可通过两组名为 SEL1 与 SEL2 的数字输入进行独立控制。这些选择输入可控制每个 6 位 DDR3 信号源的开关位置，使它们能够准确发送至两个端点中的一个。此外，本开关还可用于将单个端点与两个 6 位 DDR3 信号源中的一个连接起来。对于 12 位 DDR3 信号源的开关，只需外部连接 SEL1 与 SEL2，便可通过一个单个 GPIO 输入控制所有 12 个通道。一个 EN 输入可在不使用时使整个芯片处于高阻抗 (Hi-Z) 状态。

这些特性使 TS3DDR3812 成为存储器、模拟 / 数字视频、局域网 (LAN) 以及其它高速信号开关应用中的理想选择。

图 1. RUA 封装  
(顶视图)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

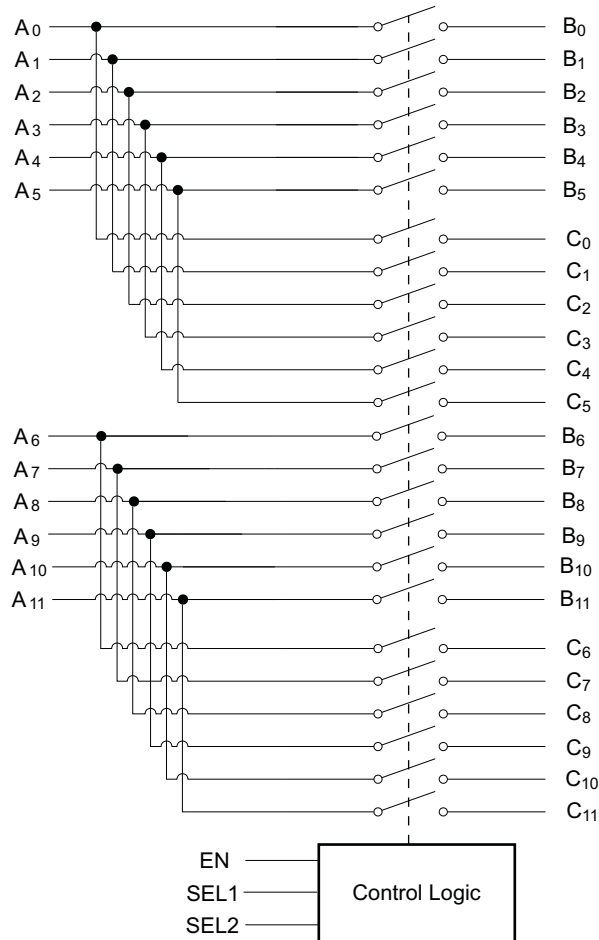


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ORDERING INFORMATION**

For package and ordering information, see the Package Option Addendum at the end of this document.

**Figure 2. LOGIC DIAGRAM**



**FUNCTION TABLE**

EN	SEL1	SEL2	FUNCTION
L	X	X	A <sub>0</sub> to A <sub>11</sub> , B <sub>0</sub> to B <sub>11</sub> , and C <sub>0</sub> to C <sub>11</sub> are Hi-Z
H	L	L	A <sub>0</sub> to A <sub>5</sub> = B <sub>0</sub> to B <sub>5</sub> and A <sub>6</sub> to A <sub>11</sub> = B <sub>6</sub> to B <sub>11</sub>
H	L	H	A <sub>0</sub> to A <sub>5</sub> = B <sub>0</sub> to B <sub>5</sub> and A <sub>6</sub> to A <sub>11</sub> = C <sub>6</sub> to C <sub>11</sub>
H	H	L	A <sub>0</sub> to A <sub>5</sub> = C <sub>0</sub> to C <sub>5</sub> and A <sub>6</sub> to A <sub>11</sub> = B <sub>6</sub> to B <sub>11</sub>
H	H	H	A <sub>0</sub> to A <sub>5</sub> = C <sub>0</sub> to C <sub>5</sub> and A <sub>6</sub> to A <sub>11</sub> = C <sub>6</sub> to C <sub>11</sub>

**TERMINAL FUNCTIONS**

PIN		DESCRIPTION
NAME	NUMBER	
V <sub>CC</sub>	1, 17, 30	Supply Voltage
GND	ThermalPad	Ground

**TERMINAL FUNCTIONS (continued)**

PIN		DESCRIPTION
NAME	NUMBER	
EN	8	Enable Input
SEL1	9	Select Input
SEL2	10	Select Input
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , A <sub>4</sub> , A <sub>5</sub> , A <sub>6</sub> , A <sub>7</sub> , A <sub>8</sub> , A <sub>9</sub> , A <sub>10</sub> , A <sub>11</sub>	2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16	Data I/Os
B <sub>0</sub> , B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub> , B <sub>5</sub> , B <sub>6</sub> , B <sub>7</sub> , B <sub>8</sub> , B <sub>9</sub> , B <sub>10</sub> , B <sub>11</sub>	41, 39, 38, 36, 34, 32, 29, 27, 25, 23, 21, 19	Data I/Os
C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>	42, 40, 37, 35, 33, 31, 28, 26, 24, 22, 20, 18	Data I/Os

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V
V <sub>I/O</sub>	Analog voltage range <sup>(2)(3)(4)</sup>	A, B, C	-0.5	7	V
V <sub>IN</sub>	Digital input voltage range <sup>(2)(3)</sup>	SEL1, SEL2	-0.5	7	V
I <sub>I/OK</sub>	Analog port diode current	V <sub>I/O</sub> < 0		-50	mA
I <sub>IK</sub>	Digital input clamp current	V <sub>IN</sub> < 0		-50	mA
I <sub>I/O</sub>	On-state switch current <sup>(5)</sup>	A, B, C	-128	128	mA
I <sub>DD</sub> , I <sub>GND</sub>	Continuous current through V <sub>DD</sub> or GND		-100	100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(6)</sup>	RUA package		31.8	°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

# TS3DDR3812

ZHCS134B – FEBRUARY 2011 – REVISED MAY 2013

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## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.6	V
V <sub>IH</sub>	High-level control input voltage	2	5.5	V
V <sub>IL</sub>	Low-level control input voltage	0	0.8	V
V <sub>IN</sub>	Input voltage	0	5.5	V
V <sub>I/O</sub>	Input/Output voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#)

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>	Digital input clamp voltage	SEL1, SEL2 V <sub>CC</sub> = 3.6 V, I <sub>IN</sub> = -18 mA	-1.2	-0.8		V
R <sub>ON</sub>	ON-state resistance	A, B, C V <sub>CC</sub> = 3 V, 1.5 V ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub> , I <sub>I/O</sub> = -40 mA		8	12	Ω
R <sub>ON(flat)</sub> <sup>(3)</sup>	ON-state resistance flatness	A, B, C V <sub>CC</sub> = 3 V, V <sub>I/O</sub> = 1.5 V and V <sub>CC</sub> , I <sub>I/O</sub> = -40 mA		1.5		Ω
ΔR <sub>ON</sub> <sup>(4)</sup>	On-state resistance match between channels	A, B, C V <sub>CC</sub> = 3 V, 1.5 V ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub> , I <sub>I/O</sub> = -40 mA		0.4	1	Ω
I <sub>IH</sub>	Digital input high leakage current	SEL1, SEL2 V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = V <sub>DD</sub>			±1	μA
I <sub>IL</sub>	Digital input low leakage current	SEL1, SEL2 V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = GND			±1	μA
I <sub>OFF</sub>	Leakage under power off conditions	All outputs V <sub>CC</sub> = 0 V, V <sub>I/O</sub> = 0 to 3.6 V, V <sub>IN</sub> = 0 to 5.5 V			±1	μA
C <sub>IN</sub>	Digital input capacitance	SEL1, SEL2 f = 1 MHz, V <sub>IN</sub> = 0 V		2.6	3.2	pF
C <sub>OFF</sub>	Switch OFF capacitance	A, B, C f = 1 MHz, V <sub>I/O</sub> = 0 V, Output is open, Switch is OFF		2		pF
C <sub>ON</sub>	Switch ON capacitance	A, B, C f = 1 MHz, V <sub>I/O</sub> = 0 V, Output is open, Switch is ON		5.6		pF
I <sub>CC</sub>	V <sub>CC</sub> supply current	V <sub>CC</sub> = 3.6 V, I <sub>I/O</sub> = 0, V <sub>IN</sub> = V <sub>DD</sub> or GND	300	400		μA

- (1) V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to I/O pins, V<sub>IN</sub> refers to the control inputs  
 (2) All typical values are at V<sub>CC</sub> = 3.3V (unless otherwise noted), T<sub>A</sub> = 25°C  
 (3) R<sub>ON(FLAT)</sub> is the difference of R<sub>ON</sub> in a given channel at specified voltages.  
 (4) ΔR<sub>ON</sub> is the difference of R<sub>ON</sub> from center port (A<sub>5</sub>, A<sub>6</sub>) to any other ports.

## SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $R_L = 200\ \Omega$ ,  $C_L = 4\text{ pF}$  (unless otherwise noted) (see [Figure 7](#) and [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}^{(2)}$	A or B,C	B,C or A		40		ps
$t_{PZH}, t_{PZL}$	SEL1	$A_{0-5}$ or $B_{0-5}, C_{0-5}$	2		7	ns
	SEL2	$A_{6-11}$ or $B_{6-11}, C_{6-11}$	2		7	ns
$t_{PHZ}, t_{PLZ}$	SEL1	$A_{0-5}$ or $B_{0-5}, C_{0-5}$	2		5	ns
	SEL2	$A_{6-11}$ or $B_{6-11}, C_{6-11}$	2		5	ns
$t_{sk(o)}^{(3)}$	A or B,C	B, C or A		6	30	ps
$t_{sk(p)}^{(4)}$	A or B, C	B, C or A		6	30	ps

- (1) All typical values are at  $V_{CC} = 3.3\text{V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .
- (2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- (3) Output skew between center port ( $A_5, A_6$ ) and any other channel.
- (4) Skew between opposite transitions of the same output  $|t_{PHL} - t_{PLH}|$

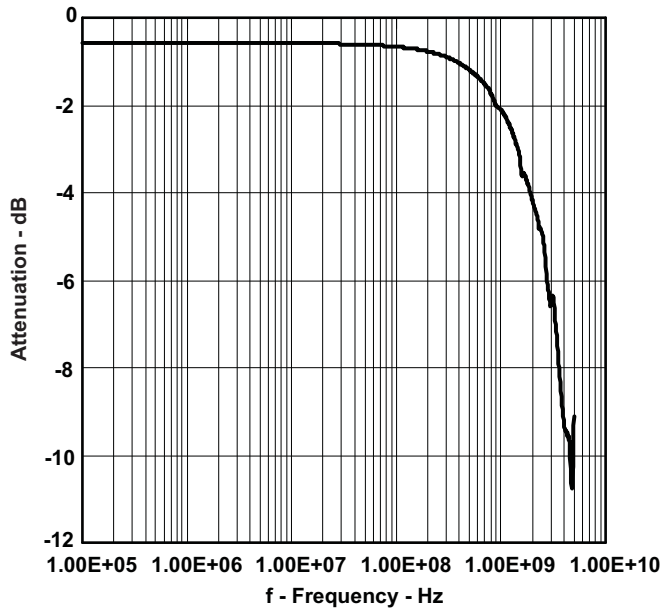
## DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

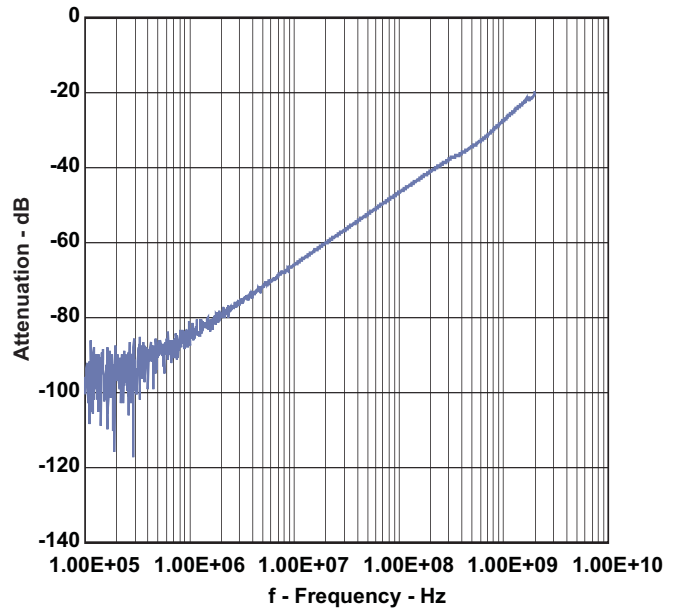
PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 250\text{ MHz}$ (see <a href="#">Figure 11</a> )	-43	dB
$O_{IRR}$	$R_L = 50\ \Omega$ , $f = 250\text{ MHz}$ (see <a href="#">Figure 12</a> )	-42	dB
BW	$R_L = 50\ \Omega$ , Switch ON (see <a href="#">Figure 10</a> )	1.675	GHz

- (1) All Typical Values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

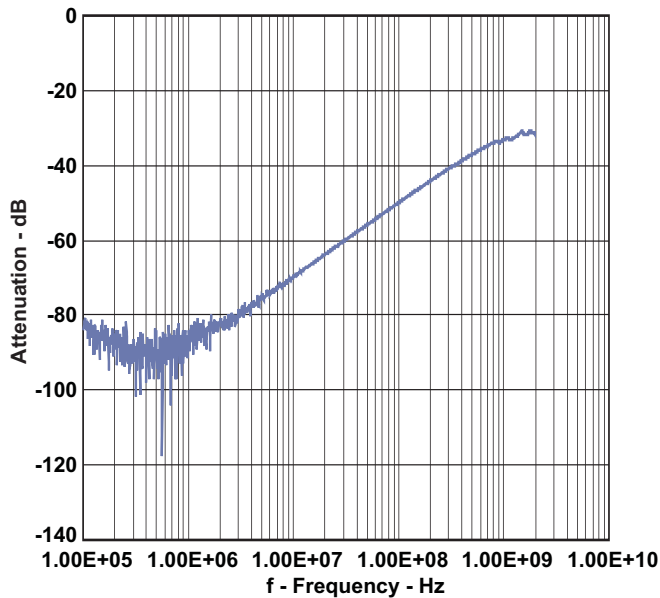
**OPERATING CHARACTERISTICS**



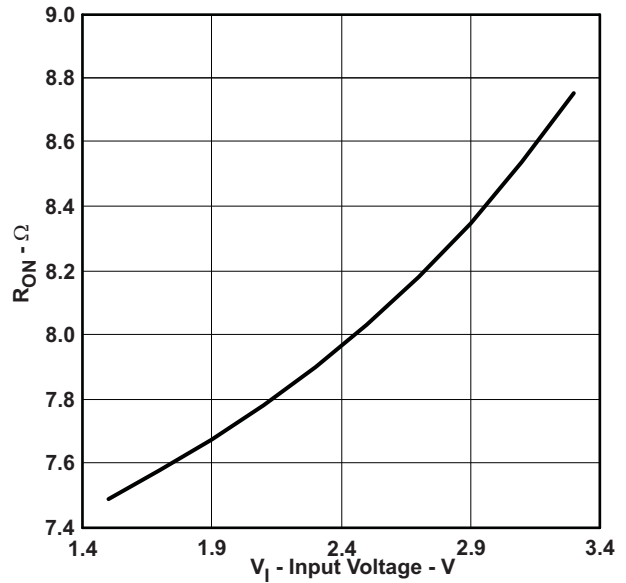
**Figure 3. Gain vs Frequency**



**Figure 4. Off Isolation vs Frequency**



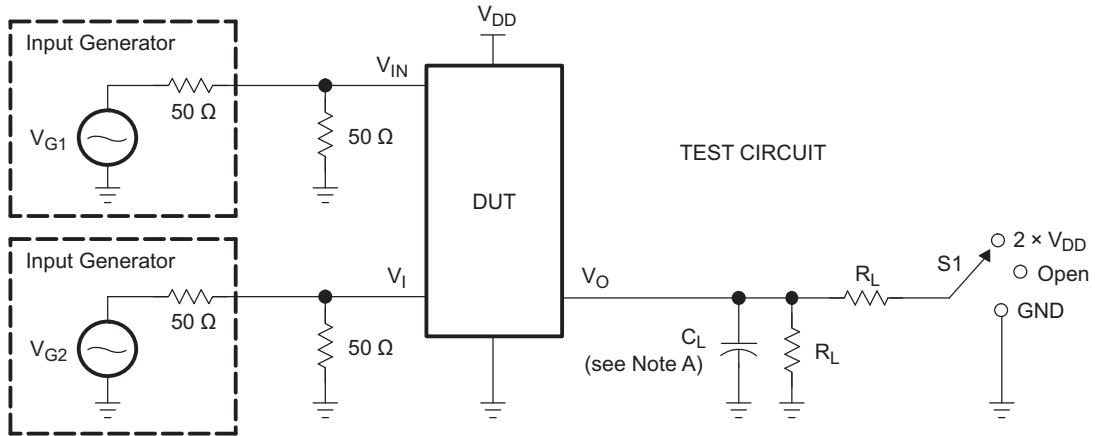
**Figure 5. Crosstalk vs Frequency**



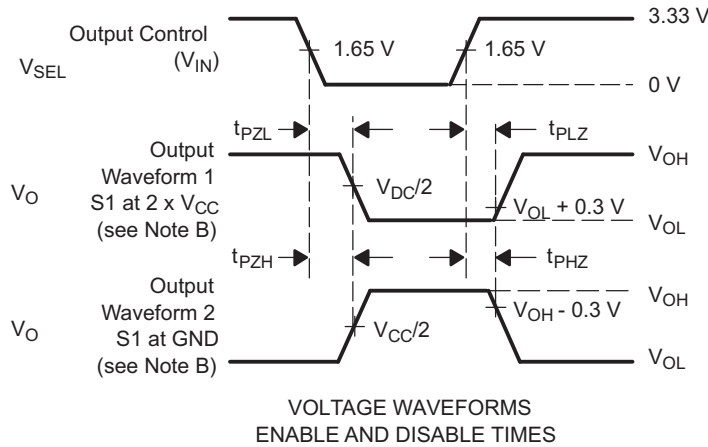
**Figure 6.  $R_{ON}$  vs  $V_{IN}$**

PARAMETER MEASUREMENT INFORMATION

Enable and Disable Times



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>in</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>DD</sub>	200 Ω	GND	4 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>DD</sub>	4 pF	0.3 V

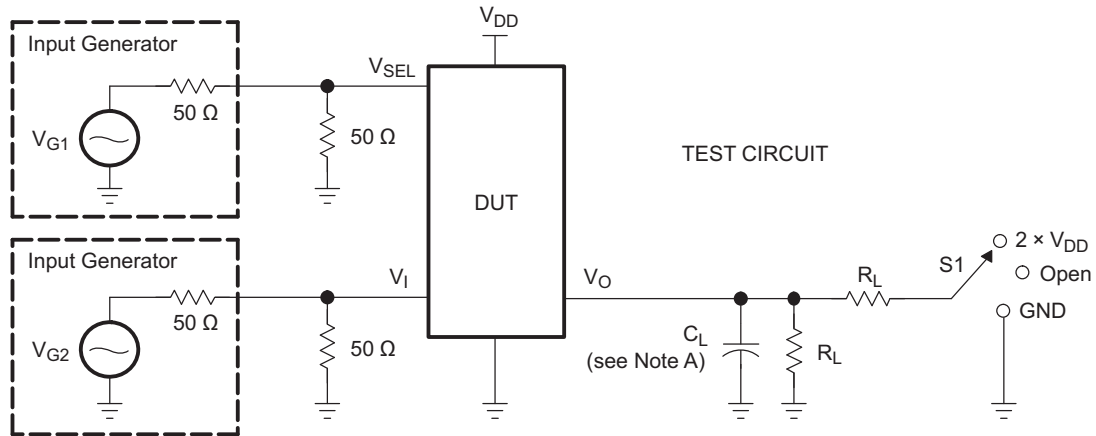


- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

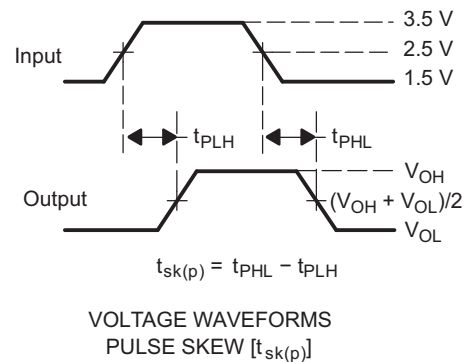
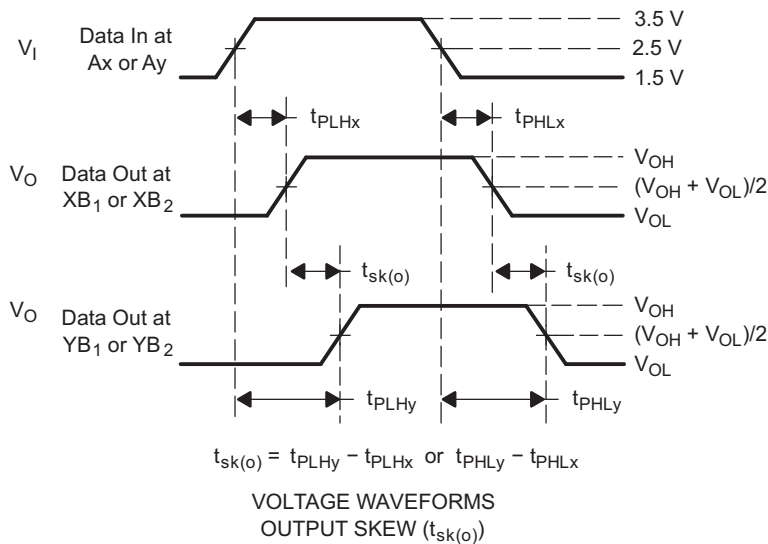
Figure 7. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

Figure 8. Skew



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>in</sub>	C <sub>L</sub>
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND	4 pF
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND	4 pF



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)

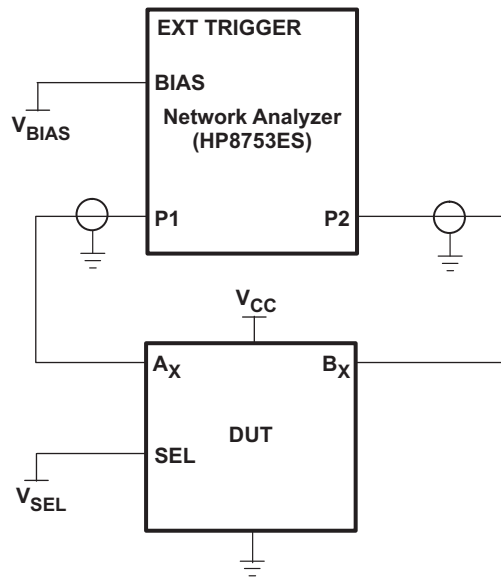
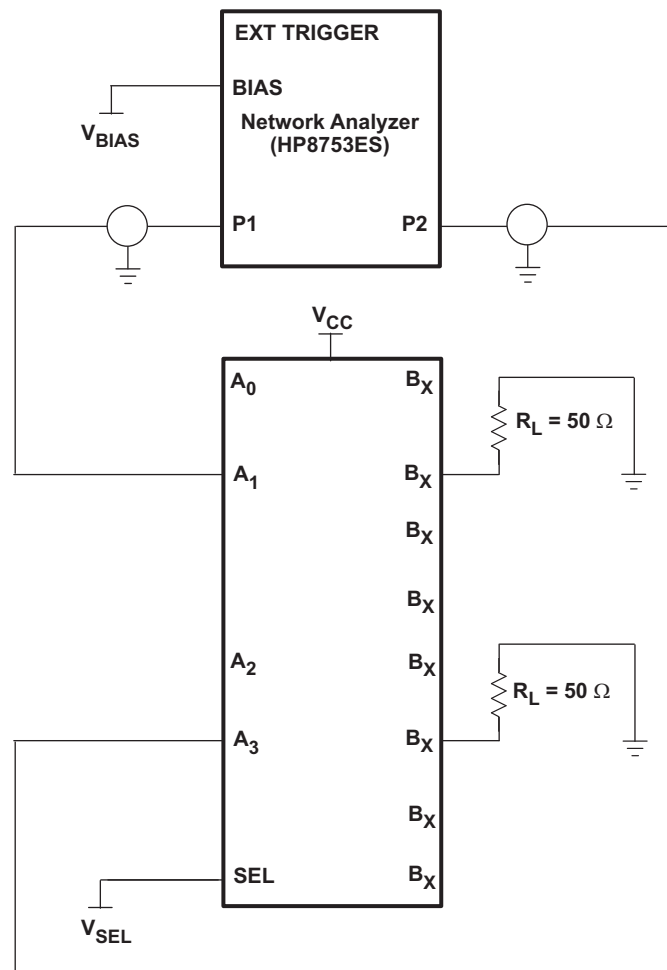


Figure 10. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $B_0$ . All unused analog I/O ports are left open.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

**PARAMETER MEASUREMENT INFORMATION (continued)**


- A.  $C_L$  includes probe and jig capacitance.  
 B. A 50 W termination resistor is needed to match the loading of the network analyzer.

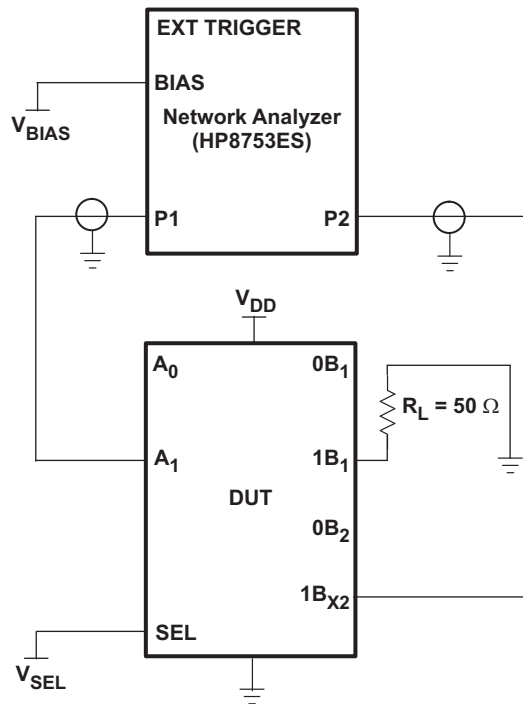
**Figure 11. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL} = 0$  and  $A_1$  is the input, the output is measured at  $A_3$ . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for OFF Isolation ( $O_{IRR}$ )

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = GND$  and  $A_1$  is the input, the output is measured at  $1B_2$ . All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

**HP8753ES Setup**

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35 V$
- ST = 2 s
- P1 = 0 dBm

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**REVISION HISTORY****Changes from Revision A (March 2012) to Revision B****Page**

- 
- 将特性列表中的低 B 低位到位偏斜从 ( 最大值  $t_{sk(o)} = 6ps$  ) 改为 ( 典型值  $t_{sk(o)} = 6ps$  ) ..... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DDR3812RUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SL812	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DDR3812RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DDR3812RUAR	WQFN	RUA	42	3000	358.0	335.0	35.0

## GENERIC PACKAGE VIEW

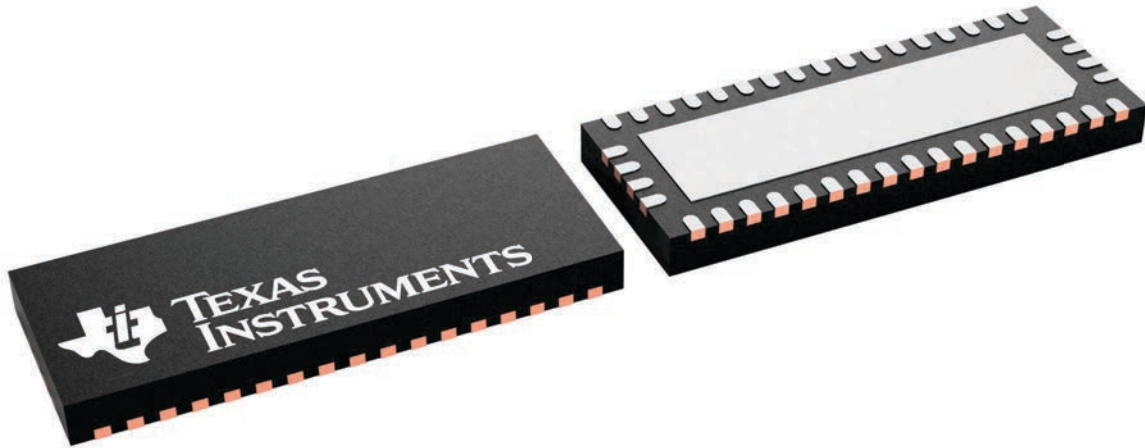
**RUA 42**

**WQFN - 0.8 mm max height**

9 x 3.5, 0.5 mm pitch

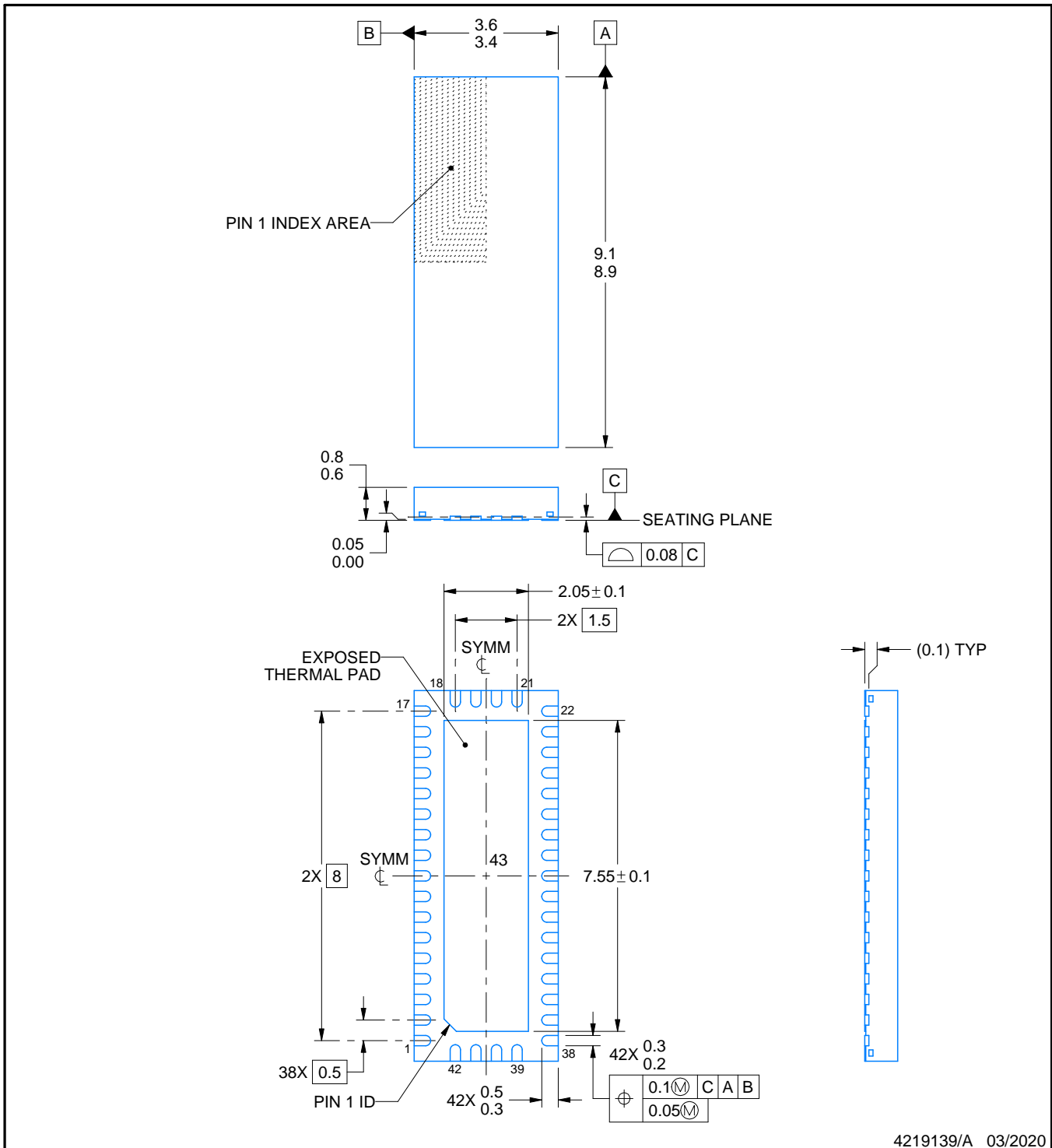
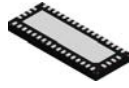
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226504/A





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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

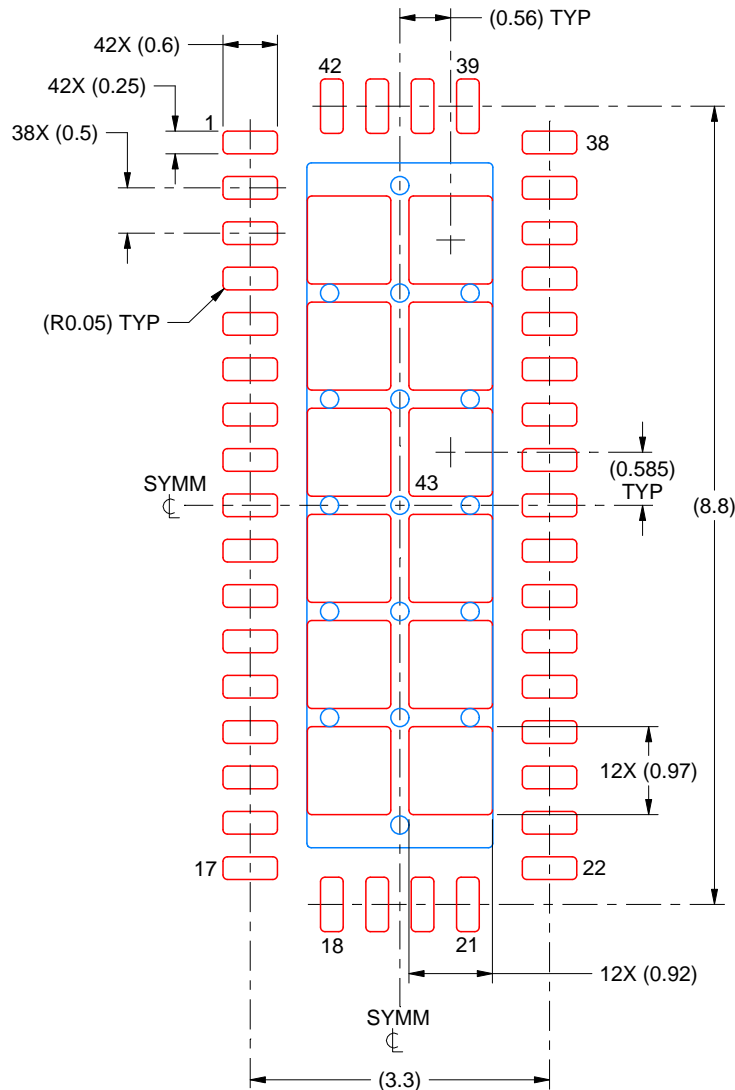


# EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 12X

EXPOSED PAD 43  
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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