TS3DV642-Q1 6Gbps 12 通道差分 1:2 和 2:1 多路复用器

1 特性

- 符合汽车级 Q100 标准
- -40°C 至 105°C 的温度范围（2 级）
- 支持 6 个差分或 12 个单端信号或其他差分/单端组合
- 支持 HDMI 1.4b/2.0、DisplayPort 1.4 HBR2、DP++、Mipi DPHY/CPHY DSI/CSI-2、LVDS
- 双向模拟多路复用器 - 处理 0 至 5.5V 和 DC 至 6Gbps 范围内的大多数电气信号
- 5.8 GHz 的 -3dB 差分带宽
- 出色的动态特性
  - 插入损耗：3.0 GHz 时为 -1.6dB
  - 回波损耗：3.0 GHz 时为 -17dB
- 支持 1.8V、3.3V 或 5.0V 控制逻辑
- 单电源电压：3.3V
- 低有功功率 (45 µA) 和待机功耗 (6 µA)
- I_{OFF} 保护，可在电源轨崩溃时防止电流泄漏 (V_{CC} = 0V)
- 3kV HBM 和 1kV CDM 的 ESD 性能
- 42 引脚、3.5mm x 9mm、0.5mm 间距 WQFN 封装，具有可湿侧面

2 应用

- 高级驾驶辅助系统 (ADAS)
- 汽车信息娱乐系统与仪表组
- 后座娱乐系统
- 汽车音响主机
- 航天与国防

3 说明

TS3DV642-Q1 是一款采用多路复用器/多路信号分离器配置的模拟高速双向无源开关，适用于许多高速差分接口，其数据速率高达 6Gbps。它适用于许多应用，包括 HDMI 1.4/2.0、DisplayPort 1.4 和 Mipi DPHY/CPHY DSI/CSI-2。TS3DV642-Q1 支持差分和单端信号传输 - 基本能够与大多数标准和非标准接口兼容。TS3DV642-Q1 的动态特性允许进行高速开关，使信号眼图具有最小的衰减，并且几乎不会增加抖动。该器件的芯片设计经过优化，可在较高信号频谱上实现出色的频率响应。该器件支持共模电压范围 (CMV) 为 0V 至 3.6V 的差分信令。该器件还支持 0V 至 5.5V 单端 CMOS 信号。

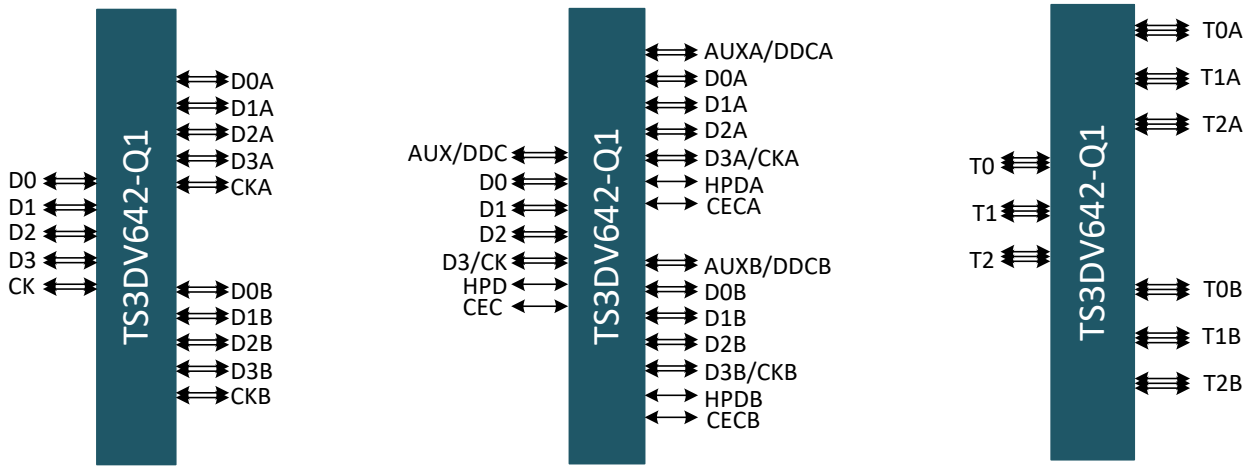
TS3DV642-Q1 消耗超低的有功功率，仅为 45 µA。该器件还具有断电模式，该模式下所有通道均具有高阻抗，并且功耗超低。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3DV642-Q1	WQFN (42)	3.50 mm x 9.00 mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化的用例



Mipi DPHY CSI-2/DSI　　DisplayPort/HDMI　　Mipi CPHY CSI-2

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2020) to Revision A (May 2021)	Page
• 将器件状态更新为“量产数据”	1

5 Pin Configuration and Functions

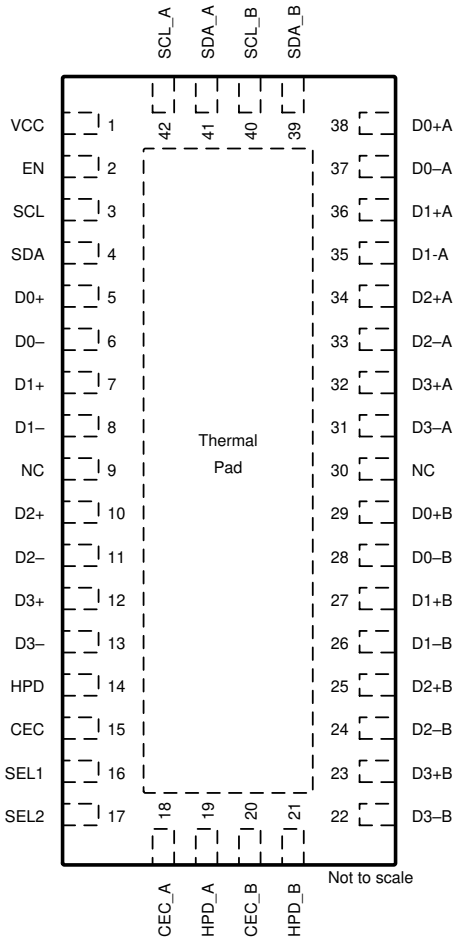


图 5-1. 42 Pin WQFN RUA Package with exposed thermal pad - top view - not to scale

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VCC	1	Power	Supply Voltage
SEL1	16	I	Select Input 1
SEL2	17	I	Select Input 2
EN	2	I	Device Enable
D0+A	38	I/O	Port A, Channel 0, +ve signal
D0 – A	37	I/O	Port A, Channel 0, – ve signal
D1+A	36	I/O	Port A, Channel 1, +ve signal
D1-A	35	I/O	Port A, Channel 1, – ve signal
D2+A	34	I/O	Port A, Channel 2, +ve signal
D2 – A	33	I/O	Port A, Channel 2, – ve signal
D3+A	32	I/O	Port A, Channel 3, +ve signal
D3 – A	31	I/O	Port A, Channel 3, – ve signal
SCL_A	42	I/O	Port A, DDC Clock
SDA_A	41	I/O	Port A, DDC Data
HPD_A	19	I/O	Port A, Hot Plug Detects

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CEC_A	18	I/O	Port A, Consumer Electronics Control
D0+B	29	I/O	Port B, Channel 0, +ve signal
D0 – B	28	I/O	Port B, Channel 0, – ve signal
D1+B	27	I/O	Port B, Channel 1, +ve signal
D1 – B	26	I/O	Port B, Channel 1, – ve signal
D2+B	25	I/O	Port B, Channel 2, +ve signal
D2 – B	24	I/O	Port B, Channel 2, – ve signal
D3+B	23	I/O	Port B, Channel 3, +ve signal
D3 – B	22	I/O	Port B, Channel 3, – ve signal
SCL_B	40	I/O	Port B, DDC Clock
SDA_B	39	I/O	Port B, DDC Data
HPD_B	21	I/O	Port B, Hot Plug Detects
CEC_B	20	I/O	Port B, Consumer Electronics Control
D0+	5	I/O	Common Port, Channel 0, +ve signal
D0 –	6	I/O	Common Port, Channel 0, – ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal
D1 –	8	I/O	Common Port, Channel 1, – ve signal
D2+	10	I/O	Common Port, Channel 2, +ve signal
D2 –	11	I/O	Common Port, Channel 2, – ve signal
D3+	12	I/O	Common Port, Channel 3, +ve signal
D3 –	13	I/O	Common Port, Channel 3, – ve signal
SCL	3	I/O	Common Port, DDC Clock
SDA	4	I/O	Common Port, DDC Data
HPD	14	I/O	Common Port, Hot Plug Detects
CEC	15	I/O	Common Port, Consumer Electronics Control
NC	9, 30	NC	No Connect
GND	PowerPad	GND	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage range		– 0.5	5.5	V
$V_{I/O-ABSMAX}$	Analog voltage range(2) (3) (4)	All I/O (data pins)	– 0.5	5.5	V
$V_{IN-ABSMAX}$	Digital input voltage range(2) (3)	SEL1, SEL2, EN	– 0.5	5.5	V
T_{jmax}	Maximum junction temperature		– 40	125	°C
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, (1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	Supply voltage	3.0	3.6	V
$V_{I/O,CM}$	Input/Output common mode voltage (data pins)	0	3.6	V
$V_{I/O}$	Input/Output voltage (data pins)	0	5.5	V
V_{IN}	Digital input voltage (control pins)	0	5.5	V
DR	Data rate for differential signals		6.0	Gbps
T_A	Operating ambient temperature	– 40	105	°C
T_J	Operating junction temperature	– 40	110	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the *TI application report,Implications of Slow or Floating CMOS Inputs,* literature numberSCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		TS3DV642-Q1 RUA 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and ICPackage Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
DC Characteristics							
R_{ON}	ON-state resistance	All data pins	$V_{I/O}$ = 0 V, $I_{I/O}$ = – 10 mA		6.5	12	Ω
$R_{ON,FLAT}$ (3)	ON-state resistance flatness	All data pins	R_{ON} at $V_{I/O}$ = 1.5 V minus R_{ON} at $V_{I/O}$ = 0 V, $I_{I/O}$ = – 10 mA			0.6	Ω
			R_{ON} at $V_{I/O}$ = 3.6 V minus R_{ON} at $V_{I/O}$ = 0 V, $I_{I/O}$ = – 10 mA			2.0	Ω
I_{OFF}	Leakage under power off (failsafe current)	All data and control pins	VCC = 0 V, $V_{I/O}$ or V_{IN} = 0 V to 5.5 V			±20	μA
Control Inputs (SEL1, SEL2, EN)							
V_{IH}	High-level input voltage for control pins	SEL1, SEL2, EN		1.4			V
V_{IL}	Low-level input voltage for control pins	SEL1, SEL2, EN				0.5	V
I_{IH}	Input high leakage current for control pins	SEL1, SEL2, EN	VCC = 3.6 V, V_{IN} = 5.5 V			±10	μA
I_{IL}	Input low leakage current for control pins	SEL1, SEL2, EN	VCC = 3.6 V, V_{IN} = GND			±10	μA
Power Supply							
I_{CC}	VCC supply current in active mode		EN = H		45		μA
I_{CC_PD}	VCC supply current in power-down mode		EN = L		6		μA

(1) V_I, V_O,I_I, and I_O refer to data I/O pins,V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $R_{ON,FLAT}$ is the difference of R_{ON} in a given channel at specified voltages.

6.6 High-Speed Performances

Over recommended operation free-air temperature range, V_{DD} =3.3V ± 0.3V (unless otherwise noted). For all data pins. R_L = 50 Ω where applicable.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
BW	Differential Bandwidth	– 3 dB from DC		5.8		GHz
IL	Differential insertion loss	DC		– 0.5		dB
		1.7 GHz		– 1.0		dB
		2.7 GHz		– 1.4		dB
		3.0 GHz		-1.6		dB
RL	Differential return loss	DC		– 24		dB
		1.7 Ghz		– 21		dB
		2.7Ghz		– 19		dB
		3.0 Ghz		– 17		dB
Xtalk	Differential crosstalk	DC		-72		dB
		1.7 GHz		– 35		dB
		2.7 GHz		– 30		dB
		3.0 GHz		– 27	-	dB
OISO	Differential off isolation	DC		– 82		dB
		1.7 GHz		– 20		dB
		2.7 GHz		– 16		dB
		3.0 GHz		– 16		dB

(1) All Typical Values are at V_{DD} = 3.3 V(unless otherwise noted), T_A = 25°C.

6.7 Switching Characteristics

over recommended operation free-air temperature range, V_{DD} =3.3 V± 0.3 V (unless otherwise noted). For all data pins.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation Delay	All I/O			66		ps
$t_{SK,INTER}$	Inter-pair Skew	D0-3	The maximum difference in differential prop delay between data channels; 1.7 GHz; at nominal corner		10		ps
$t_{SK,INTRA}$	Intra-pair Skew	D0-3	The maximum difference in prop delay between +ve and – ve signals of each channel (for all channels); at 1.7 GHz; at nominal corner		8		ps
t_{ON} (2)	Switch turn-on time	All I/O	When EN goes from L to H			5	µs
t_{SWITCH} (3)	Switching time between channels	All I/O	When SEL pins toggles			5	µs

(1) All typical values are at V_{DD} = 3.3 V(unless otherwise noted), T_A = 25°C.
(2) t_{ON} is the time it takes the output to recover within 95% of final value after enabling switches
(3) t_{SWITCH} is the time it takes for theoutput to recover within 95% of final value after the state is changed

6.8 Typical Characteristics

图 6-1, 图 6-2, 图 6-3 and 图 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

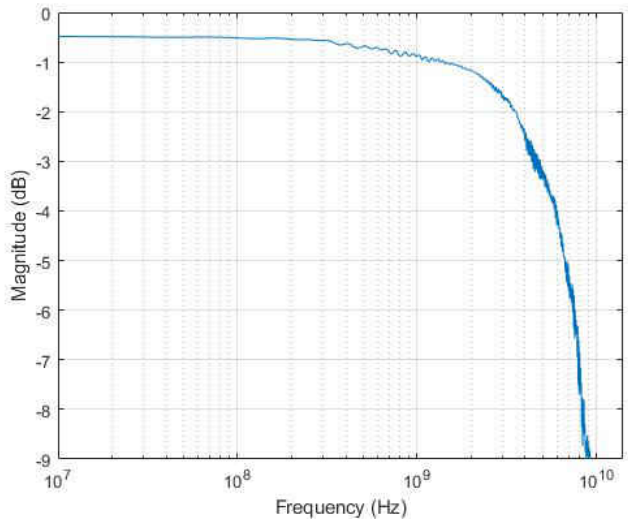


图 6-1. Typical differential gain vs frequency

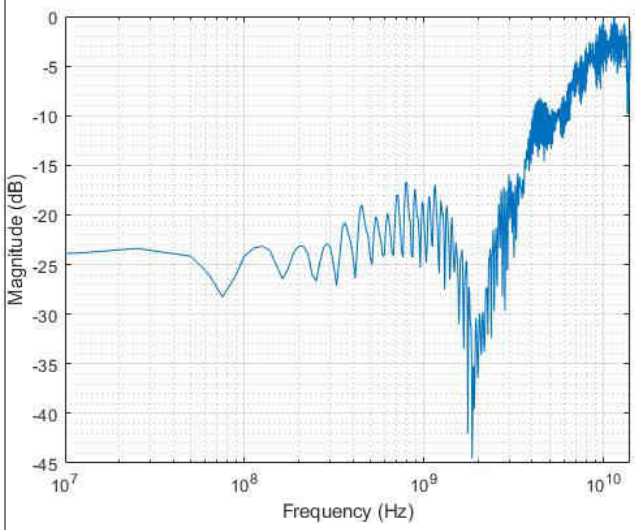


图 6-2. Typical return loss vs frequency

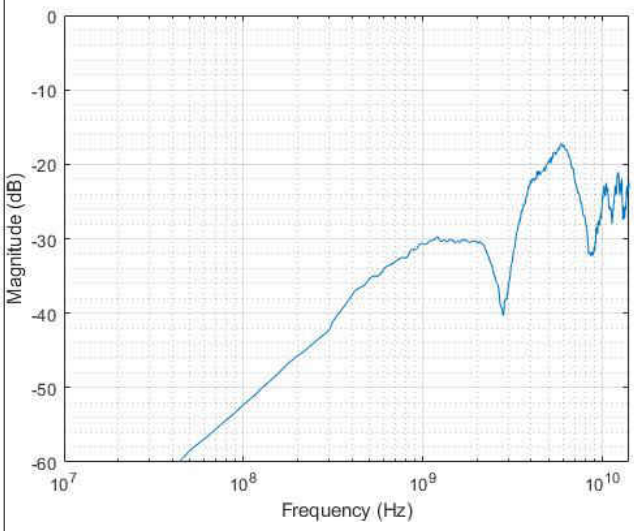


图 6-3. Typical differential cross-talk vs frequency

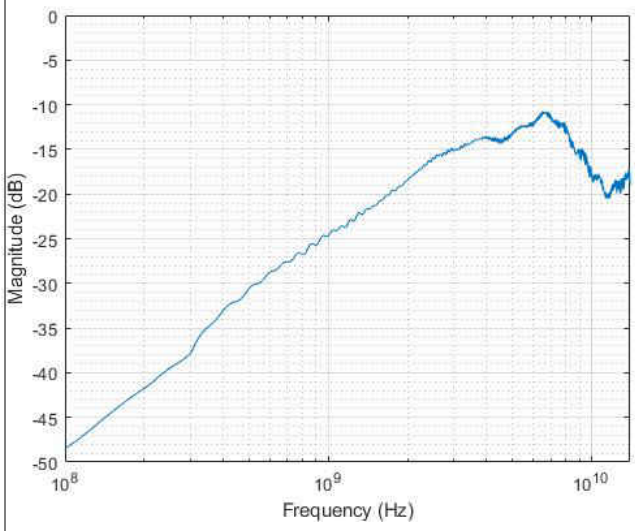


图 6-4. Typical differential off-isolation vs frequency

6.8 Typical Characteristics

图 6-1, 图 6-2, 图 6-3 and 图 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

图 6-5. Typical eye diagrams at 3.4 Gbps. Top: baseline calibration setup. Middle: through TS3DV642-Q1 Port A. Bottom: through TS3DV642-Q1 Port B.

6.8 Typical Characteristics

图 6-1, 图 6-2, 图 6-3 and 图 6-4 show typical high speed performance plots for TS3DV642-Q1 in TI evaluation board with measurement parasitics calibrated out.

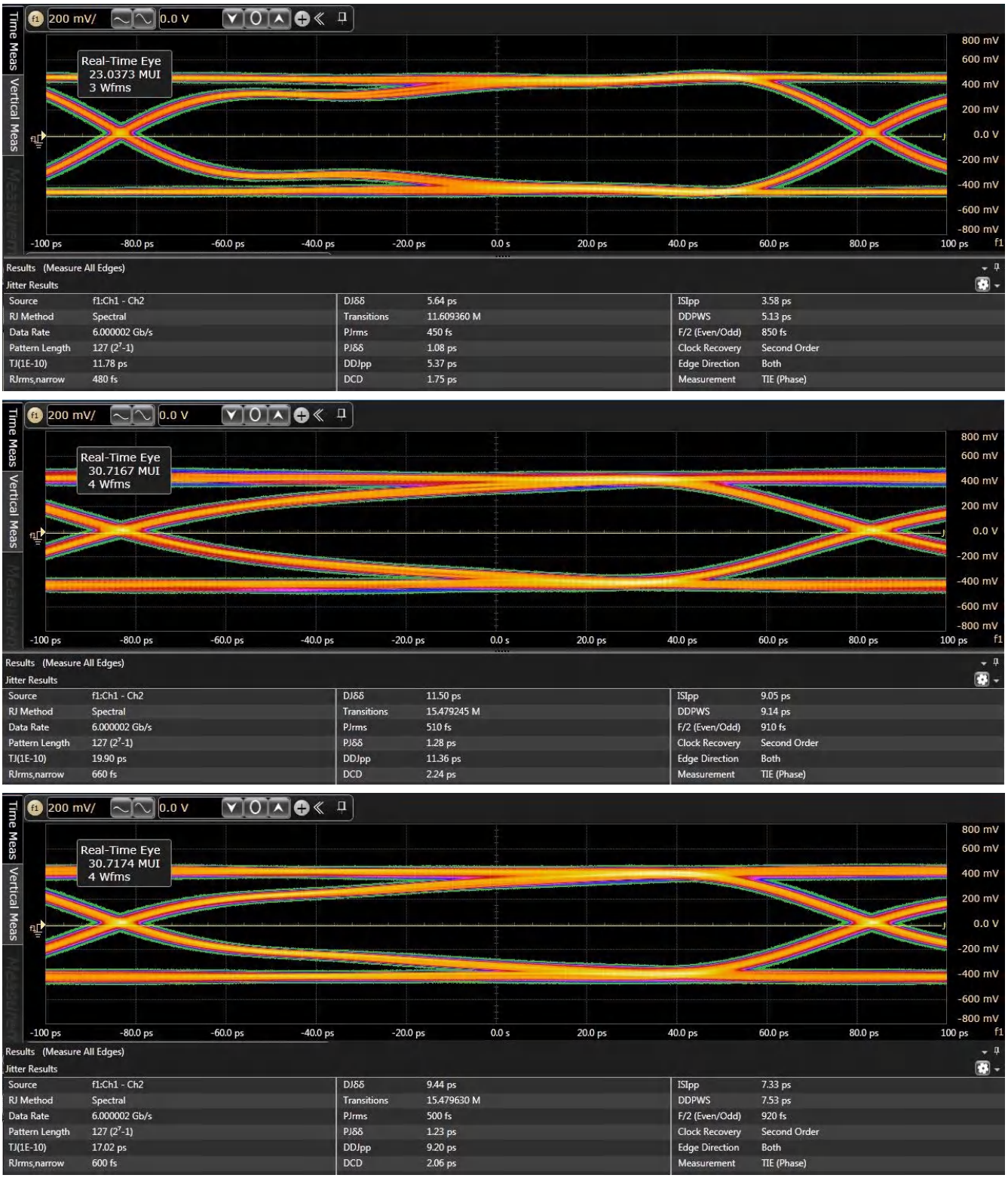


图 6-6. Typical eye diagrams at 6.0 Gbps. Top: baseline calibration setup. Middle: through TS3DV642-Q1 Port A. Bottom: through TS3DV642-Q1 Port B.

7 Parameter Measurement Information

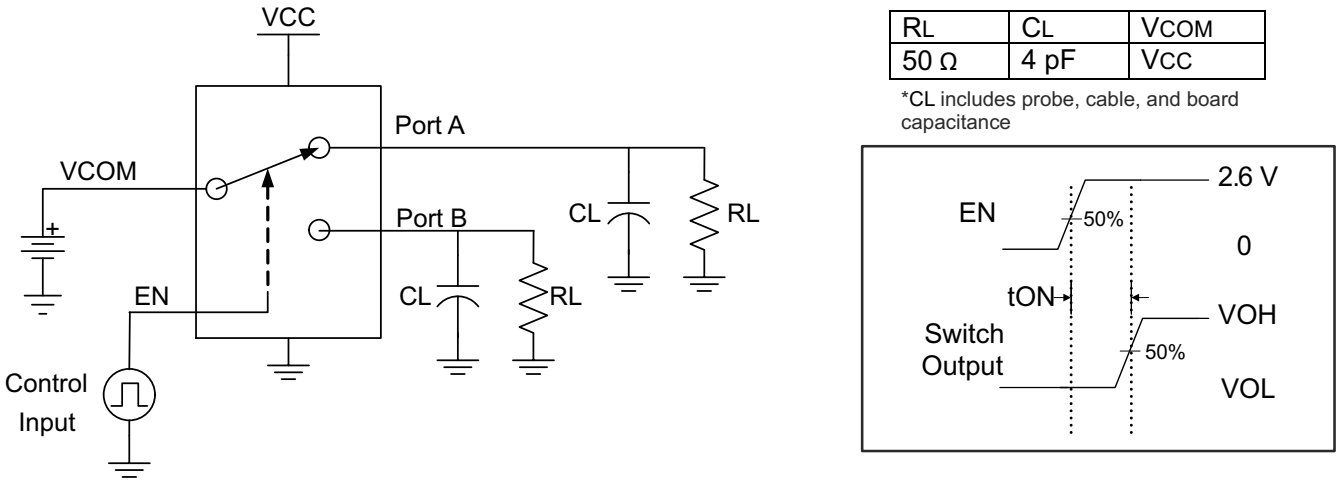


图 7-1. Switch Turn-On Time (t_{ON})

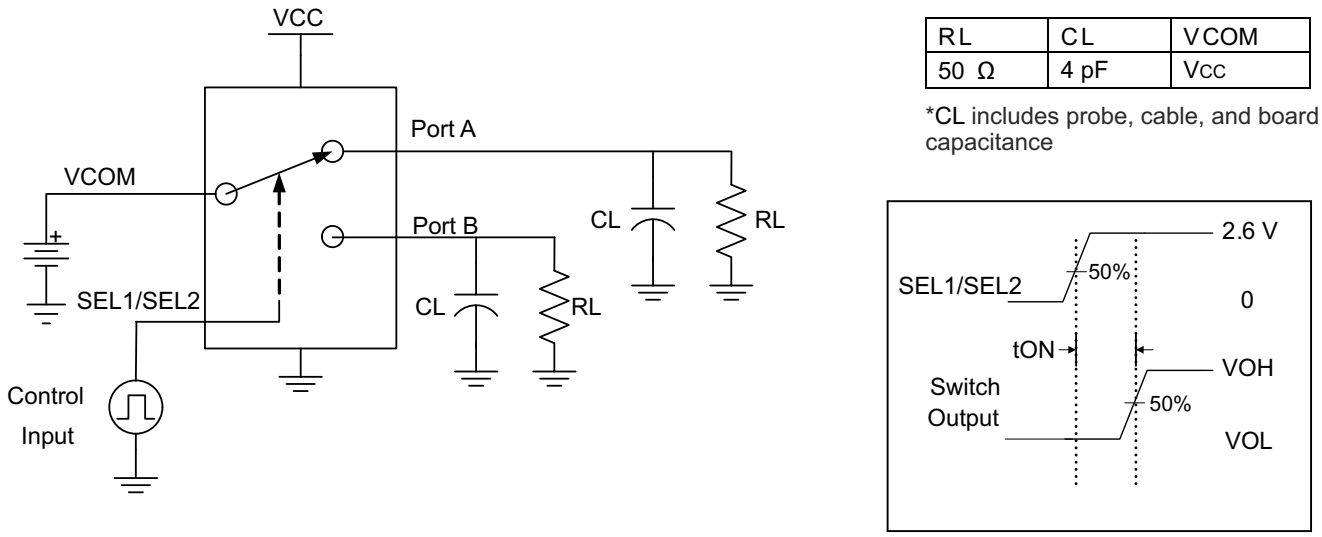
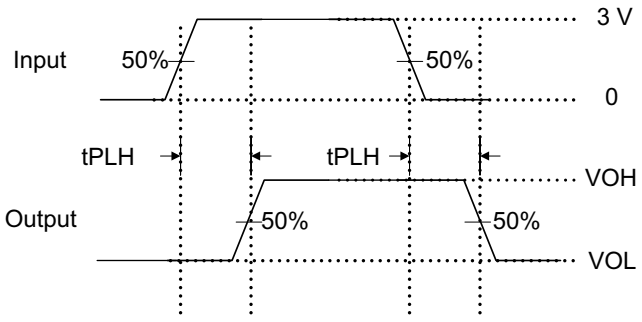
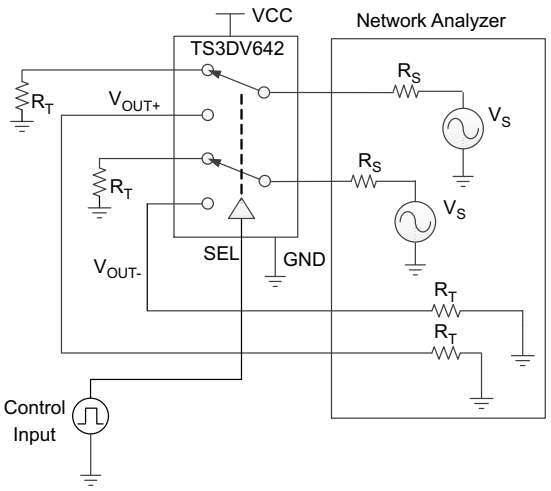


图 7-2. Switching Time Between Channels (t_{SWITCH})



$$tpd = (tPLH + tPLH) / 2$$

图 7-3. Propagation Delay (t_{pd})

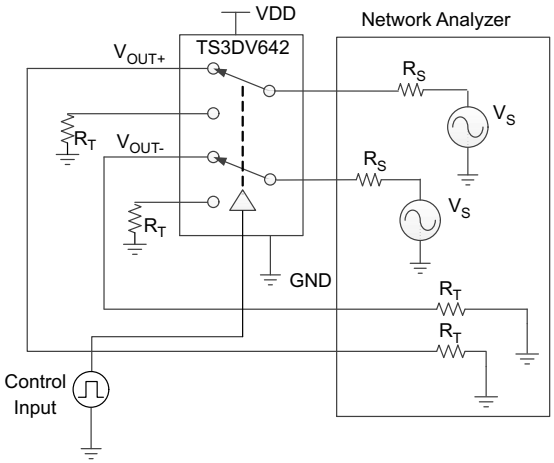


Channel OFF

SEL = H or L
$R_S = R_T = 50\Omega$

V_S = -10dBm (200mV at 50Ω Load)
V_{DC_BIAS} = 1 V

图 7-4. Differential Off-Isolation and Xtalk



Channel ON

SEL = H or L
$R_S = R_T = 50\Omega$

V_S = -10dBm (200mV at 50Ω Load)
V_{DC_BIAS} = 1 V

图 7-5. Differential Bandwidth (BW)

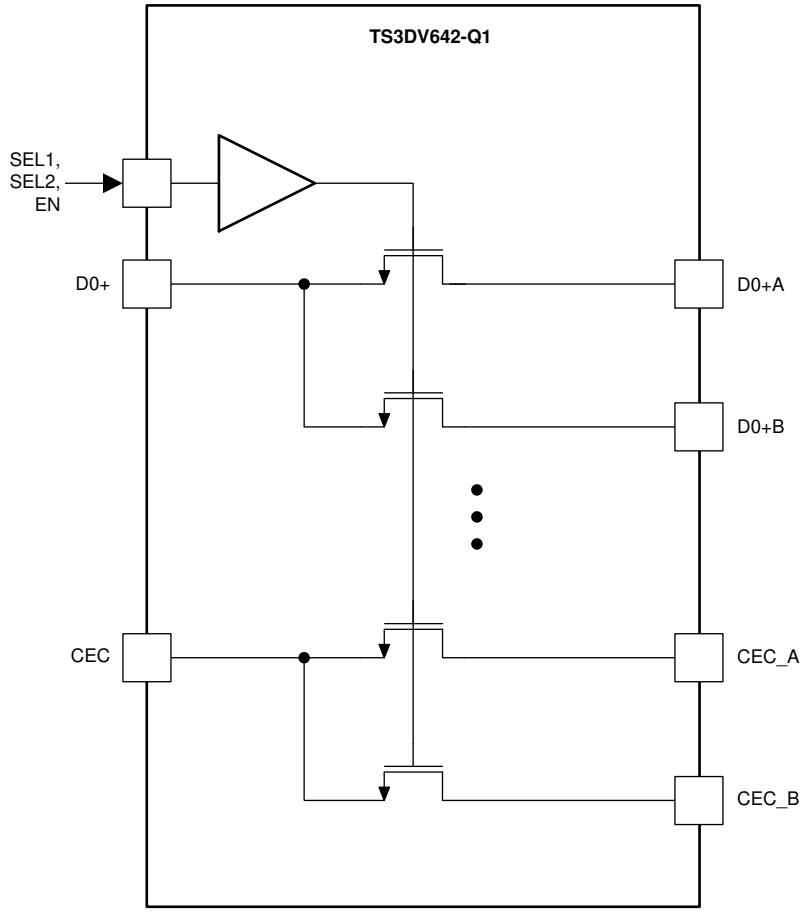
8 Detailed Description

8.1 Overview

The TS3DV642-Q1 is a 6 differential channel or 12 single ended channel bidirectional multiplexer/demultiplexer. It offers low on-state resistance as well as low datapath parasitics which allows it to achieve a high bandwidth. The TS3DV642-Q1 is a passive mux that is recommended for data rates up to 6 Gbps, however the device can be used for interfaces with higher data rates depending on how much loss is permissible for the mux from the overall electrical link budget. The device provides the high bandwidth necessary for many interfaces to handle differential and as well as single ended signals. The device supports differential signaling with common mode voltage range (CMV) of 0 to 3.6 V and 0 - 5.5 V CMOS signals.

The TS3DV642-Q1 has total 6 differential channels. All these channels are functionally equivalent and provides almost identical electrical performance. The channels can be used in an arbitrary fashion for differential and single ended signals in any order.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3DV642-Q1 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. TS3DV642-Q1 has 6 differential channel or 12 single ended channel bidirectional switches with a high bandwidth. TS3DV642-Q1 uses an extremely low power technology and uses only 45 µA I_{CC} in active mode. The device has integrated ESD that can support up to 3-kV Human-Body Model (HBM) and 1-kV Charge Device Model (CDM). TS3DV642-Q1 is offered in a 42-pin QFN package (9 mm x 3.5 mm) with 0.5 mm pitch. The device can support analog I/O signal in 0 to 5.5 V range. TS3DV642-Q1 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature

prevents leakage current in the device. The TS3DV642-Q1 is not designed for passing signals with negative swings.

8.4 Device Functional Modes

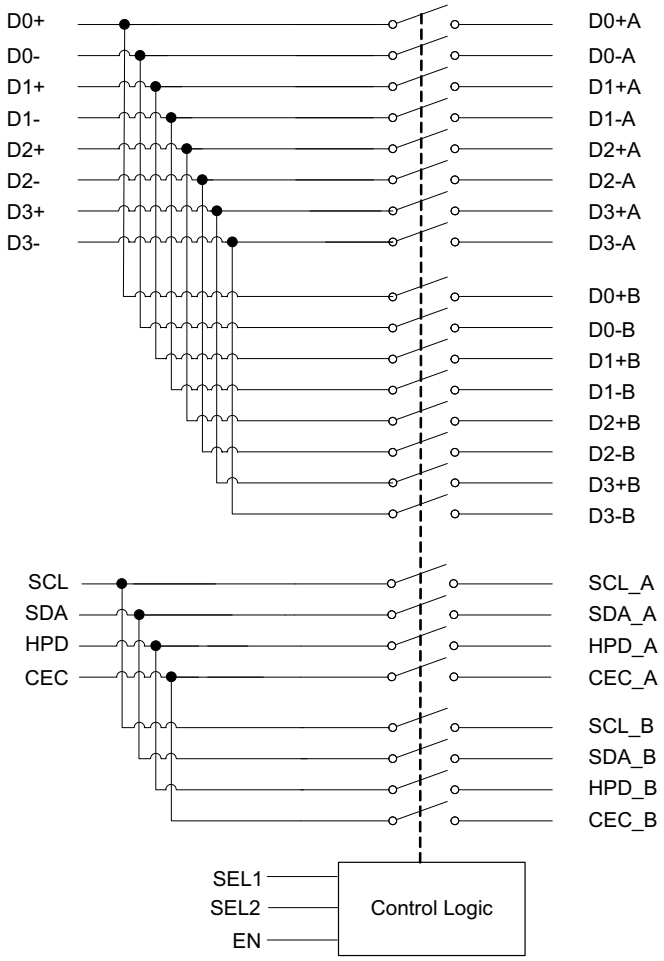


图 8-1. Logic Diagram

表 8-1 lists the device functions for the TS3DV642-Q1 device.

表 8-1. Functional Table

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	Channel D0+/D0 – to D0+A/D0 – A is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	L	H	Channel D0+/D0 – to D0+B/D0 – B is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	H	L	All A channels are enabled. All B channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3DV642-Q1 is an analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 6 Gbps. The device also works for single ended signals. The TS3DV642-Q1 supports differential signaling with common mode voltage range (CMV) of 0 to 3.6 V and with differential amplitude up to 1800 mVpp, and single ended CMOS signaling with swing limited to 0 to 5.5 V. TS3DV642-Q1 can be used as mux or demux switch for:

- HDMI 1.4 and HDMI 2.0 - up to 6 Gbps per channel
- DisplayPort (DP) for RBR, HBR, and HBR-2 data rates - up to 5.4 Gbps per lane
- DP++
- Mipi DPHY interfaces such as DSI and CSI-2 - up to 4.5 Gbps per lane
- Mipi CPHY based CSI-2
- LVDS

6 Channels of the TS3DV642-Q1 are functionally equivalent and can be used in an arbitrary fashion for differential and single ended signals in any order. For example in Mipi DPHY applications any of the 6 differential channels can be used for clock signals. For Mipi CPHY applications the data pins can be grouped any order to form trio signals. For HDMI application, while TS3DV642-Q1 data signal pins are marked for specific HDMI use, the main-link data, main-link clock, DDC, HPD, CEC can be assigned in any order if required.

9.2 Typical Application - Demultiplexing HDMI Signals

The TS3DV642-Q1 can be used to mux HDMI signals. 图 9-1 shows use case where TS3DV642-Q1 switches HDMI signals from a source to either to an external connector or to an SOC. This section provides detailed design implementation for a HDMI application where TS3DV642-Q1 provides 1:2 multiplexing function.

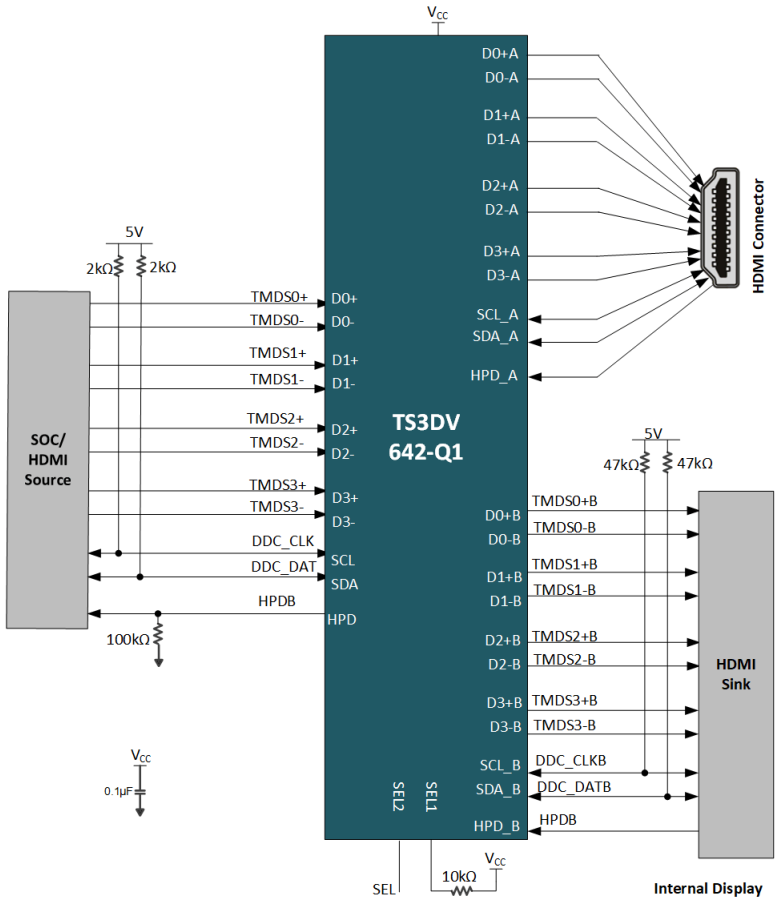


图 9-1. Demultiplexing HDMI signals - schematic

9.2.1 Design Requirements

表 9-1. Design Parameters for HDMI Application

Design parameter	Example value
V_{CC}	3.0 V to 3.6 V
VCC decoupling capacitor	0.1 μF
DDC Pull-up resistors on sink side (only for internal display path)	47 kΩ to 5 V
DDC Pull-up resistors on source side	2 kΩ to 5 V
HPD pull-down resistor on source side	100 kΩ to GND
Pull-up / Pull-down resistors for SEL1 / SEL2 pins	10 kΩ

9.2.2 Detailed Design Procedure

The TS3DV642-Q1 is designed to operate with 3.0 V to 3.6 V power supply. Decoupling capacitors may be used to reduce noise and improve power supply integrity. Pull-up resistors to 5 V must be placed on the sinke side DDC clock and data lines according to the HDMI standard.

9.2.3 Application Curves

An HDMI connector functioning as a source is subject to HDMI source compliance test. This section provides application curves related to HDMI 1.4 and 2.0 source compliance for jitter and eye mask respectively.

图 9-2 shows HDMI 1.4 compliance jitter performance at 3.0 Gbps data rate. For brevity only one of the three data channels and Port A illustrated. Other channels have similar performances. As illustration shows the TS3DV642-Q1 adds minimal jitter to the link - 89 mTbit through mux vs 73 mTbit without mux.

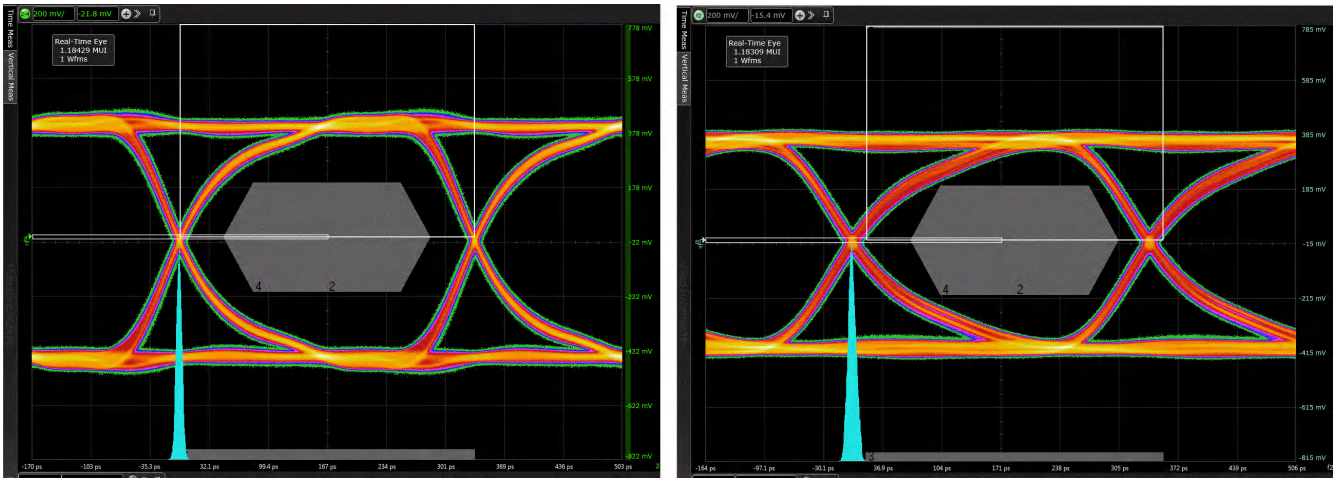


图 9-2. HDMI 1.4 compliance at 3.0 Gbps - jitter performance. Left: with no DUT in the path. Right: TS3DV642-Q1 in the path

图 9-3 shows HDMI 2.0 eye mask performance at 6.0 Gbps data rate. For brevity only one of the three data channels and Port A is illustrated. Eye masks are for worst case positive skew. Other channels, and cases have similar performances.

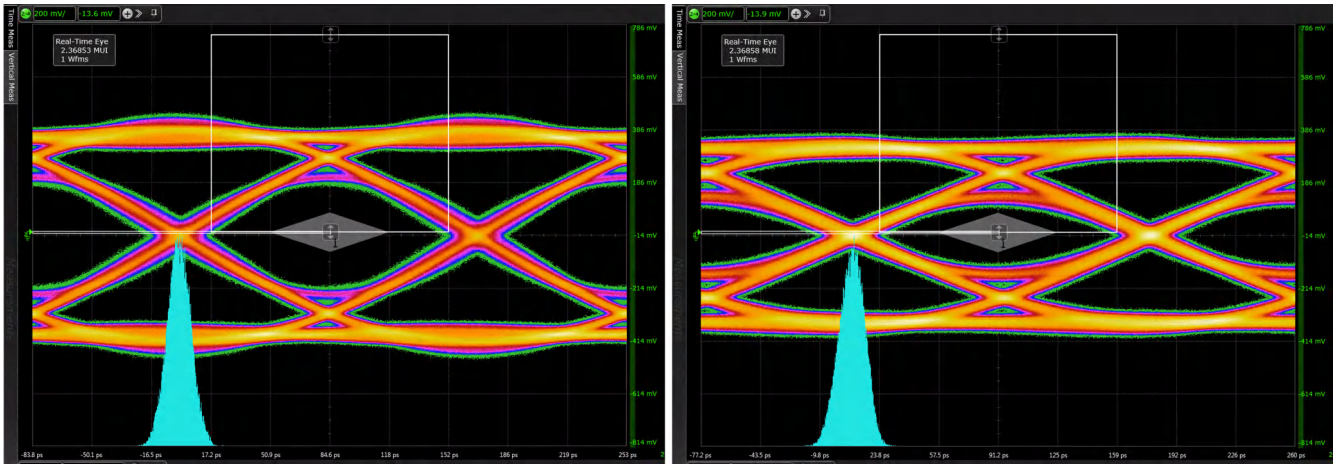


图 9-3. HDMI 2.0 compliance at 6.0 Gbps - eye mask at TP2_EQ. Left - with no DUT in the path. Right - TS3DV642-Q1 in the path

9.3 Typical Application - Multiplexing HDMI Signals

图 9-4 shows a 2:1 multiplexing use case where TS3DV642-Q1 is being used to choose HDMI signals from either an external HDMI connector or an internal HDMI source to connect to a HDMI sink device. Note HDMI connector in this use case represents a Sink port and is subject to HDMI sink compliance requirements. Part of the compliance requirements the mainlink data and clock signals needs to have 50Ω termination from each pin to 3.3 V supply with certain tolerance depending on data rate. Note the TS3DV642-Q1 adds a series resistance (R_{ON}) to the mainlink sink termination. To account for the additional series resistance it is recommended that sink internal termination resistance is reduce by equal amount. Where such provisioning is not possibble, alternate solution is to install external resistors on board from each pin to VCC as shown in 图 9-4. In applications where a retimer is used behind a HDMI connector in sink application, this series resistance provisioning is not required as retimer termination is tested for HDMI compliance.

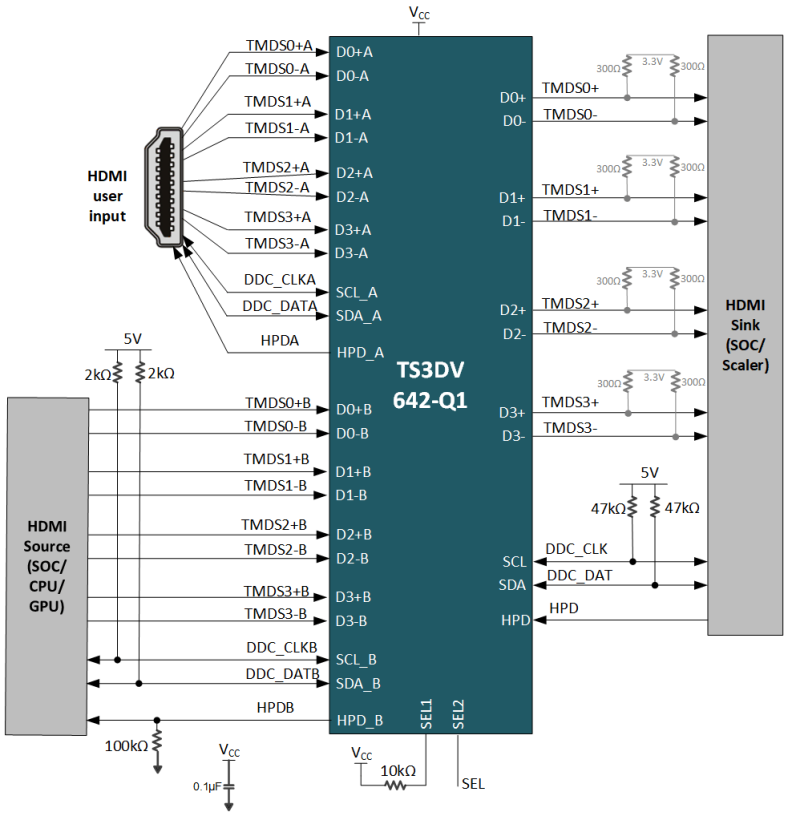


图 9-4. Multiplexing HDMI signals - schematic

9.4 Systems Examples

TS3DV642-Q1 can be used for many high speed interfaces. 图 9-5, 图 9-6, 图 9-7, and 图 9-8 show some system level examples for select few interfaces. Note for brevity exact detail design implementation is not shown.

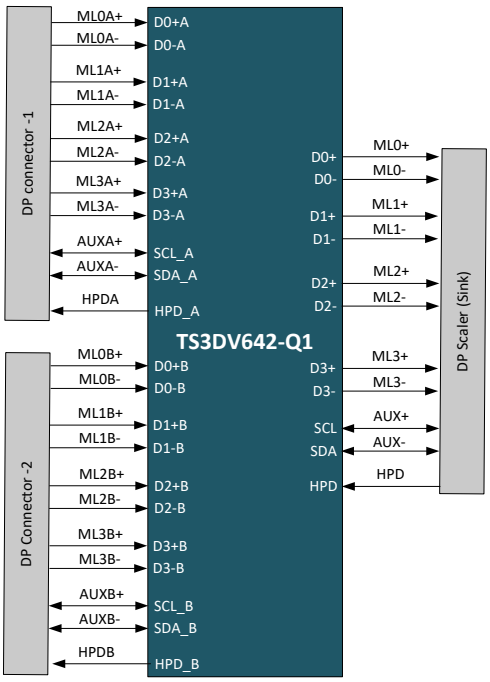


图 9-5. DisplayPort 2:1 switching

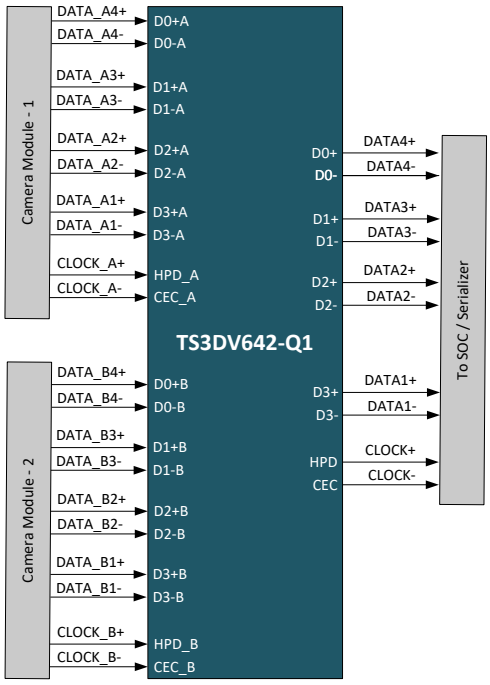


图 9-6. Mipi DPHY based CSI-2 switching

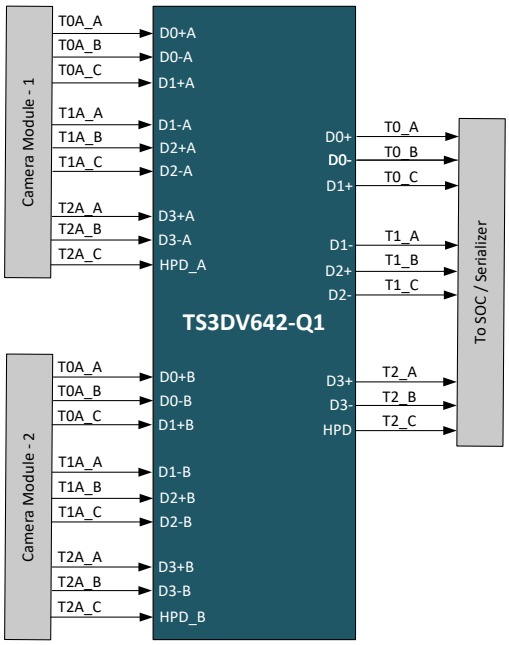


图 9-7. Mipi CPHY based CSI-2 switching

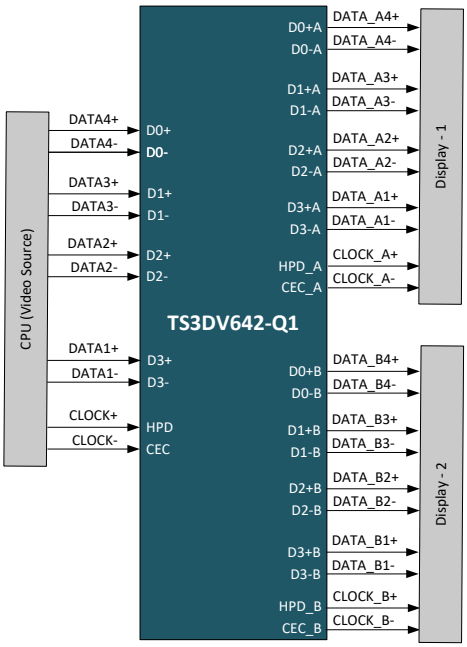


图 9-8. Mipi DPHY based DSI switching

10 Power Supply Recommendations

V_{CC} should be in the range of 3.0 V to 3.6 V. Voltage levels above those listed in the Absolute Ratings table should not be used. Decoupling capacitor(s) such as 0.1 μF may be used to reduce noise and improve power supply integrity. There are no power sequence requirements for the TS3DV642-Q1.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed-circuit board layout guidelines are recommended:

- Decoupling capacitors should be used between power supply pin and ground pin to ensure low impedance to reduce noise To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- ESD and EMI protection devices (if used) should be placed as close as possible to the connector.
- Short trace lengths should be used to avoid excessive loading.
- To minimize the effects of crosstalk on adjacent traces, keep the traces at least two times the trace width apart.
- Separate high-speed signals from low-speed signals and digital from analog signals
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- The high-speed differential signal traces should be routed parallel to each other as much as possible. The traces are recommended to be symmetrical.
- A solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

11.2 Layout Example

TS3DV642-Q1 application with a single controller interfacing with two HDMI connectors.

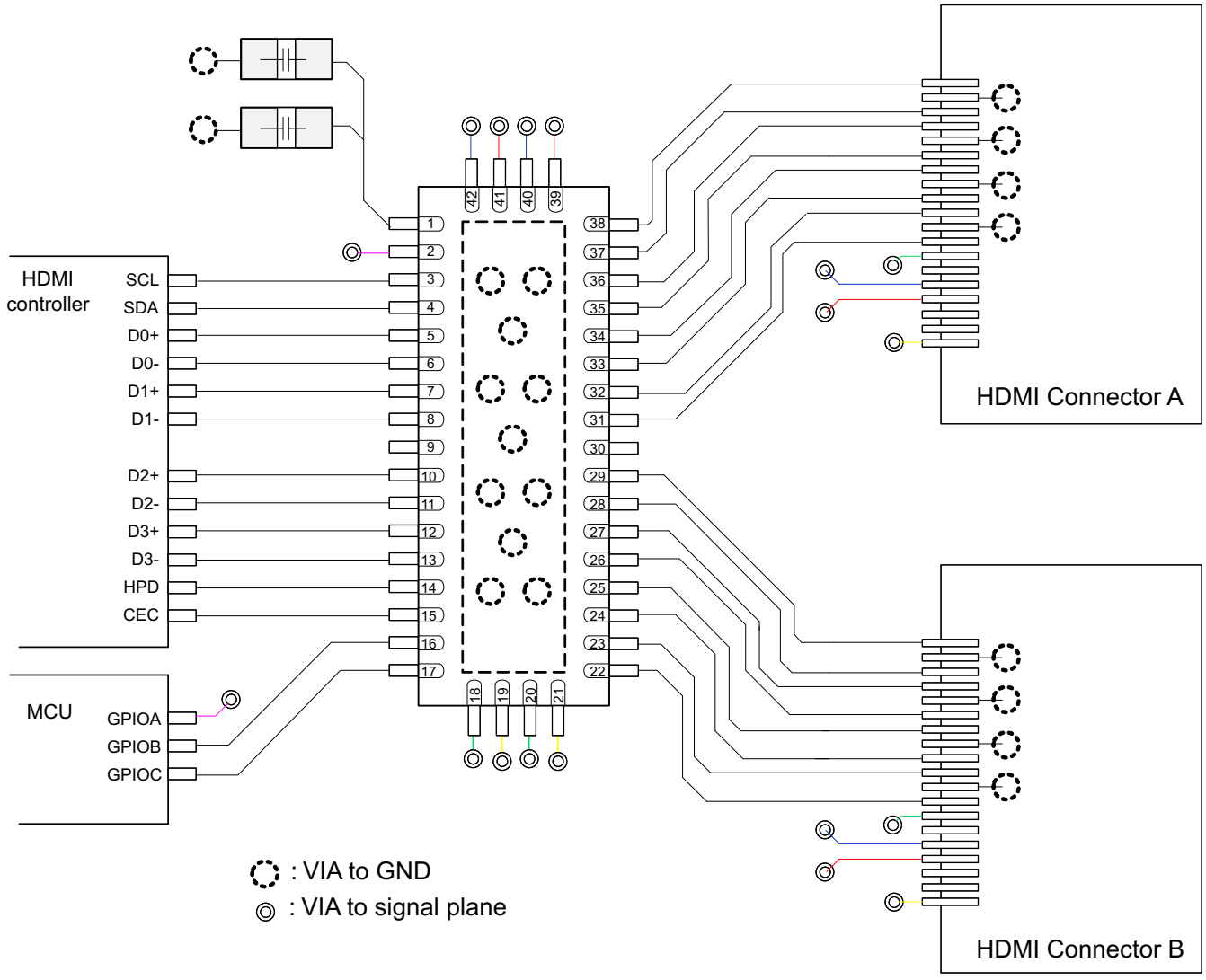


图 11-1. Layout Example

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

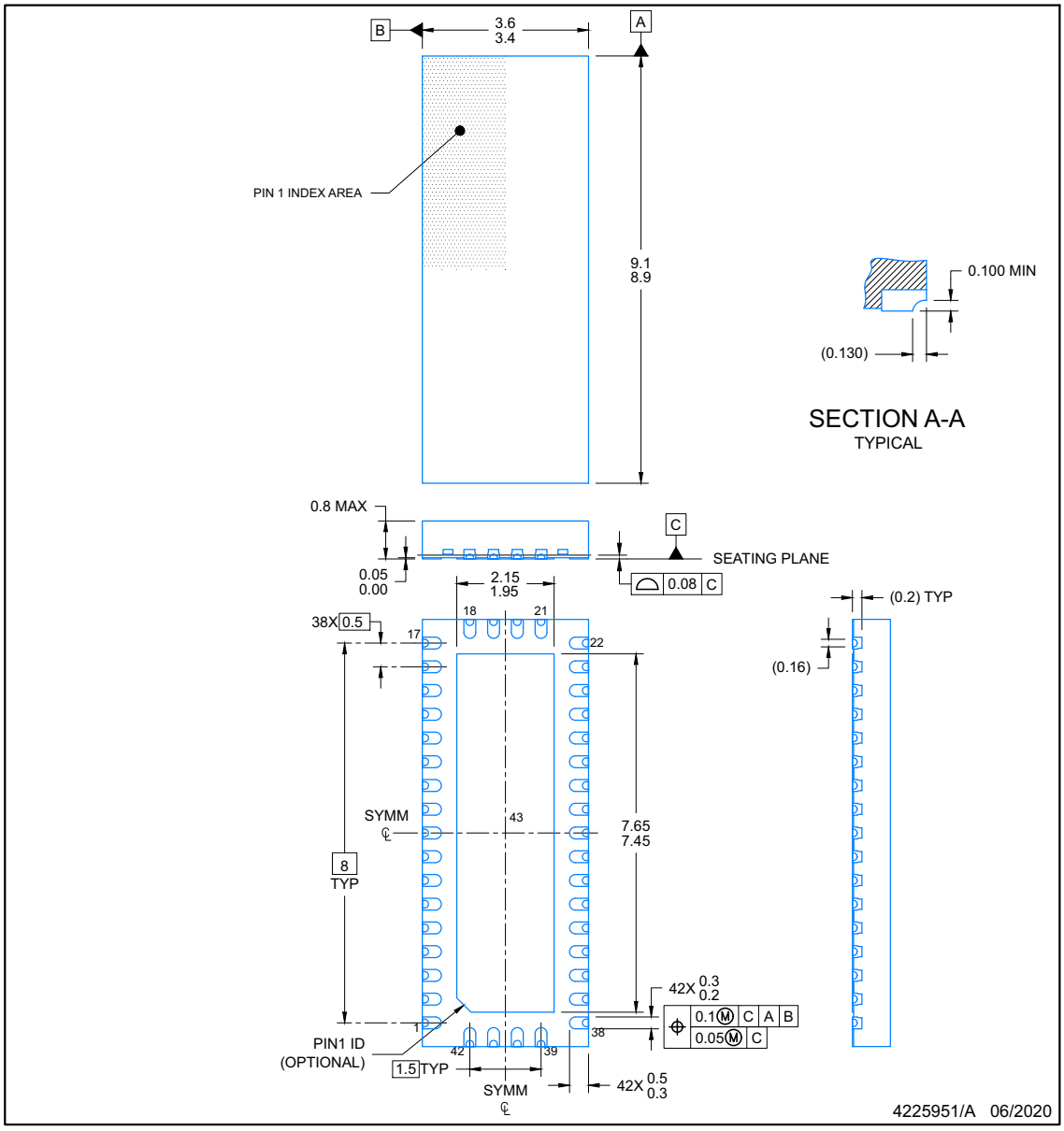
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RUA0042B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

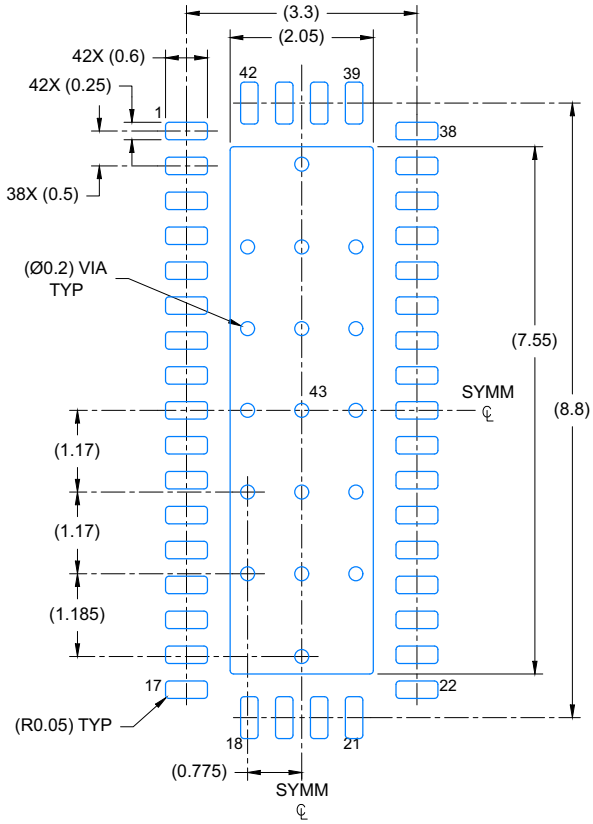
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

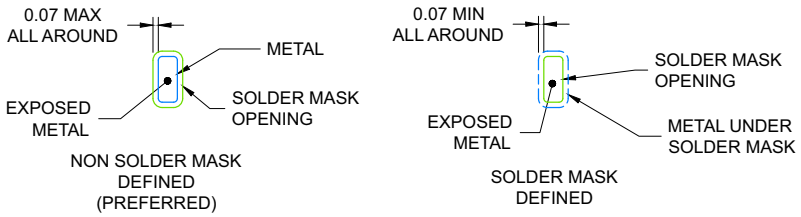
RUA0042B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 11X



SOLDER MASK DETAILS

4225951/A 06/2020

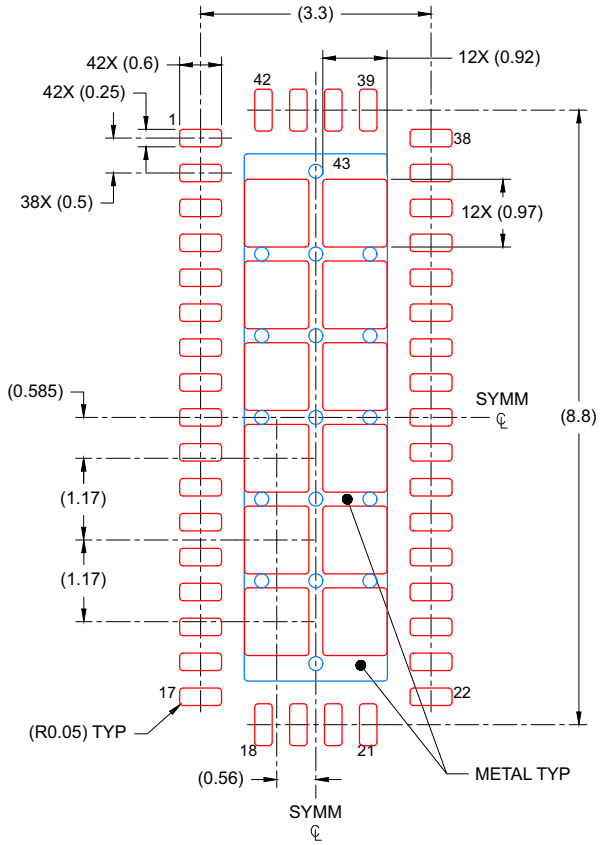
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 11X

4225951/A 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV642RUARQ1	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q	Samples
TS3DV642RUATQ1	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	T3DV642Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS3DV642-Q1 :

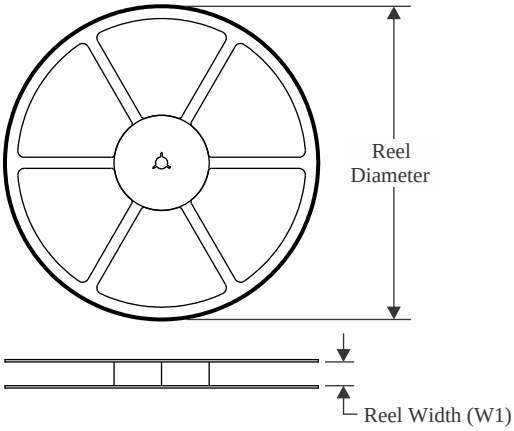
- Catalog : TS3DV642

NOTE: Qualified Version Definitions:

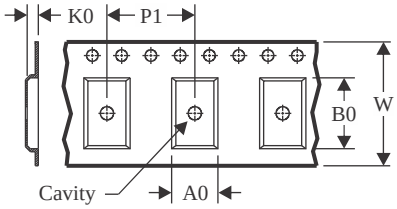
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

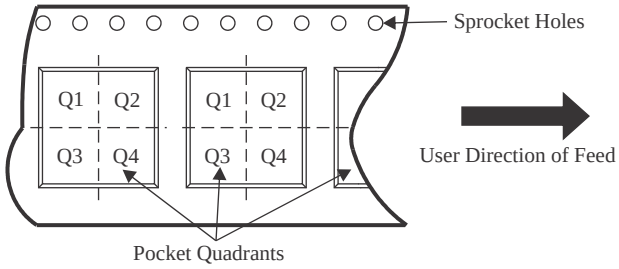


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

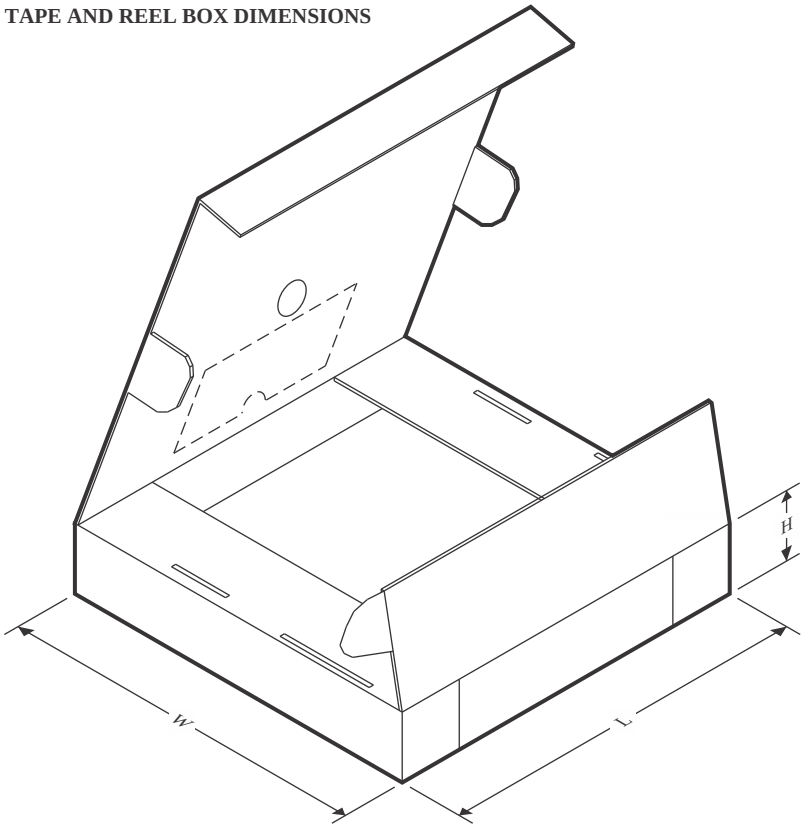
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV642RUARQ1	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3DV642RUATQ1	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV642RUARQ1	WQFN	RUA	42	3000	367.0	367.0	35.0
TS3DV642RUATQ1	WQFN	RUA	42	250	210.0	185.0	35.0

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