TS3USB3000 DPDT USB 2.0 高速和移动高清链路 (MHL) 6.1GHz 开关

1 特性

- V_{CC} 范围为 2.3V 至 4.8V
- 移动高清链接 (MHL) 开关：
  - 带宽 (-3dB)：6.1GHz
  - R_{ON}（典型值）：5.7Ω
  - C_{ON}（典型值）：1.6pF
- USB 开关：
  - 带宽 (-3dB)：6.1GHz
  - R_{ON}（典型值）：4.6Ω
  - C_{ON}（典型值）：1.4pF
- 电流消耗：30μA（典型值）
- 特殊 特性的 xHCI 控制器：
  - I_{OFF} 保护防止在掉电状态（V_{CC} 和 V_{BUS} = 0V）下产生泄漏电流
  - 1.8V 兼容控制输入 (SEL，$\overline{OE}$)
  - 所有 I/O 引脚上的过压容限 (OVT) 高达 5.5V，而且无需使用外部组件
  - 在 D+/- 引脚短接至 9V 电压时提供过压保护
- 静电放电 (ESD) 性能:
  - 3.5kV 人体放电模型（A114B，II 类）
  - 1kV 带电器件模型 (C101)
- 10 引脚超薄四方扁平无引线 (UQFN) 封装（1.5mm×2mm，间距为 0.5mm）

2 应用

- 智能手机、平板电脑、移动设备
- 便携式仪表
- 数码相机

3 说明

TS3USB3000 器件是一款双刀双掷 (DPDT) 多路复用器，在同一封装内包含一个高速移动高清链接 (MHL) 开关和一个 USB 2.0 高速 (480Mbps) 开关。这些配置使得系统设计人员能够为 MHL 视频信号和 USB 数据使用一个普通 USB 或者微型 USB 连接器。

TS3USB3000 的 V_{CC} 范围为 2.3V 至 4.8V，支持过压容限 (OVT) 功能，允许 I/O 引脚承受过压条件（最高可达 5.5V）。掉电保护功能可在掉电时强制所有 I/O 引脚进入高阻抗模式，从而将信号线完全隔离，免受过量泄漏电流的影响。TS3USB3000 的选择引脚与 1.8V 控制电压兼容，允许其直接与移动处理器的通用 I/O (GPIO) 相连。

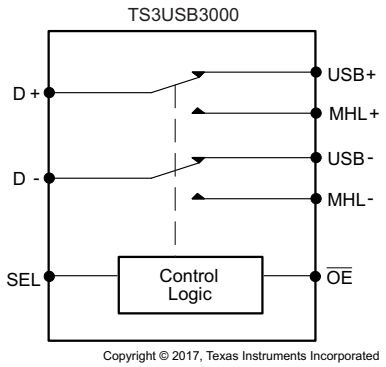
TS3USB3000 采用小型 10 引脚 UQFN 封装，尺寸仅为 1.5mm × 2mm，是移动应用的 理想之选提供所含元件数较少的高效解决方案。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TS3USB3000	UQFN (10)	1.50mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



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4 修订历史记录

Changes from Revision E (July 2018) to Revision F — **Page**

- 删除了重复的“卷带信息” ... 19

Changes from Revision D (November 2017) to Revision E — **Page**

- 将*特性* 从“在 D- 引脚短接至 9V 电压时提供过压保护”更改为“在 D+/- 引脚短接至 9V 电压时提供过压保护” ... 1
- Changed From: V_{D-}, D– DC voltage To: $V_{D+/-}$, D+/- DC voltage in the *Absolute Maximum Ratings* ... 4
- Changed Note (4) From: This rating only applies to the D– pin with respect to GND. To: This rating only applies to the D+/– pins with respect to GND in the *Absolute Maximum Ratings* ... 4
- Changed D- To: D+/- in *Overvoltage Protection When 9-V Short to D+/– Pin* ... 10
- Changed D- To: D+/- in *Pin Leakage* ... 12

Changes from Revision C (January 2017) to Revision D — **Page**

- 更改了*封装选项附录* 器件标记列 ... 19

Changes from Revision B (October 2015) to Revision C — **Page**

- Extended the IC recommended V_{CC} operating range to V_{CC} = 2.3 to 4.8 V in the *特性*, *说明*, *Absolute Maximum Ratings*, *Recommended Operating Conditions*, *Electrical Characteristics*, *Dynamic Characteristics* and *Timing Requirements* sections ... 5

Changes from Revision A (April 2013) to Revision B — **Page**

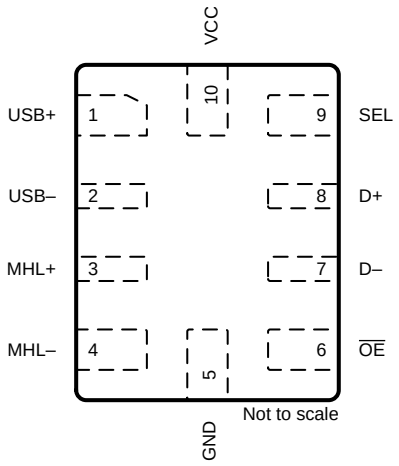
- 已添加*引脚配置和功能*部分，*ESD 额定值*表，*特性*、*说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

Changes from Original (December 2012) to Revision A **Page**

- 已更新 TI 数据表 – 无特定更改。 1

5 Pin Configuration and Functions

RSE Package
10-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	USB+	I/O	USB data (Differential +)
2	USB–	I/O	USB data (Differential –)
3	MHL+	I/O	MHL data (Differential +)
4	MHL–	I/O	MHL data (Differential –)
5	GND	—	Ground
6	$\overline{OE}$	I	Output enable (Active low)
7	D–	I/O	Data switch output (Differential –)
8	D+	I/O	Data switch output (Differential +)
9	SEL	I	Switch select (logic Low = D+/D– to USB+/USB– Logic High = D+/D– to MHL+/MHL–)
10	VCC	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.3	5.5	V
$V_{I/O}$	Input-output DC voltage(3)		–0.3	5.5	V
$V_{D+/-}$	D+/- DC voltage(4)		–0.3	9	V
V_I	Digital input voltage (SEL, $\overline{OE}$)		–0.3	5.5	V
I_K	Input-output port diode current	$V_{I/O} < 0$	–50		mA
I_{IK}	Digital logic input clamp current(3)	$V_I < 0$	–50		mA
I_{CC}	Continuous current through VCC			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) This rating only applies to the D+/– pins with respect to GND. VCC must be powered within the recommended operating conditions of 2.3 V to 4.8 V and the $\overline{OE}$ pin must be logic high for this rating to be applicable. Any condition where VCC is unpowered or the $\overline{OE}$ pin is not high must reference the rest of the *Absolute Maximum Ratings* Table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	4.8	V
$V_{I/O\ (USB)}$	Analog voltage	0	3.6	V
$V_{I/O\ (MHL)}$				
V_I	Digital input voltage (SEL, $\overline{OE}$)	0	V_{CC}	V
T_{RAMP} (V_{CC})	Power supply ramp time requirement (V_{CC})	100	1000	µs/V
T_A	Operating free-air temperature	–40	85	ºC

6.4 Thermal Information

THERMAL METRIC (1)		TS3USB3000 RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	117.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	117.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to +85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		5.7	9	Ω
		V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		5.7	9.5	
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V to 3.45 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.8 V	Switch OFF, $V_{MHL\pm}$ = 1.65 V to 3.45 V, $V_{D\pm}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{MHL\pm}$ = 1.65 V to 3.45 V, $V_{D\pm}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.8 V	Switch ON, $V_{MHL\pm}$ = 1.65 V to 3.45 V, $V_{D\pm}$ = NC	–2		2	µA
		V_{CC} = 2.3 V	Switch ON, $V_{MHL\pm}$ = 1.65 V to 3.45 V, $V_{D\pm}$ = NC	–125		125	
USB SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.3 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		4.6	7.5	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.3 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 2.3 V	$V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.8 V	Switch OFF, $V_{USB\pm}$ = 0 V to 3.6 V, $V_{D\pm}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{USB\pm}$ = 0 V to 3.6 V, $V_{D\pm}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.8 V	Switch ON, $V_{USB\pm}$ = 0 V to 3.6 V, $V_{D\pm}$ = NC	–2		2	µA
		V_{CC} = 2.3 V	Switch ON, $V_{USB\pm}$ = 0 V to 3.6 V, $V_{D\pm}$ = NC	–125		125	
DIGITAL CONTROL INPUTS (SEL, $\overline{OE}$)							
V_{IH}	Input logic high	V_{CC} = 2.3 V to 4.8 V		1.3			V
V_{IL}	Input logic low	V_{CC} = 2.3 V to 4.8 V				0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.8 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = 0 to 4.8 V		–10		10	µA

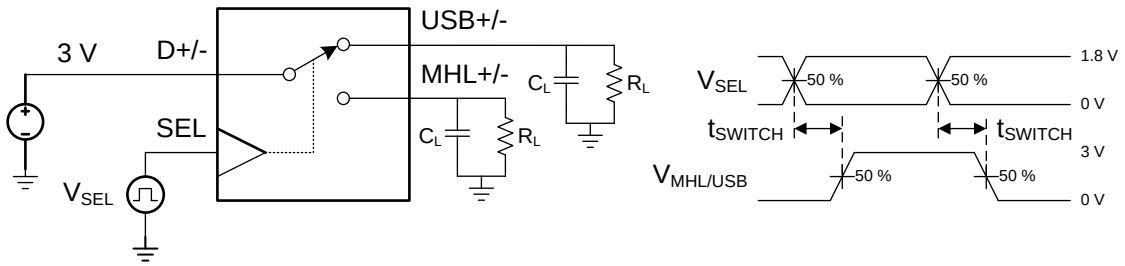
6.6 Dynamic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{ON(MHL)}$	MHL path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.6	2	pF
$C_{ON(USB)}$	USB path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.4	2	pF
$C_{OFF(MHL)}$	MHL path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V f = 240 MHz	Switch OFF		1.4	2	pF
$C_{OFF(USB)}$	USB path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V f = 240 MHz	Switch OFF		1.6	2	pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 or 2 V			2.2		pF
O_{ISO}	OFF Isolation	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω, f = 240 MHz	Switch OFF		–34		dB
X_{TALK}	Crosstalk	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω, f = 240 MHz	Switch ON		–37		dB
$B_{W(MHL)}$	MHL path –3-dB bandwidth	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω, f = 240 MHz	Switch ON		6.1		GHz
$B_{W(USB)}$	USB path –3-dB bandwidth	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω,	Switch ON		6.1		GHz
SUPPLY							
V_{CC}	Power supply voltage			2.3		4.8	V
I_{CC}	Positive supply current	V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF			30	50	µA
$I_{cc, HZ}$	Power supply current in high-Z mode	V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF, $\overline{OE}$ = H			5	10	µA

6.7 Timing Requirements

				MIN	NOM	MAX	UNIT
t_{pd}	Propagation delay		R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 4.8 V		100		ps
t_{switch}	Switching time (SEL to output)	See Figure 1				600	ns
$t_{ZH, ZL (MHL)}$	MHL enable time ($\overline{OE}$ to output)	$V_{I/O}$ = 3.3 V or 0 V			100		µs
$t_{HZ, LZ (MHL)}$	MHL disable time ($\overline{OE}$ to output)				200		ns
$t_{ZH, ZL (USB)}$	USB enable time ($\overline{OE}$ to output)	$V_{I/O}$ = 0.8 V or 0 V			100		µs
$t_{HZ, LZ (USB)}$	USB disable time ($\overline{OE}$ to output)				200		ns
$t_{SK(P)}$	Skew of opposite transitions of same output				20		ps



(1) All input pulses are suppleid by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns

(2) C_L includes probe and jig capacitance.

Figure 1. Timing Diagram

6.8 Typical Characteristics

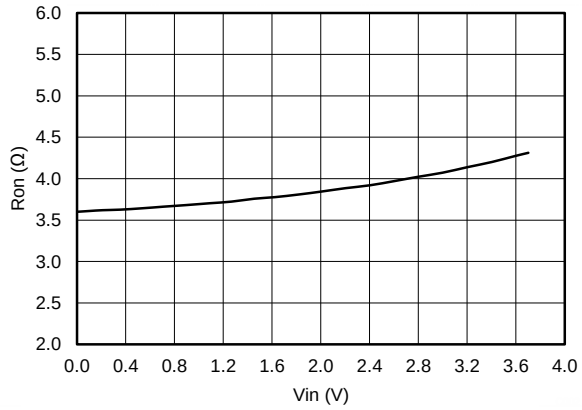


Figure 2. ON-Resistance vs VI for MHL Switch

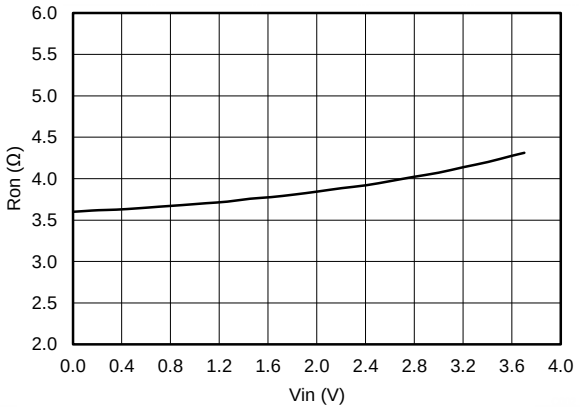


Figure 3. ON-Resistance vs VI for USB Switch

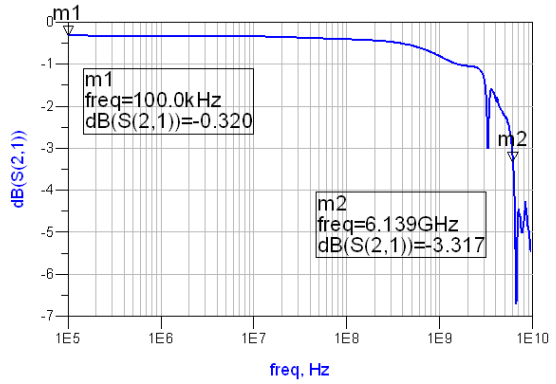


Figure 4. Differential S21 vs Frequency for MHL Switch

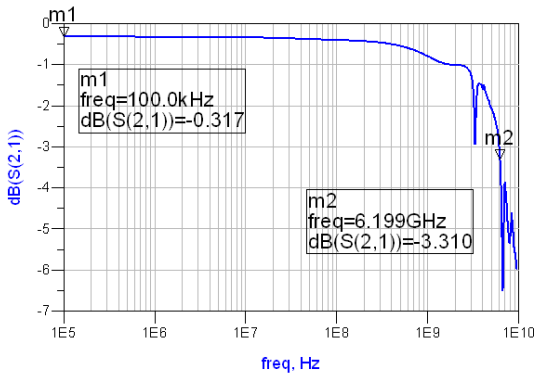


Figure 5. Differential S21 vs Frequency for USB Switch

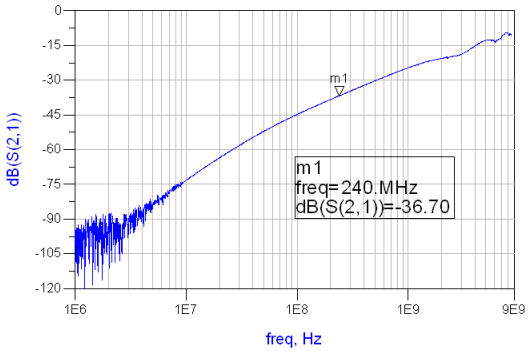


Figure 6. Off Isolation vs Frequency for MHL Path

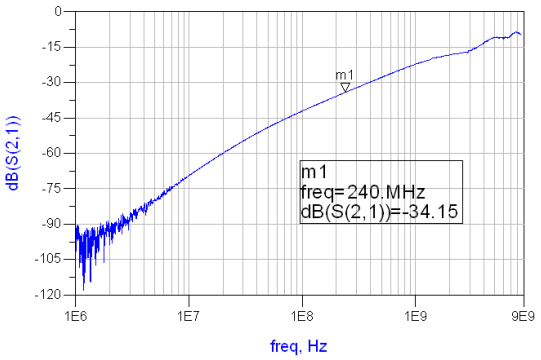


Figure 7. Off Isolation vs Frequency for USB Path

Typical Characteristics (continued)

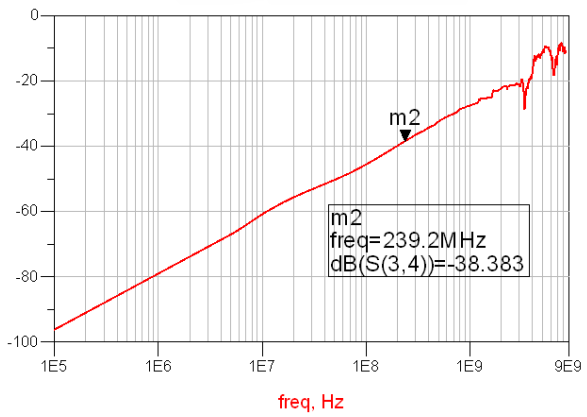


Figure 8. Cross Talk vs Frequency for MHL Path

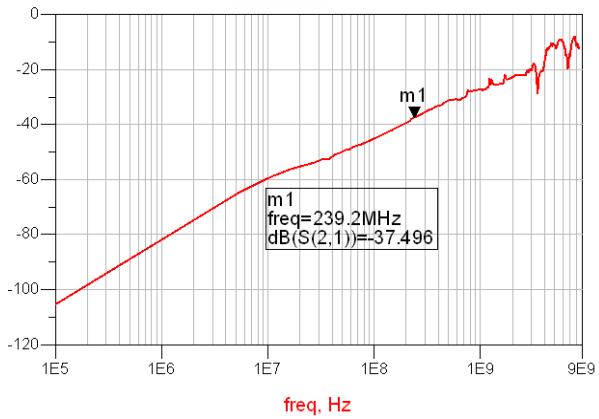
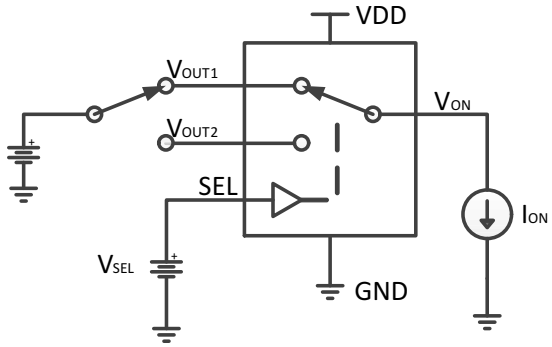


Figure 9. Cross Talk vs Frequency for USB Path

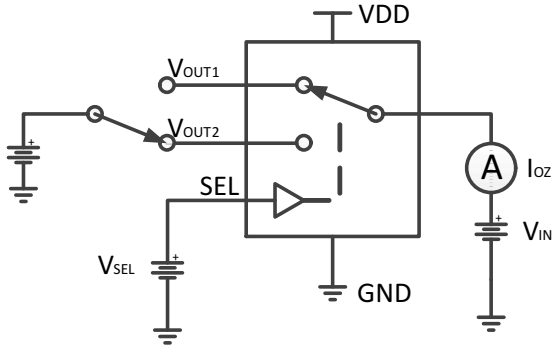
7 Parameter Measurement Information



Channel ON

$R_{ON} = (V_{ON} – V_{I/O1}) / I_{ON}$ or $(V_{ON} – V_{I/O2}) / I_{ON}$
V_{SEL} = H or L

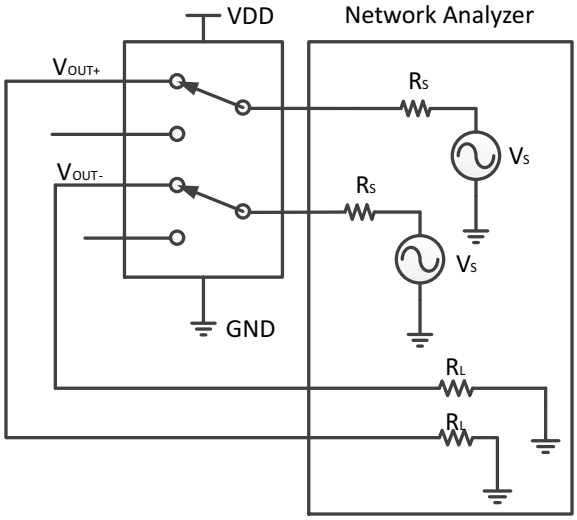
Figure 10. ON-State Resistance (R_{ON})



Channel OFF

V_{SEL} = H or L

Figure 11. OFF Leakage Current (I_{OZ})



Channel ON

V_{SEL} = H or L
$R_S=R_L=50\Omega$

Figure 12. Bandwidth (BW)

8 Detailed Description

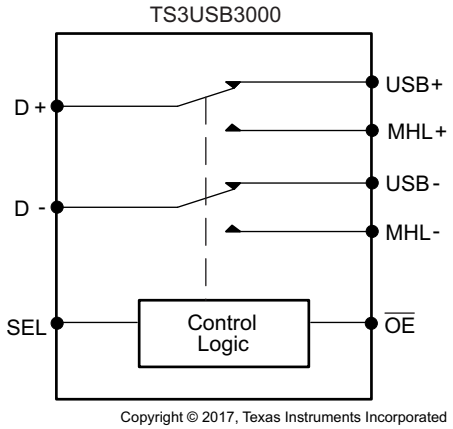
8.1 Overview

The TS3USB3000 device is a 2-channel SPDT switch specially designed for the switching of high-speed MHL and USB 2.0 and 3.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (6.1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs or from one USB connector to two processors or controllers. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that reduces the power consumption to 5 μA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB3000 device integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.5 mm × 2 mm) and is characterized over the free-air temperature range from –40°C to +85°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Power Mode

The TS3USB3000 has a low power mode that reduces the power consumption to 5 μA while the device is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic High signal.

8.3.2 Overvoltage Protection When 9-V Short to D+/– Pin

This section describes how to protect the TS3USB3000 and the surrounding system when the D+/– pin is exposed to voltages greater than 5 V and less than 9 V. Voltages higher than 9 V damages the device.

In charging applications it is possible for the USB plug to be inserted in such a way that the VBUS pin shorts to the D+/– pin of the connector. If there are peripherals on the D+/– pin that cannot tolerate conditions up to 9 V they can be damaged or destroyed. The TS3USB3000 can be used to protect the system from excess voltage if the correct precautions are taken.

Feature Description (continued)

In Figure 13, the system has an application processor (AP) that cannot survive 9 V on the USB data lines. The following procedure protects the system and the TS3USB3000. As stated in the *Absolute Maximum Ratings* table footnotes, the 9 V rating is only applicable while the VCC is powered within the voltage range of the recommended operating conditions and the $\overline{OE}$ pin is high.

1. After a charger is connected to the USB port, the AP detects that a DCP is attached.
2. The AP pulls the $\overline{OE}$ pin high to disable the switches.
3. The AP communicates to the Charger that it can negotiate for a faster charging mode with VBUS at 9 V.
4. The TS3USB3000 is now in a low-power state with the switches disabled and can protect the AP.

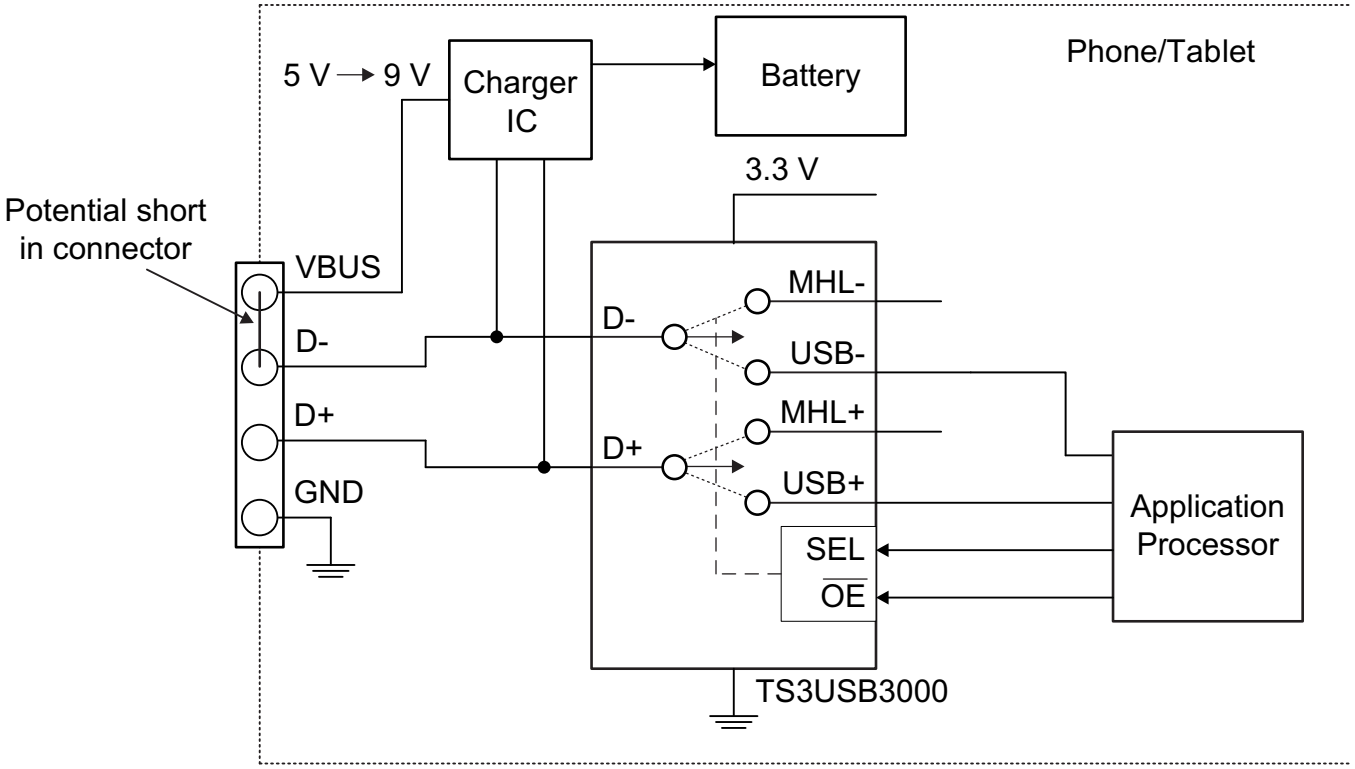


Figure 13. Potential VBUS to D+/– Short Example

Feature Description (continued)

8.3.3 Pin Leakage

When the voltage on the D+/– pins rises above VCC +1 V a leakage path in the device starts conducting as shown in Figure 14. The amount of leakage depends on the VCC voltage and the pin voltage. This leakage is governed by Equation 1:

$$Pin\ Leakage = \frac{V_D - V_{CC}}{12000} \quad (1)$$

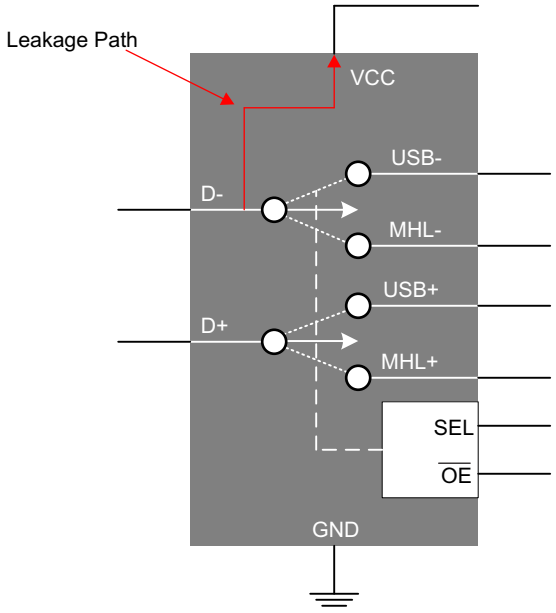


Figure 14. Potential Leakage Path D+/– to VCC

8.4 Device Functional Modes

8.4.1 High Impedance Mode

The TS3USB3000 has a high impedance mode that places all the signal paths in a Hi-Z state while the device is not in use. To put the device in high impedance mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic *High* signal as shown in Table 1.

Table 1. Function Table

SEL	$\overline{OE}$	SWITCH STATUS
X	High	Both USB and MHL switches in High-Z
Low	Low	D+/D– to USB+/USB–
High	Low	D+/D– to MHL+/MHL–

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TS3USB3000 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from on connector to two different locations.

9.2 Typical Application

Figure 15 represents a typical application of the TS3USB3000 USB/MHL switch. The TS3USB3000 is used to switch signals between the USB path, which goes to the baseband or application processor, or the MHL path, which goes to the HDMI to MHL bridge. The TS3USB3000 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$. The pulldown on SEL ensure the USB channel is selected by default. The pulldown on $\overline{OE}$ enables the switch when power is applied. The TS5A3157 is a separate SPDT switch that is used to switch between MHL's CBUS and the USB ID line that is needed for USB OTG (USB On-The-Go) application.

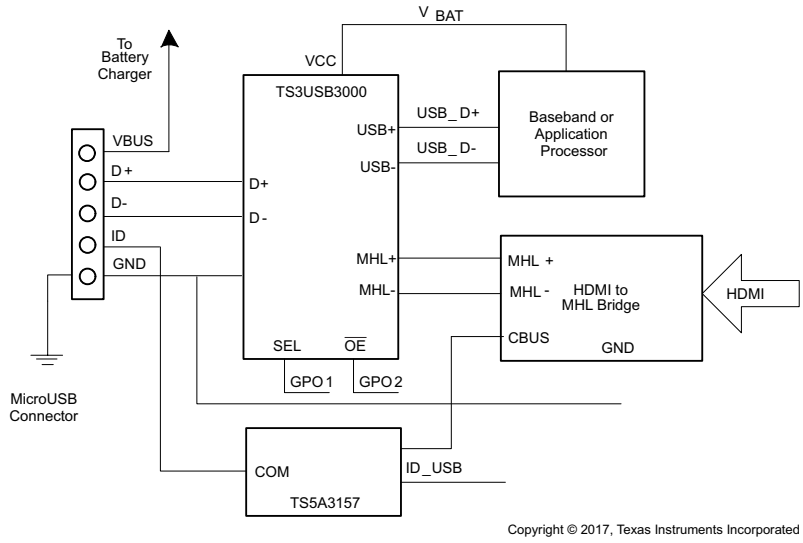


Figure 15. Typical TS3USB3000 Application

9.2.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed. The TS3USB3000 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$, so no external resistors are required on the logic pins. The internal pulldown resistor on SEL ensures the USB channel is selected by default. The internal pulldown resistor on $\overline{OE}$ enables the switch when power is applied to VCC.

9.2.2 Detailed Design Procedure

The TS3USB3000 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

Typical Application (continued)

9.2.3 Application Curves

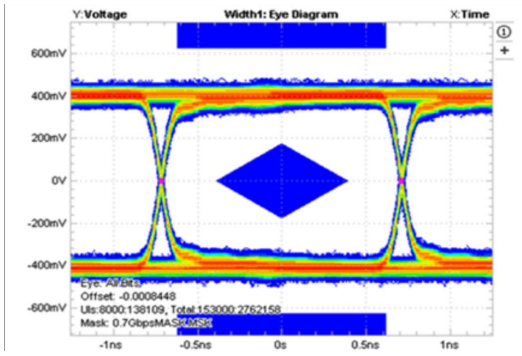


Figure 16. Eye Pattern: 0.7 Gbps With No Device

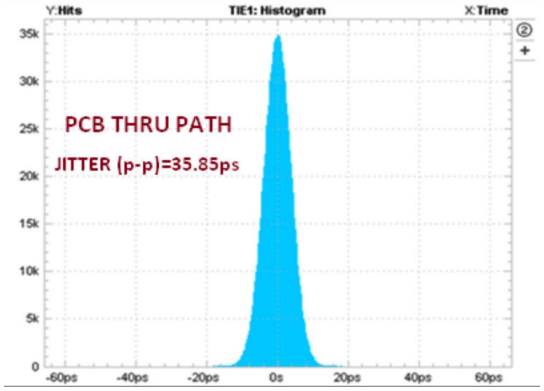
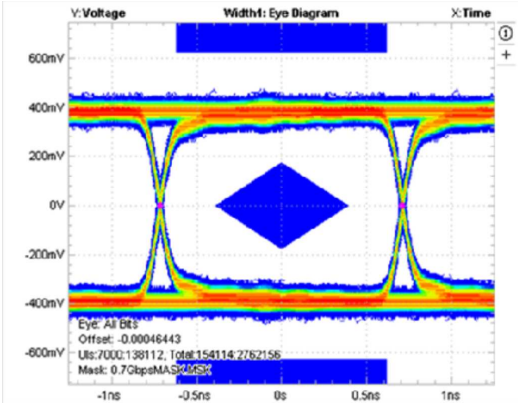
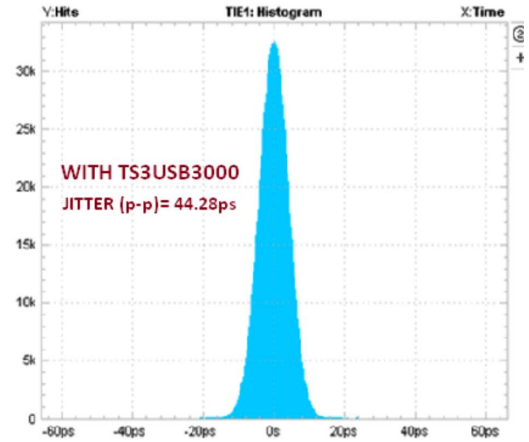


Figure 17. Time Interval Error Histogram: 0.7 Gbps With No Device



The TS3USB3000 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

Figure 18. Eye Pattern: 0.7 Gbps for MHL Switch



The TS3USB3000 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

Figure 19. Time Interval Error Histogram: 0.7 Gbps for MHL Switch

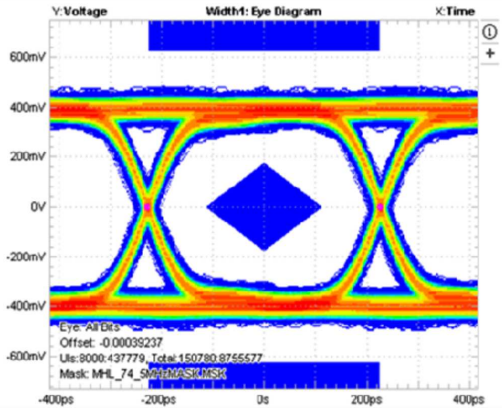


Figure 20. Eye Pattern: 2.2 Gbps With No Device

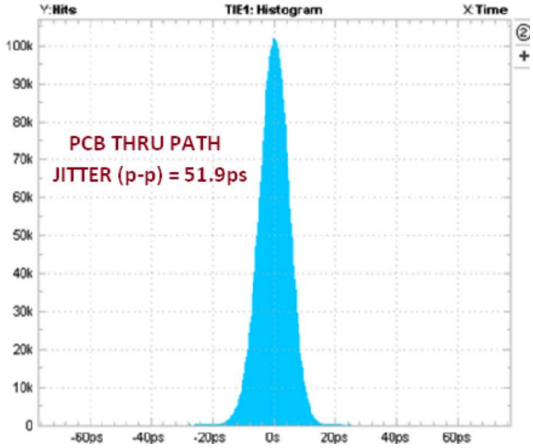
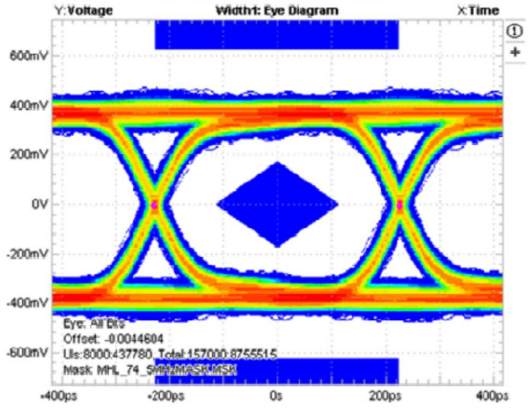


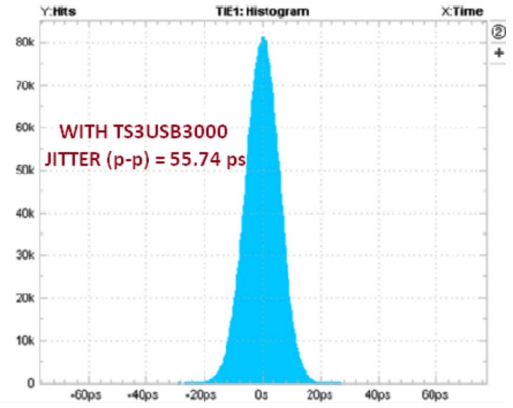
Figure 21. Time Interval Error Histogram: 2.2 Gbps With No Device

Typical Application (continued)



The TS3USB3000 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

Figure 22. Eye Pattern: 2.2 Gbps for MHL Switch



The TS3USB3000 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

Figure 23. Time Interval Error Histogram: 2.2 Gbps for MHL Switch

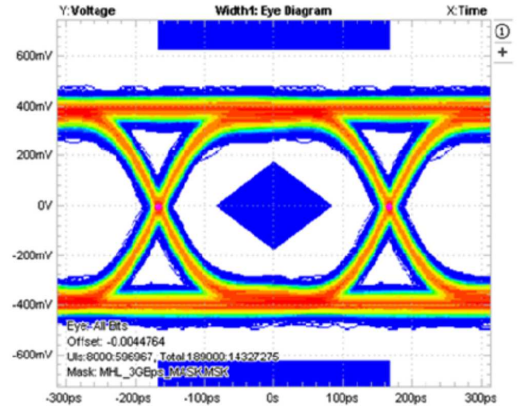


Figure 24. Eye Pattern: 3 Gbps With No Device

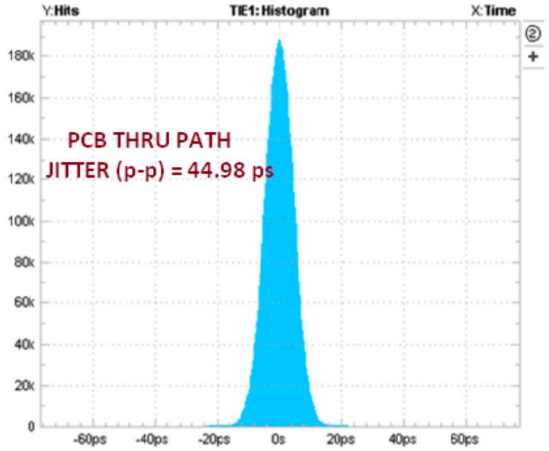
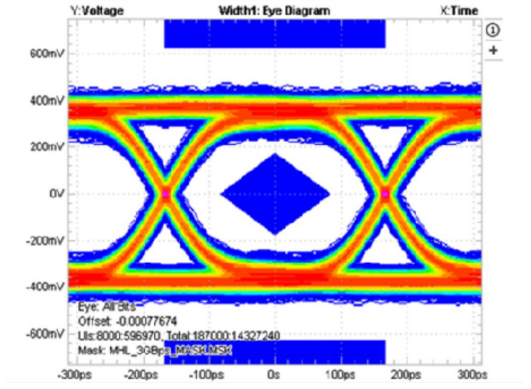
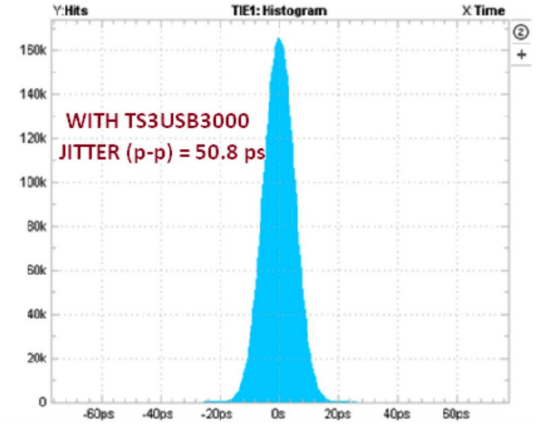


Figure 25. Time Interval Error Histogram: 3 Gbps With No Device



The TS3USB3000 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

Figure 26. Eye Pattern: 3 Gbps for MHL Switch



The TS3USB3000 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

Figure 27. Time Interval Error Histogram: 3 Gbps for MHL Switch

Typical Application (continued)

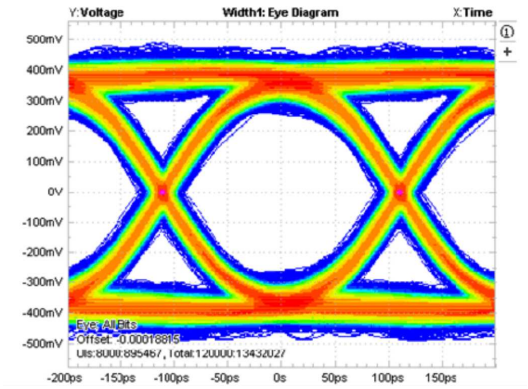


Figure 28. Eye Pattern: 4.5 Gbps With No Device

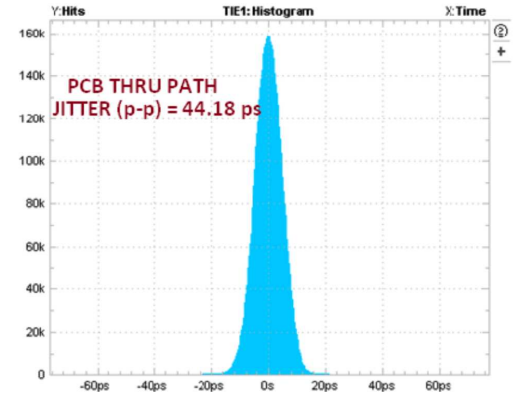
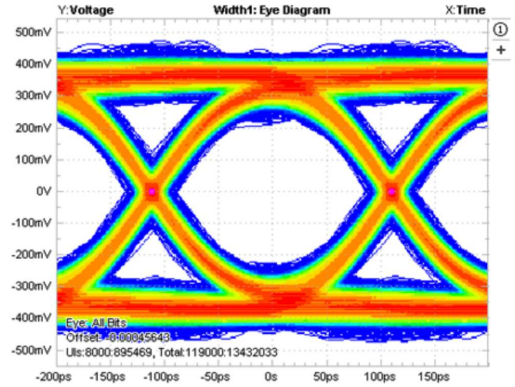
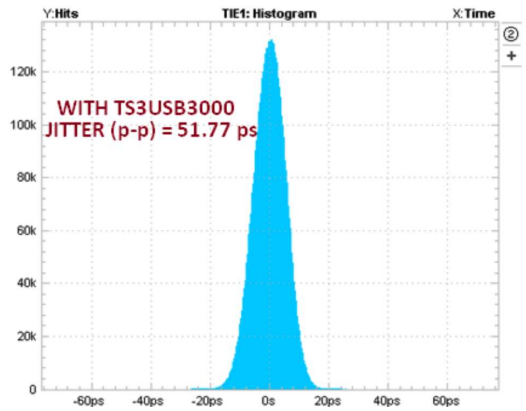


Figure 29. Time Interval Error Histogram: 4.5 Gbps With No Device



The TS3USB3000 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

Figure 30. Eye Pattern: 4.5 Gbps for MHL Switch



The TS3USB3000 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

Figure 31. Time Interval Error Histogram: 4.5 Gbps for MHL Switch

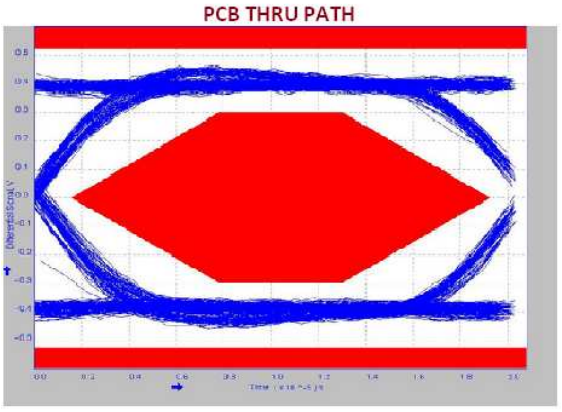


Figure 32. 480-Mbps USB 2.0 Eye Pattern With No Device

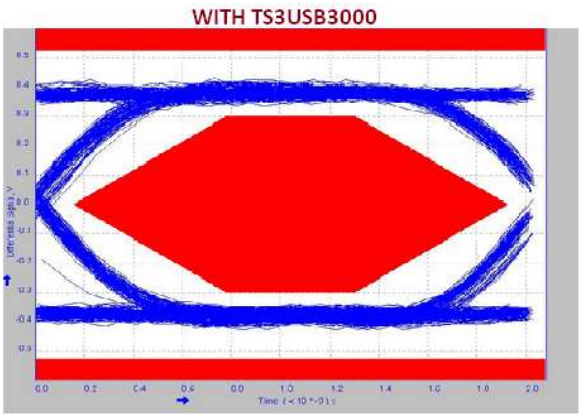


Figure 33. 480-Mbps USB 2.0 Eye Pattern for USB Switch

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D± traces.

The high-speed D± must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 34.

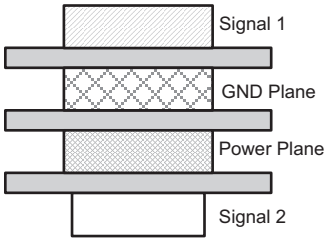


Figure 34. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

11.2 Layout Example

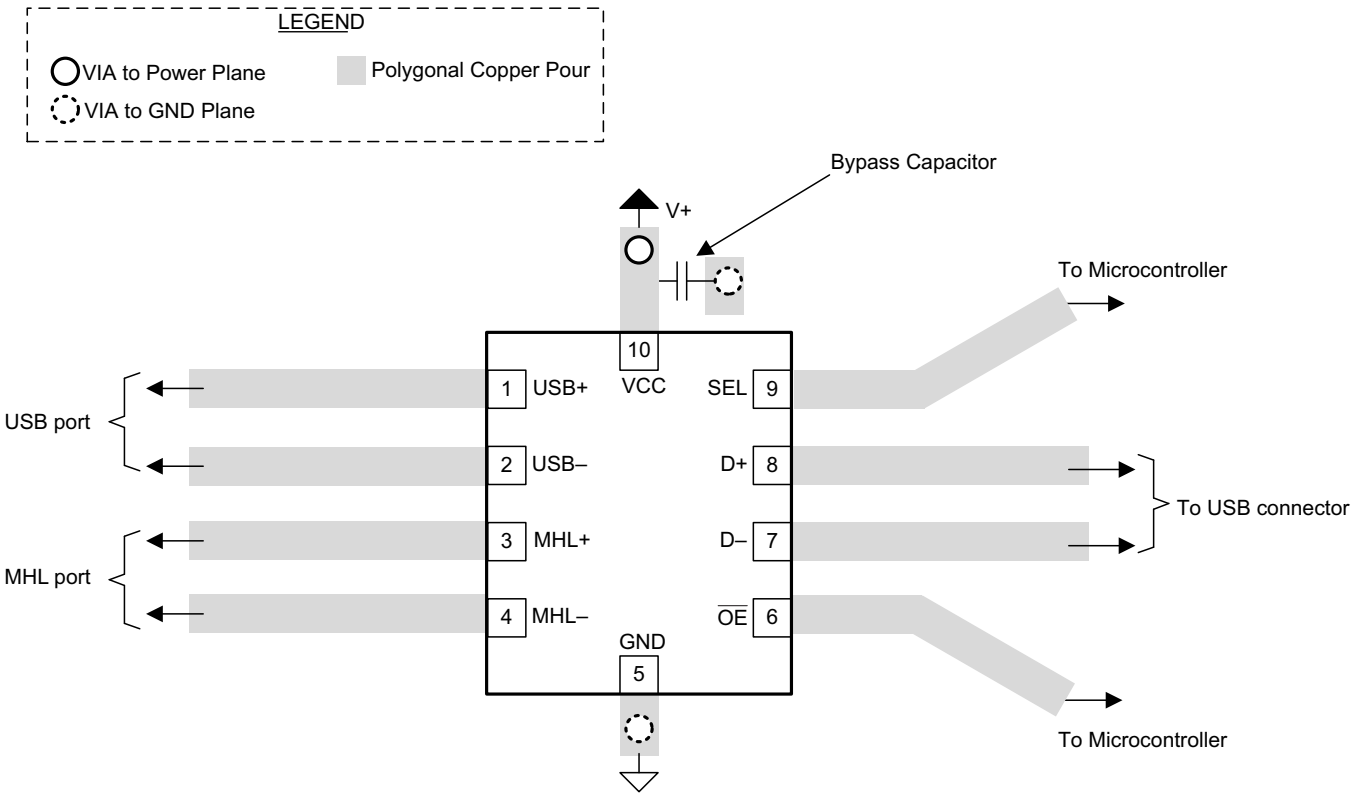


Figure 35. Package Layout Diagram

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *USB 2.0 电路板设计及布线指南*
- *应用报告《高速布局指南》*
- *《高速接口布局指南》*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

13.1 封装选项附录

13.1.1 封装信息

可订购器件	状态 (1)	封装类型	封装图纸	引脚	封装数量	环保计划 (2)	铅/焊球涂层(3)	MSL 峰值温度 (4)	工作温度 (°C)	器件标记(5)(6)
TS3USB3000MRSER	正在供货	UQFN	RSE	10	3000	绿色（RoHS，无锑/溴）	CU NIPDAU	Level-1-260C-UNLIM	-40 至 85	DRJ、DR0、DRR
TS3USB3000RSER	正在供货	UQFN	RSE	10	3000	绿色（RoHS，无锑/溴）	CU NIPDAU	Level-1-260C-UNLIM	-40 至 85	DSJ、DSO、DSR

(1) 销售状态值定义如下：
正在供货：建议用于新设计的产品器件。
限期购买：TI 已宣布器件停产，但购买期限仍有效。
NRND：不推荐用于新设计。为支持现有客户，器件尚在正常生产，但 TI 不建议在新设计中使用此器件。
PRE_PROD：未发布的器件，尚未进行生产，未向大众市场供货，也未在网络上供应，未提供样片。
预览：器件已发布，但尚未生产。可能提供样片，也可能未提供样片。
停产：TI 已停止生产该器件。

(2) 环保计划 - 规划的环保分类包括：无铅 (RoHS)，无铅（RoHS 豁免）或绿色（RoHS，无锑/溴）- 欲了解最新供货信息及更多产品内容详情，请访问 http://www.ti.com.cn/productcontent。
待定：无铅/绿色转换计划尚未确定。
无铅 (RoHS)：TI 所说的“无铅”是指符合针对所有 6 种物质的现行 RoHS 要求的半导体产品，包括要求铅的重量不超过均质材料总重量的 0.1%。因在设计时就考虑到了高温焊接要求，因此 TI 的无铅产品适用于指定的无铅作业。
无铅（RoHS 豁免）：该组件在以下两种情况下具有 RoHS 豁免权：1) 芯片和封装之间使用铅基倒装芯片焊接凸点；2) 芯片和引线框架之间使用铅基芯片粘合剂。否则，组件被归为上面定义的无铅（符合 RoHS）。
绿色（RoHS，无锑/溴）：TI 定义的“绿色”表示无铅（符合 RoHS）以及无溴 (Br) 和锑 (Sb) 系阻燃剂（溴或锑的重量不超过均质材料总重量的 0.1%）。

(3) 铅/焊球涂层 - 可订购器件可能有多种涂层材料选项。各涂层选项用垂直线隔开。如果铅/焊球涂层值超出最大列宽，则会折为两行。

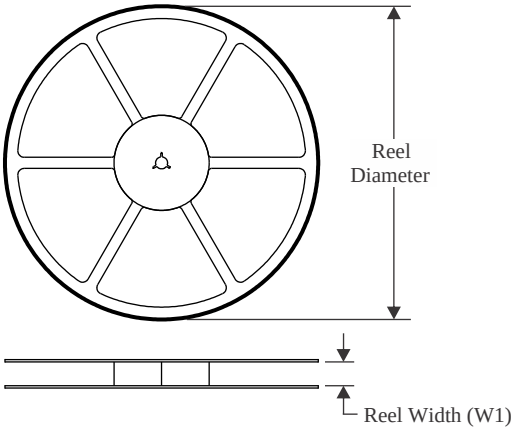
(4) MSL，峰值温度-- 湿敏等级额定值（符合 JEDEC 工业标准分类）和峰值焊接温度。

(5) 器件上可能还有与徽标、批次跟踪代码或环境分类相关的标记。

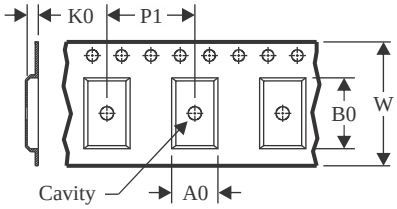
(6) 括号内将包含多个器件标记。不过，器件上仅显示括号中以“~”隔开的其中一个器件标记。如果某一行缩进，说明该行续接上一行，这两行合在一起表示该器件的完整器件标记。

TAPE AND REEL INFORMATION

REEL DIMENSIONS

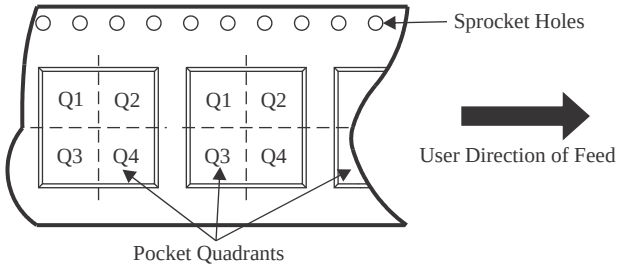


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

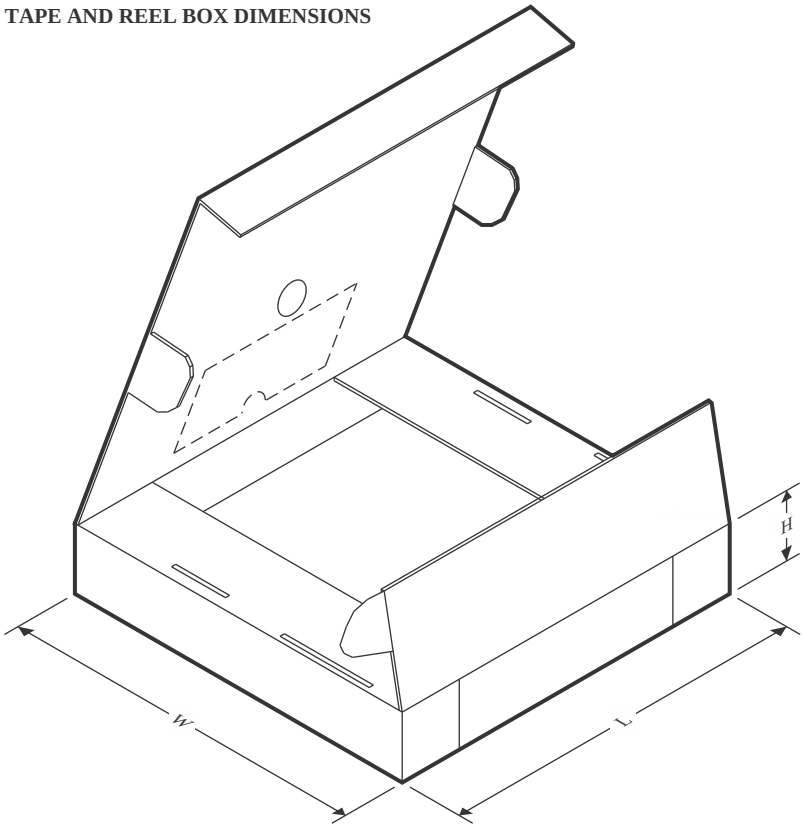
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB3000MRSER	UQFN	RSE	10	3000	180.0	9.5	2.2	1.8	0.75	4.0	8.0	Q3
TS3USB3000RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

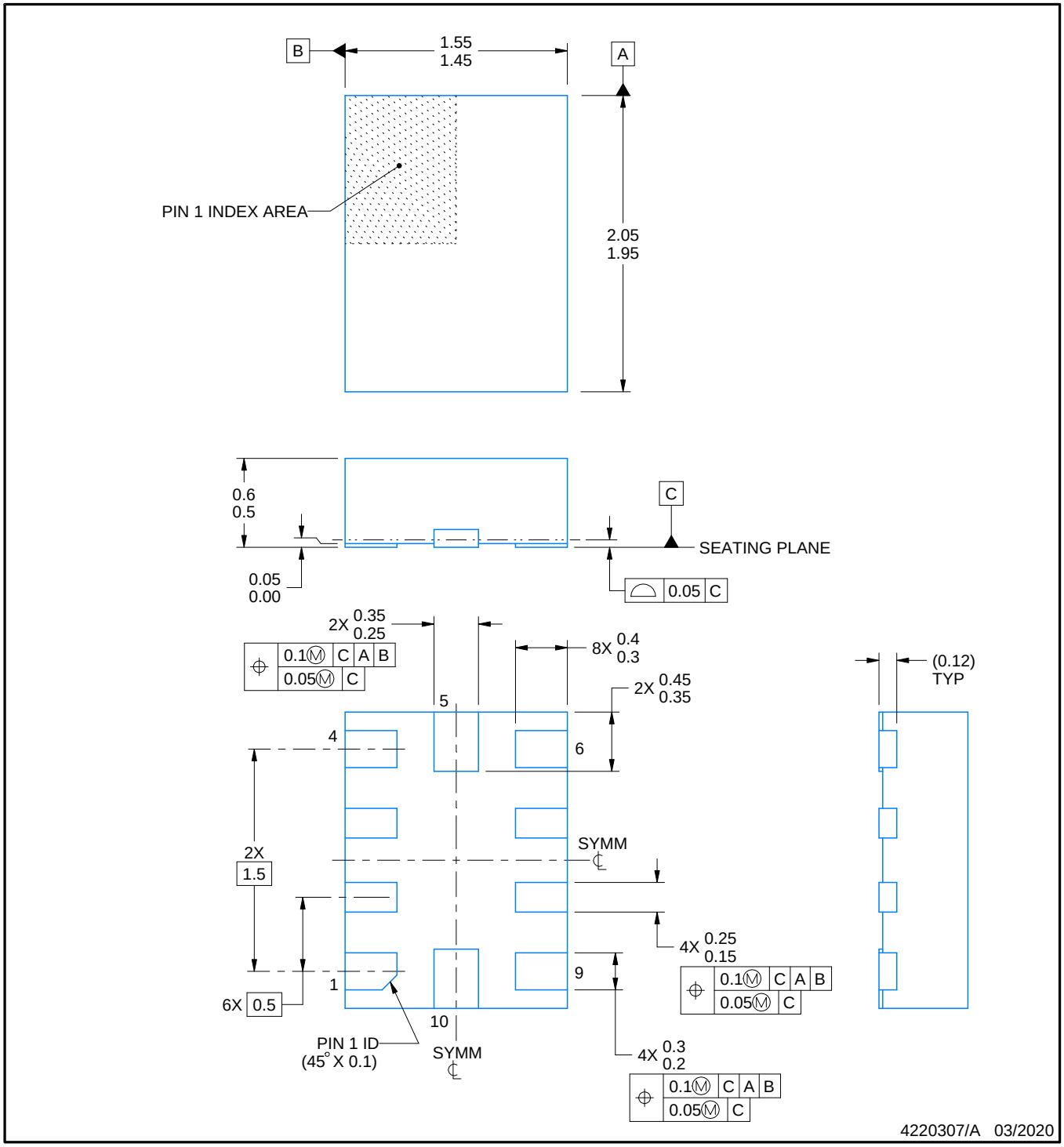
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB3000MRSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TS3USB3000RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

RSE0010A

PACKAGE OUTLINE

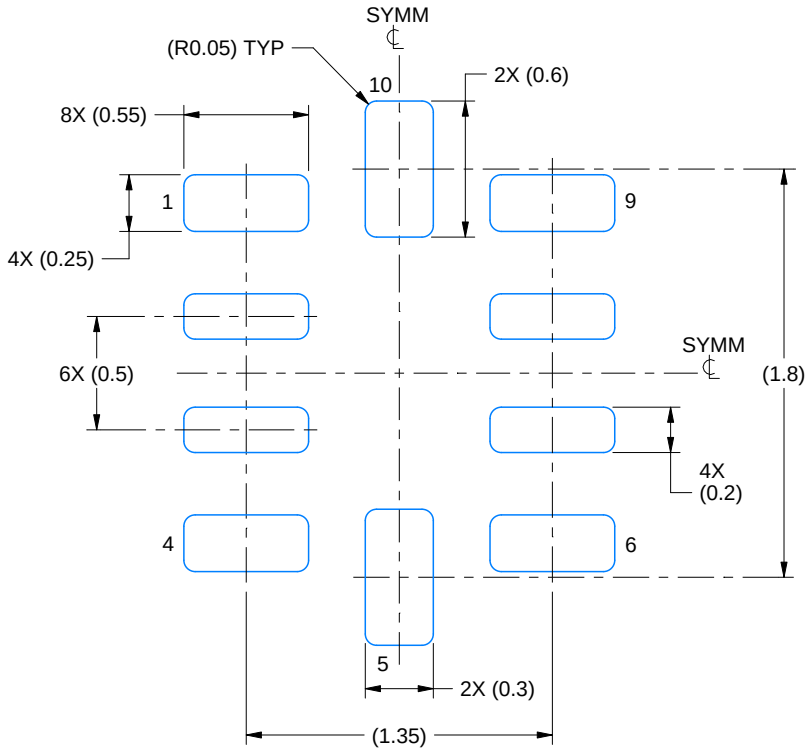
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

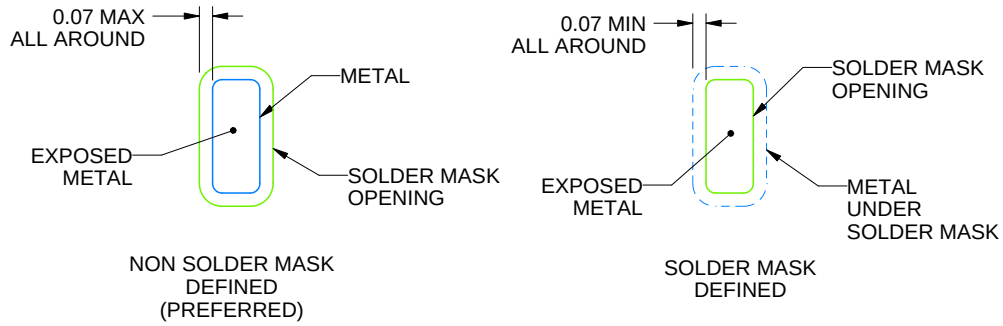


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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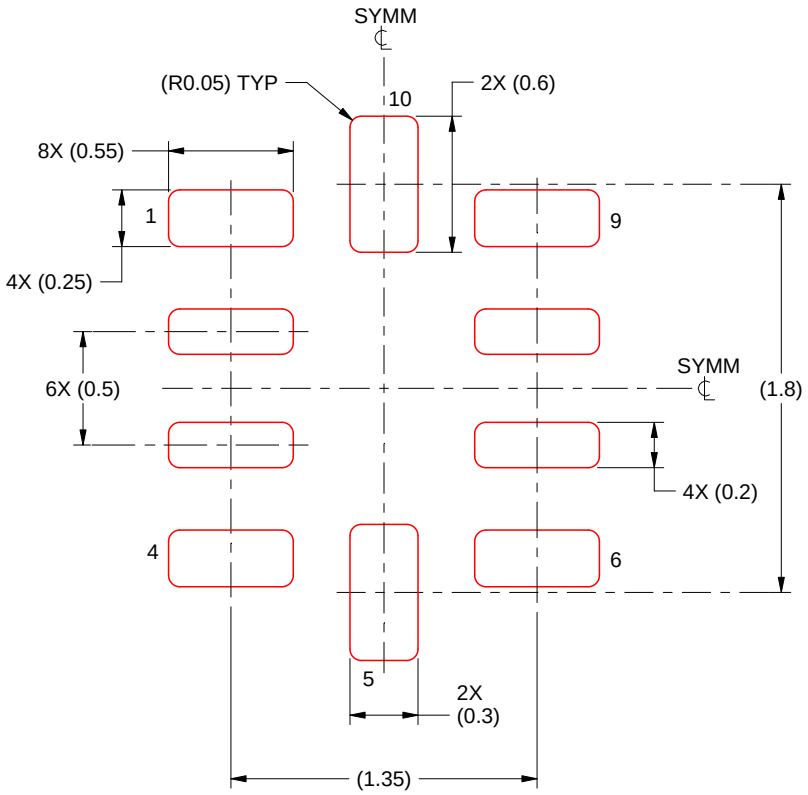
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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