TS3USB30E 具有单使能端和 ESD 保护的高速 USB 2.0 (480Mbps) 1:2 多路复用器/多路信号分离器开关

1 特性

- 在 2.7V 至 4.3V V_{CC} 下运行
- D+/D – 引脚可承受高达 5.25V 的电压
- 1.8V 兼容控制引脚输入
- I_{OFF} 支持局部断电模式运行
- R_{ON} = 10Ω（最大值）
- ΔR_{ON} = 0.35Ω（典型值）
- $C_{io(ON)}$ = 7.5pF（典型值）
- 低功耗（最大值为 70nA）
- –3dB 带宽= 1400MHz（典型值）
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求 [1]
- ESD 性能测试符合 JESD 22 标准
  - 8000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)
- I/O 端口（相对于 GND）的 ESD 性能 [2]
  - 15000V 人体放电模型
- 采用 10 引脚 UQFN (1.8mm × 1.4mm) 封装

2 应用

- 为 USB 1.0、1.1 和 2.0 路由信号
- 通用信号开关
- 便携式电子产品
- 工业
- 消费类产品

3 说明

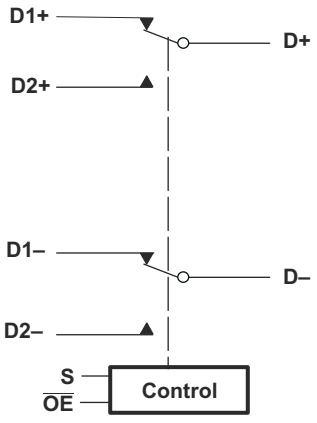
TS3USB30E 是一款高带宽 1:2 开关，专为手持和消费类应用（例如手机、数码相机和具有集线器的笔记本电脑或具有受限 USB I/O 的控制器）中的高速 USB 2.0 信号切换而设计。此开关具有较宽的带宽 (1400MHz)，这一特性使得信号传递具有超低的边缘失真和相位失真。该器件将一个 USB 主机器件的差分输出多路复用到两个相应输出的其中之一，或者将两个不同主机的差分输出多路复用到一个相应的输出。此开关为双向开关，输出端高速信号具有极少或零衰减。TS3USB30E 经过精心设计，可实现低位间偏移和高通道间噪声隔离，并且与高速 USB 2.0 (480Mbps) 等各种标准兼容。

TS3USB30E 在所有引脚上集成了 ESD 保护单元，采用微型 UQFN 封装 (1.8mm × 1.4mm) 或 VSSOP 封装，自然通风条件下的额定工作温度范围为 –40°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
TS3USB30E	DGS（VSSOP，10）	3mm × 4.9mm
	RSW（UQFN，10）	1.8mm × 1.4mm

(1) 有关所有可用封装，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



功能方框图

[1] $\overline{OE}$ 和 S 输入除外
[2] 除标准 HBM 测试（A114-B，II 类）外还执行了高压 HBM 测试，仅适用于相对于 GND 进行测试的 I/O 端口。

Table of Contents

4 Pin Configuration and Functions

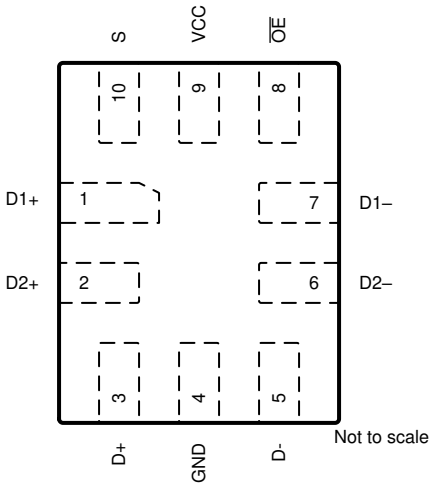


图 4-1. RSW Package 10-Pin UQFN Top View

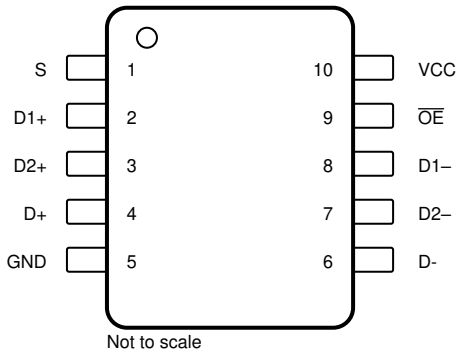


图 4-2. DGS Package 10-Pin VSSOP Top View

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	UQFN	VSSOP		
D+	3	4	I/O	Common USB signal path
D –	5	6	I/O	
D1+	1	2	I/O	USB signal path port 1
D1 –	7	8	I/O	
D2+	2	3	I/O	USB signal path port 2
D2 –	6	7	I/O	
GND	4	5	—	Ground
$\overline{OE}$	8	9	I	Bus-switch enable
S	10	1	I	Select input
VCC	9	10	—	Voltage supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_{IN}	Control input voltage		–0.5	7	V
$V_{I/O}$	Signal path I/O voltage (3)	D+, D– when V_{CC} > 0V	–0.5	V_{CC} + 0.3	V
		D+, D– when V_{CC} = 0V	–0.5	5.25	
I_{IK}	Control input clamp current	V_{IN} < 0V		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0V		–50	mA
$I_{I/O}$	ON-state switch current(4)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(4) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	8000	V
			I/O port to GND	15000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)		1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 3V to 3.6V	1.3	V_{CC}	V
		V_{CC} = 4.3V	1.7	V_{CC}	
V_{IL}	Low-level control input voltage	V_{CC} = 3V to 3.6V	0	0.5	V
		V_{CC} = 4.3V	0	0.7	
$V_{I/O}$	Data input/output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

THERMAL METRIC(1)		Device		UNIT
		DGS (VSSOP)	RSW (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.1	114.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.7	64.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.0	21.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.2	1.9	°C/W

THERMAL METRIC(1)		Device		UNIT
		DGS (VSSOP)	RSW (UQFN)	
		10 PINS	10 PINS	
ψ_{JB}	Junction-to-board characterization parameter	121.6	21.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{IK}	Control inputs clamp voltage	V_{CC} = 3V, I_I = –18mA			–1.2	V
I_{IN}	Control inputs	V_{CC} = 4.3V, 0V, V_{IN} = 0V to 4.3V			±1	µA
I_{OZ}	D+ and D– OFF-state leakage current(3)	V_{CC} = 4.3V, V_O = 0V to 3.6V, V_I = 0V, Switch OFF			±1	µA
I_{OFF}	Powered off leakage current	V_{CC} = 0V, V_O = 0V to 4.3V, V_I = 0V, V_{IN} = V_{CC} or GND			±2	µA
I_{CC}	Supply current	V_{CC} = 4.3V, $I_{I/O}$ = 0mA, Switch ON or OFF			1	µA
ΔI_{CC} (4)	Control inputs	V_{CC} = 4.3V, V_{IN} = 2.6V			10	µA
C_{in}	Control inputs digital input capacitance	V_{CC} = 0V, V_{IN} = V_{CC} or GND		1		pF
$C_{io(OFF)}$	OFF-state input capacitance	V_{CC} = 3.3V, $V_{I/O}$ = 3.3V or 0V, Switch OFF		2		pF
$C_{io(ON)}$	ON-state input capacitance	V_{CC} = 3.3V, $V_{I/O}$ = 3.3V or 0V, Switch ON		7.5		pF
R_{ON}	ON-state resistance(5)	V_{CC} = 3V, V_I = 0.4V, I_O = –8mA		6	10	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3V, V_I = 0.4V, I_O = –8mA		0.35		Ω
$r_{on(flat)}$	ON-state resistance flatness	V_{CC} = 3V, V_I = 0V or 1V, I_O = –8mA		2		Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50Ω, f = 240MHz, See 图 6-3	–32	dB
O_{ISO}	OFF isolation	R_L = 50Ω, f = 240MHz, See 图 6-2	–32	dB
BW	Bandwidth (–3 dB)	R_L = 50Ω, See 图 6-4	1400	MHz

(1) For minimum or maximum conditions, use the appropriate value specified under *Electrical Characterisics* for the applicable device type.

5.7 Switching Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)	R_L = 50Ω, C_L = 5pF, At 480Mbps, See 图 6-5		0.25		ns
t_{ON}	Line enable time, SEL to D, nD	R_L = 50Ω, C_L = 5pF, See 图 6-1			30	ns
t_{OFF}	Line disable time, SEL to D, nD	R_L = 50Ω, C_L = 5pF, See 图 6-1			25	ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50Ω, C_L = 5pF, See 图 6-1			30	ns

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3V ±10%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50Ω, C_L = 5pF, See 图 6-1			25	ns
$t_{SK(O)}$	Output skew between center port to any other port(2)	R_L = 50Ω, C_L = 5pF, See 图 6-6			50	ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50Ω, C_L = 5pF, See 图 6-6			20	ps
t_J	Total jitter(2)	R_L = 50Ω, C_L = 5pF, t_R = t_F = 500ps at 480Mbps (PRBS = 2^{15} – 1)			20	ps

(1) For minimum or maximum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, bus switch adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

5.8 Typical Characteristics

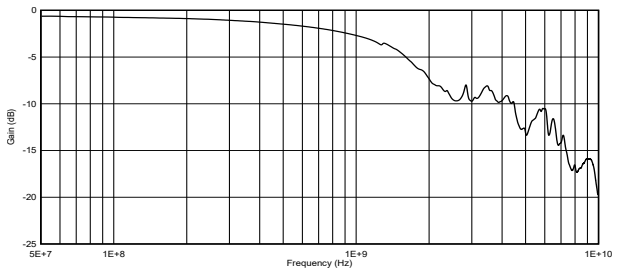


图 5-1. Gain vs Frequency

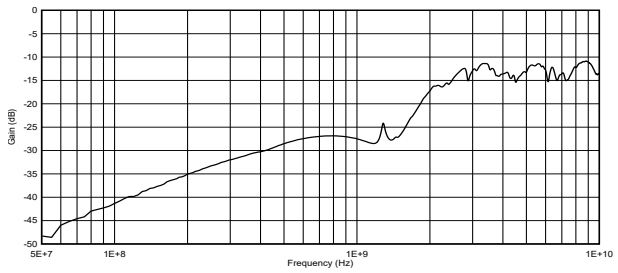


图 5-2. OFF Isolation

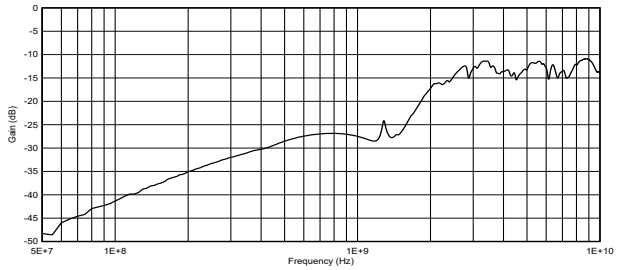
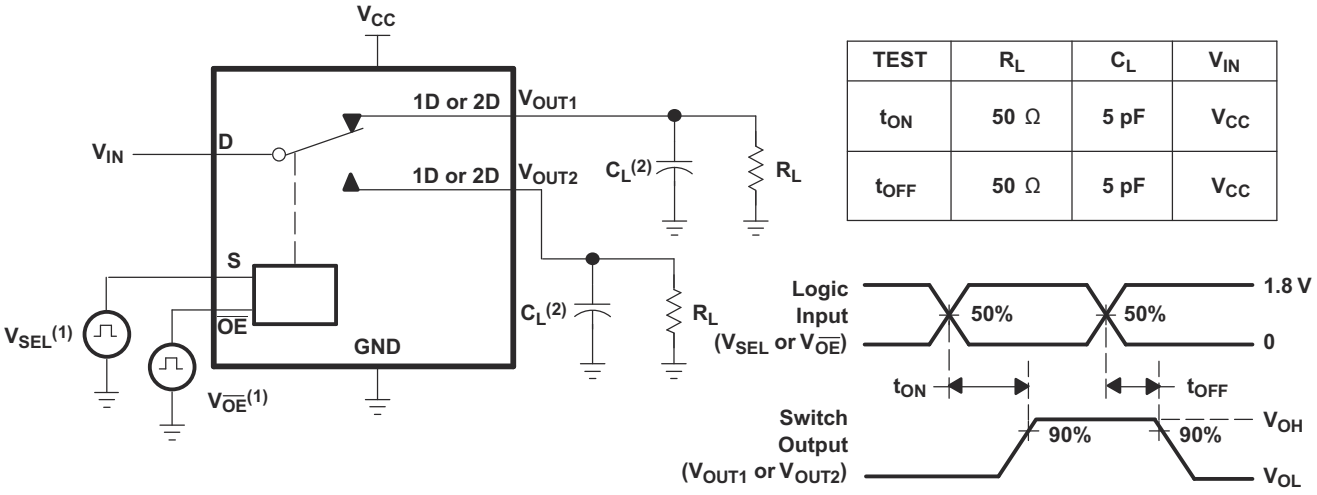


图 5-3. Crosstalk

6 Parameter Measurement Information



TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 5ns, t_f < 5ns.
B. C_L includes probe and jig capacitance.

图 6-1. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

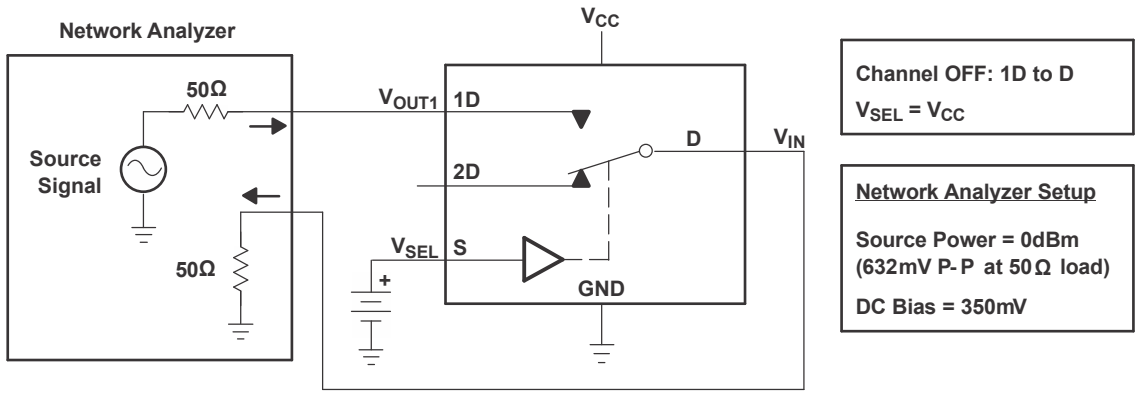


图 6-2. OFF Isolation (O_{ISO})

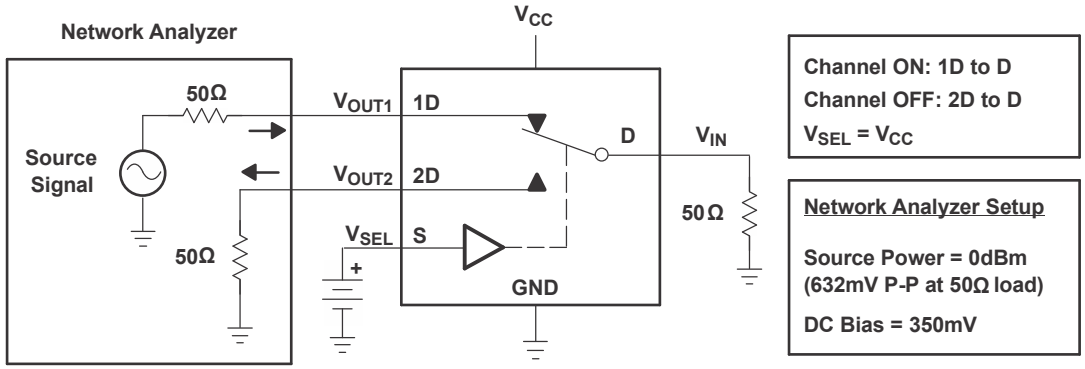


图 6-3. Crosstalk (X_{TALK})

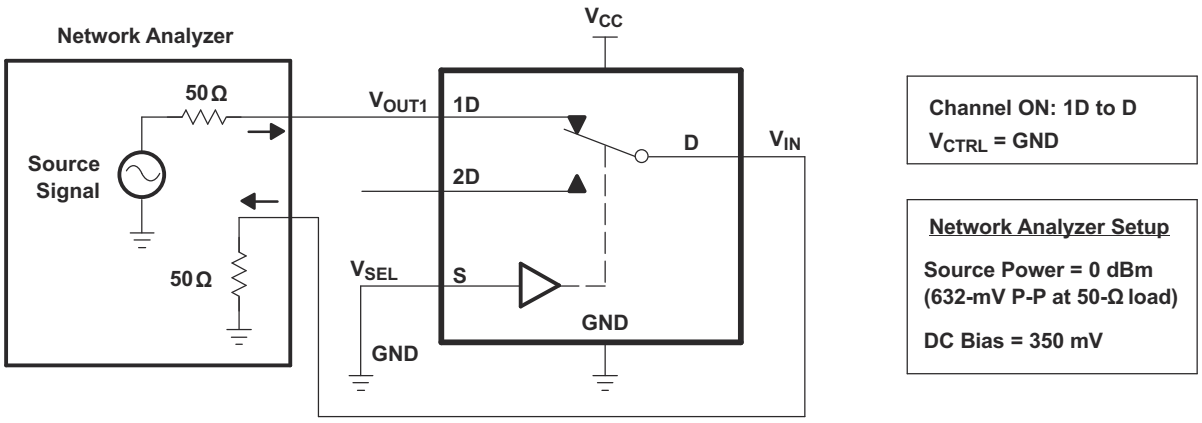


图 6-4. Bandwidth (BW)

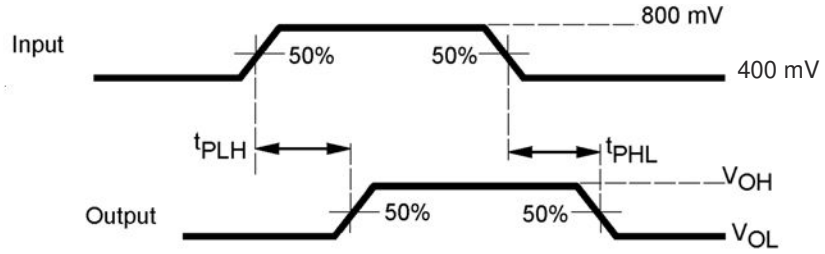
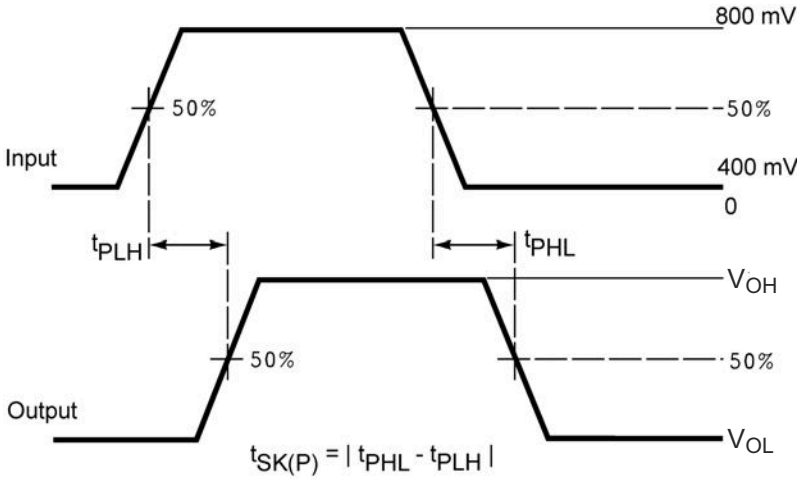
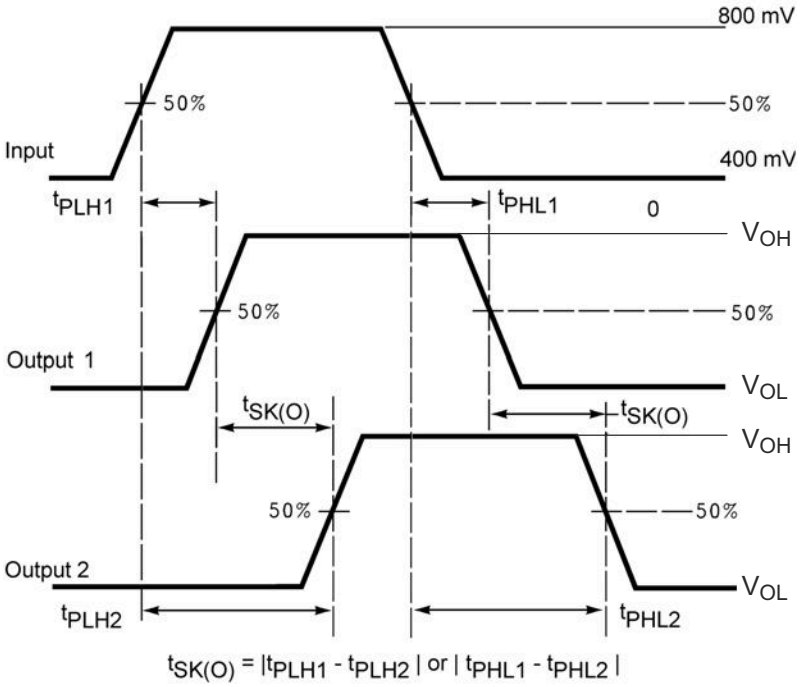


图 6-5. Propagation Delay



Pulse Skew $t_{SK(P)}$



Output Skew $t_{SK(P)}$

图 6-6. Skew Test

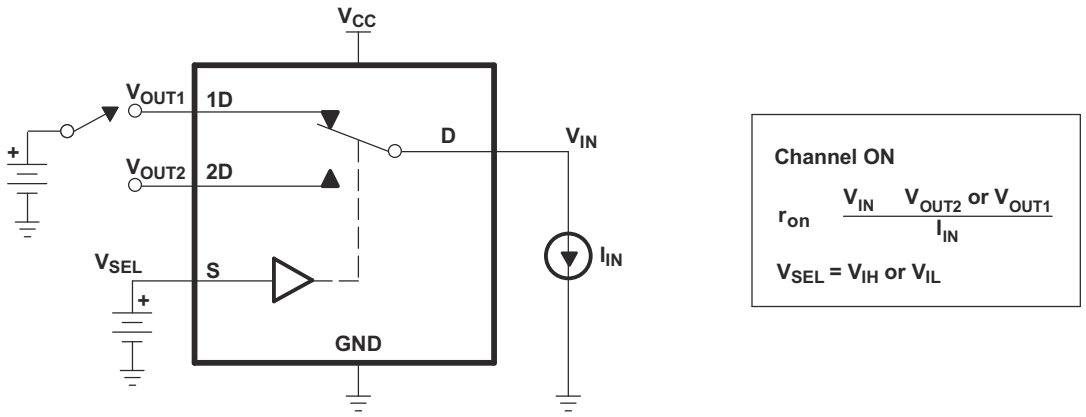


图 6-7. ON-State Resistance (R_{ON})

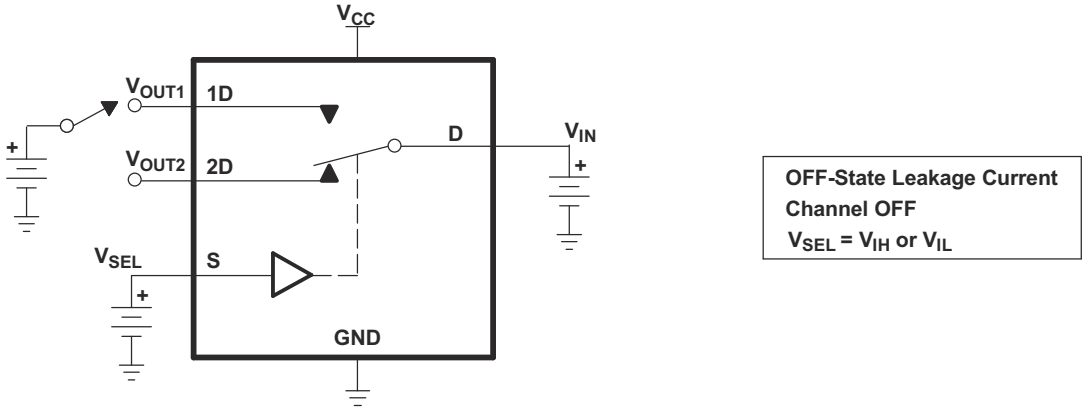


图 6-8. OFF-State Leakage Current

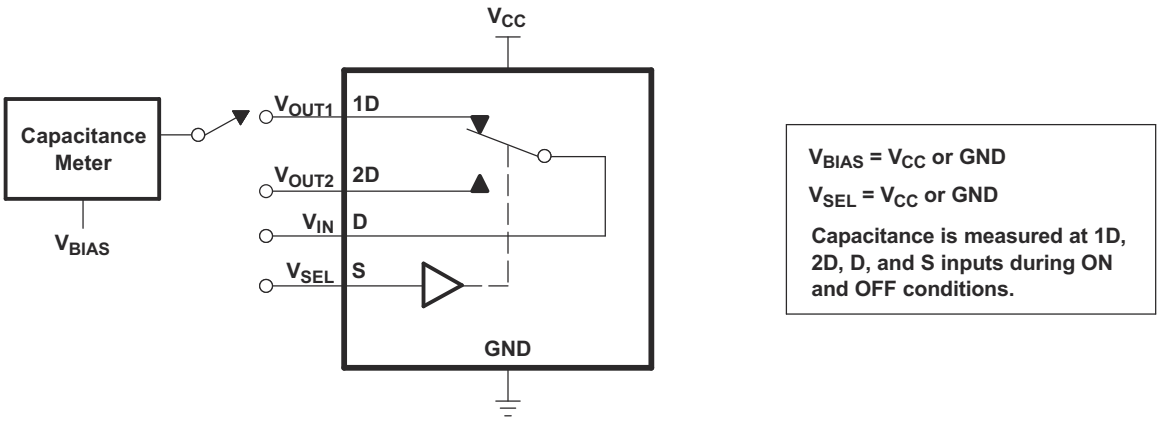


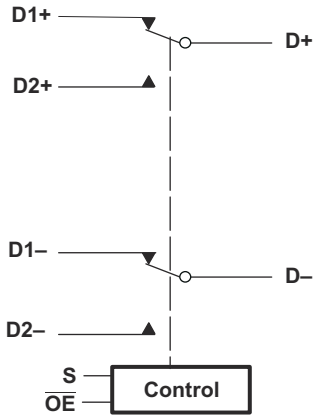
图 6-9. Capacitance

7 Detailed Description

7.1 Overview

The TS3USB30E is a high-bandwidth switch specially designed for the switching and isolating of high-speed USB 2.0 signals in systems with limited USB I/Os. The wide bandwidth (1400MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs or from two different hosts to one corresponding output. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The switch is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards such as high-speed USB 2.0 (480Mbps).

7.2 Functional Block Diagram



7.3 Feature Description

The TS3USB30E has a bus-switch enable pin $\overline{OE}$ that can place the signal paths in high impedance. This allows the user to isolate the bus when the bus is not in use to consume less current.

7.4 Device Functional Modes

The device functional modes are shown in 表 7-1.

表 7-1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB30E solution can effectively expand the limited USB I/Os by switching between multiple USB buses to a single USB hub or controller. The TS3USB30E can also be used to connect a single USB controller to two USB connectors or controllers.

8.2 Typical Application

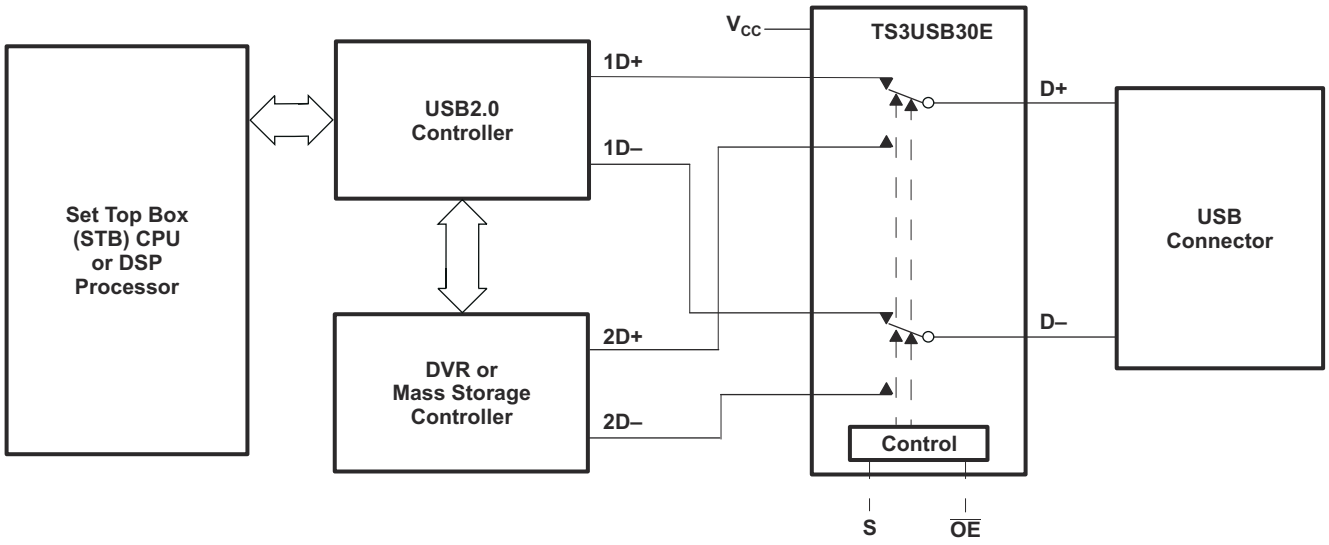


图 8-1. Application Diagram

8.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed. TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.2 Detailed Design Procedure

The TS3USB30E can be properly operated without any external components. However, TI recommends to connect any unused pins to ground through a 50 Ω resistor to prevent signal reflections back into the device.

8.2.3 Application Curves

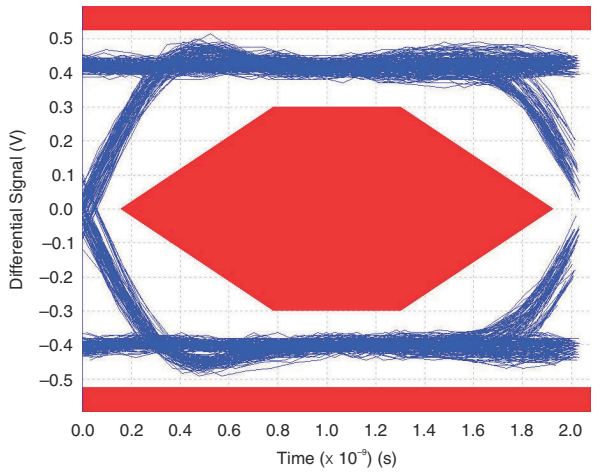


图 8-2. Eye Pattern: 480Mbps USB Signal With No Switch (Through Path)

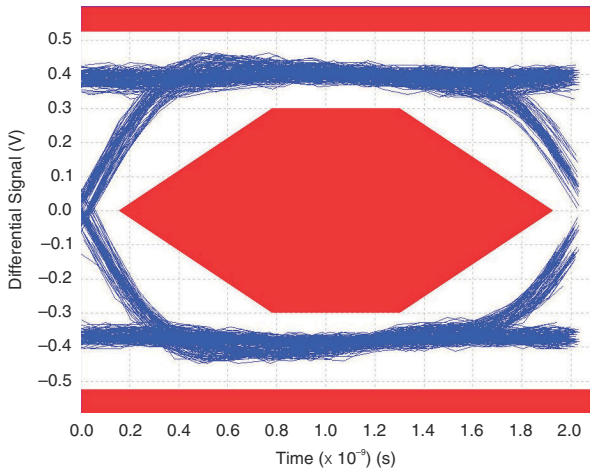


图 8-3. Eye Pattern: 480Mbps USB Signal With Switch NC Path

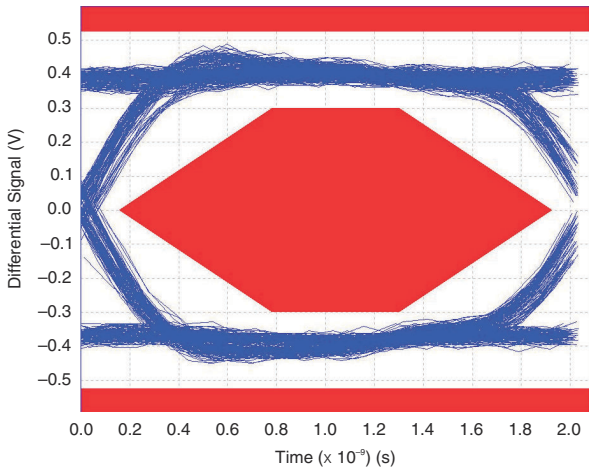


图 8-4. Eye Pattern: 480Mbps USB Signal With Switch NO Path

8.3 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D – traces.

The high-speed D+ and D – traces must always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, make sure the impedance of D+ and D – traces match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners to reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because the stubs can cause signal reflections. If a stub is unavoidable, then make sure the stub is less than 200mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* and *USB 2.0 Board Design and Layout Guidelines*.

8.4.2 Layout Example

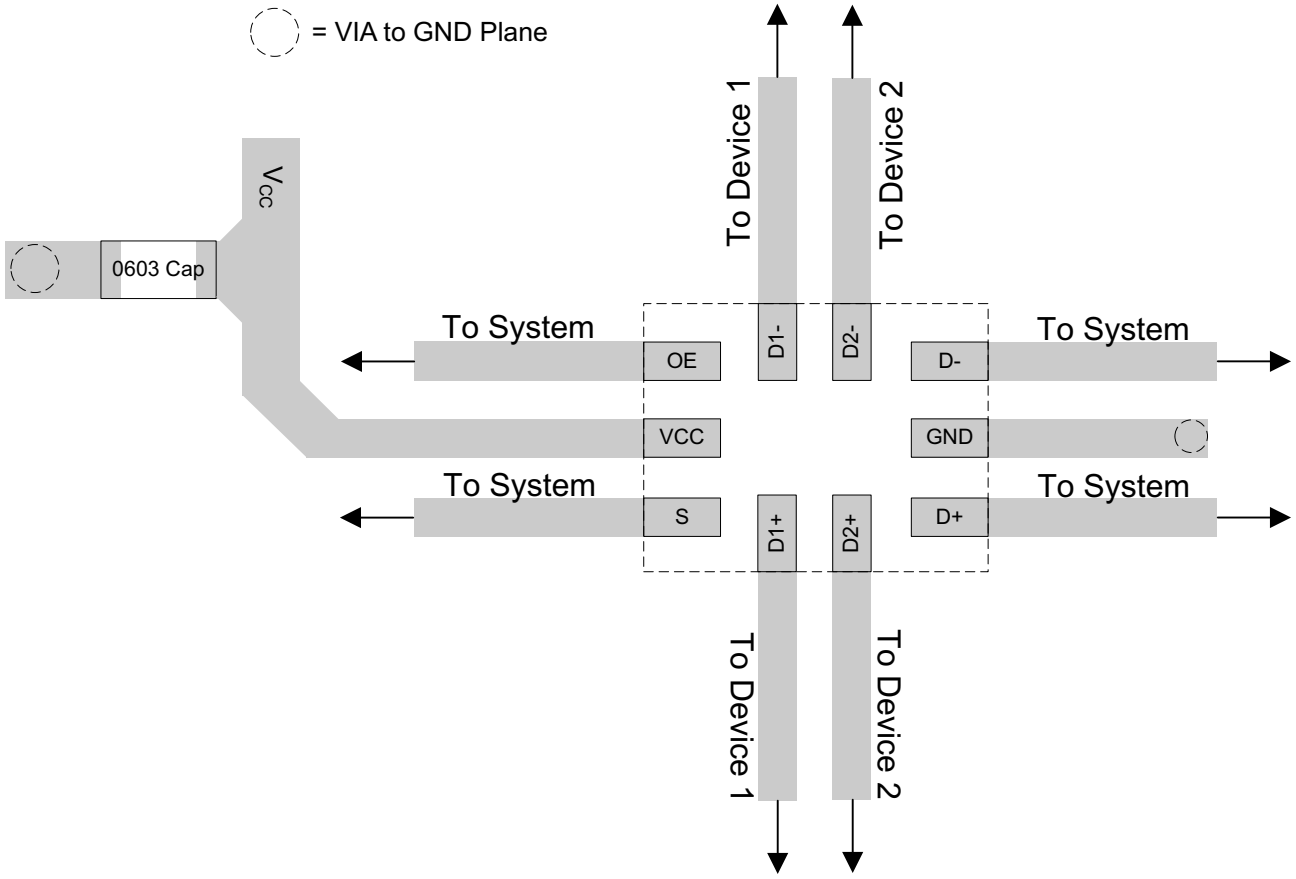


图 8-5. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *High Speed Layout Guidelines*
- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (August 2015) to Revision G (October 2024)	Page
• Changed the *Pin Configuration* images and removed the RSW bottom view pinout	3
• Removed footnote in *Absolute Maximum Ratings* which stated "The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed."	4
• Changed XTALK from -54dB to -32dB	5
• Changed OISO from -40dB to -32dB	5
• Changed BW from 900MHz to 1400GHz and removed CL = 5pF from Test Conditions	5
• Changed the *Gain vs Frequency* graph	7
• Changed the *Crosstalk (X_{TALK})* graph	7
• Changed the *Off Isolation (O_{ISO})* graph	7
• Removed the 50 Ω pulldown resistor on VOUT1 from the *Off Isolation (O_{ISO})* image	8
• Added the text D next to V_{IN} the *Crosstalk (X_{TALK})* image	8

Changes from Revision E (August 2012) to Revision F (August 2015) **Page**

- 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- 将*说明*中的封装类型从 DGS 更改为 VSSOP 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB30EDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L6Q, L6R)	Samples
TS3USB30ERSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LY7, LYO, LYV)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

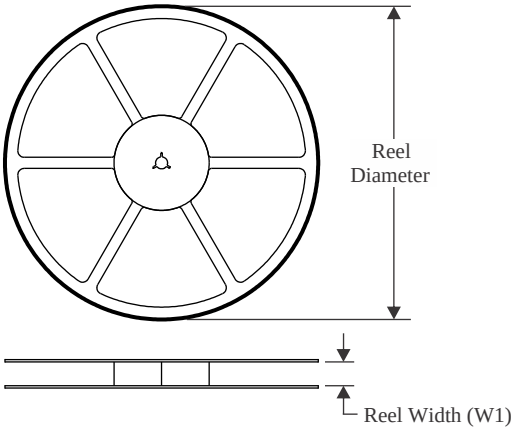
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

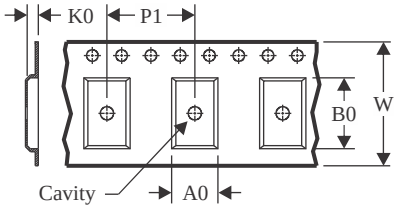
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

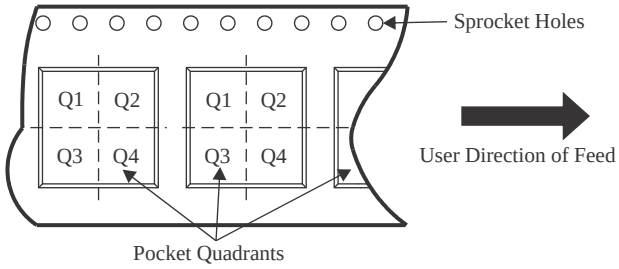


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

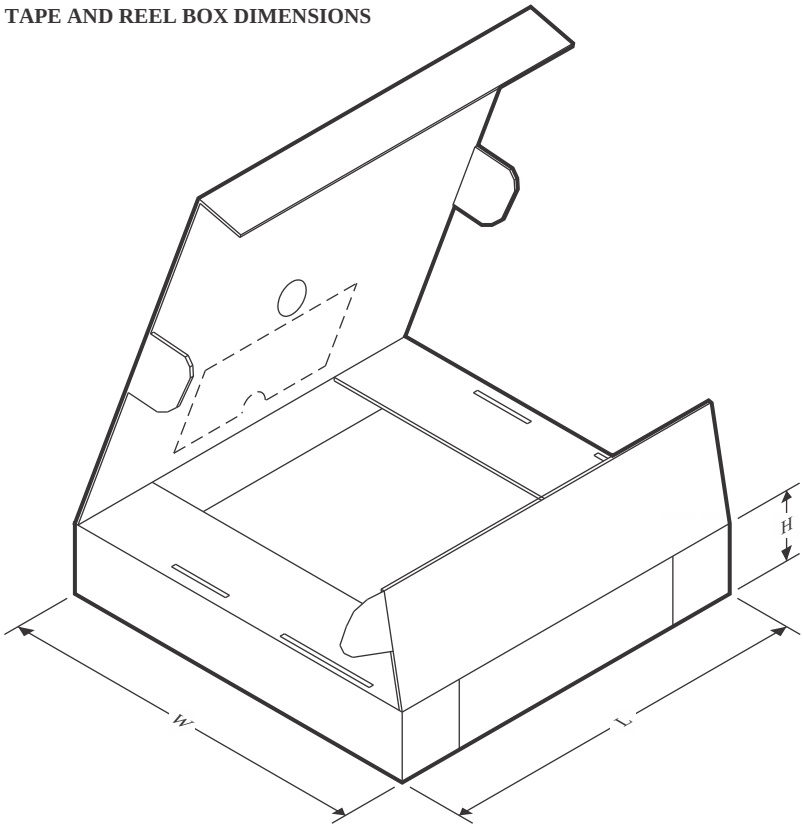
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB30EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3USB30ERSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
TS3USB30ERSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	4.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

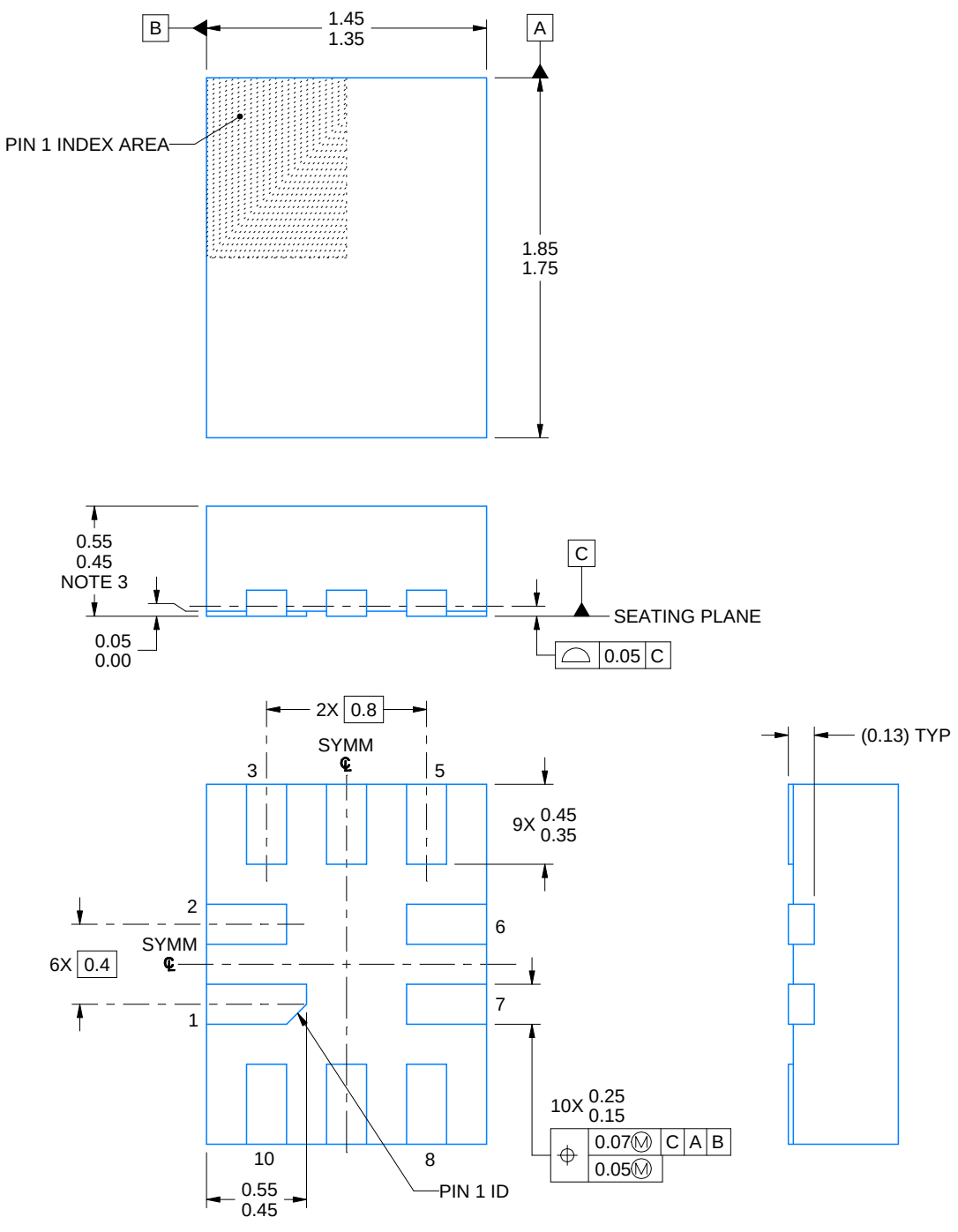
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB30EDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3USB30ERSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
TS3USB30ERSWR	UQFN	RSW	10	3000	184.0	184.0	19.0

PACKAGE OUTLINE

RSW0010A

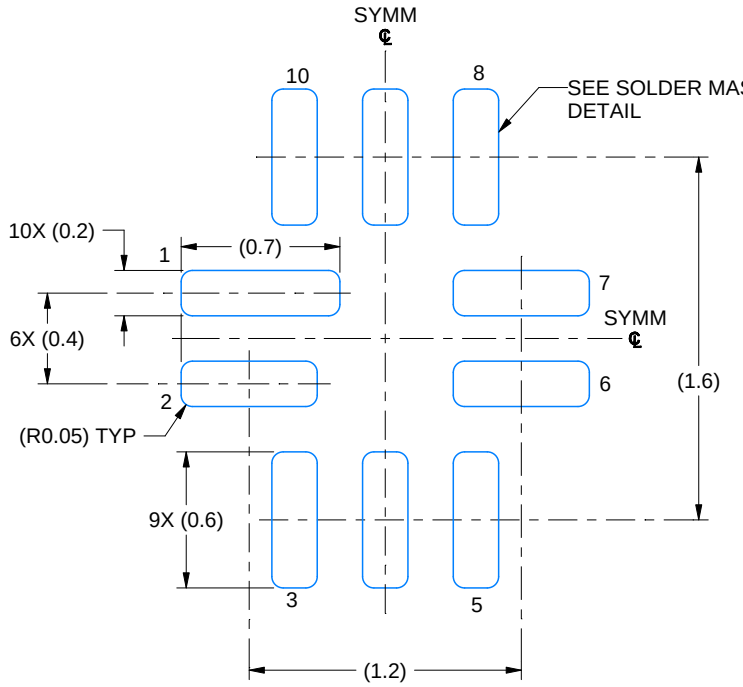
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

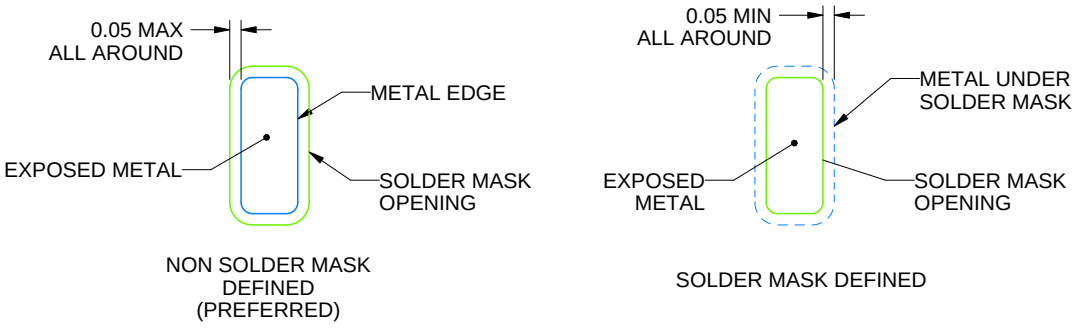


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

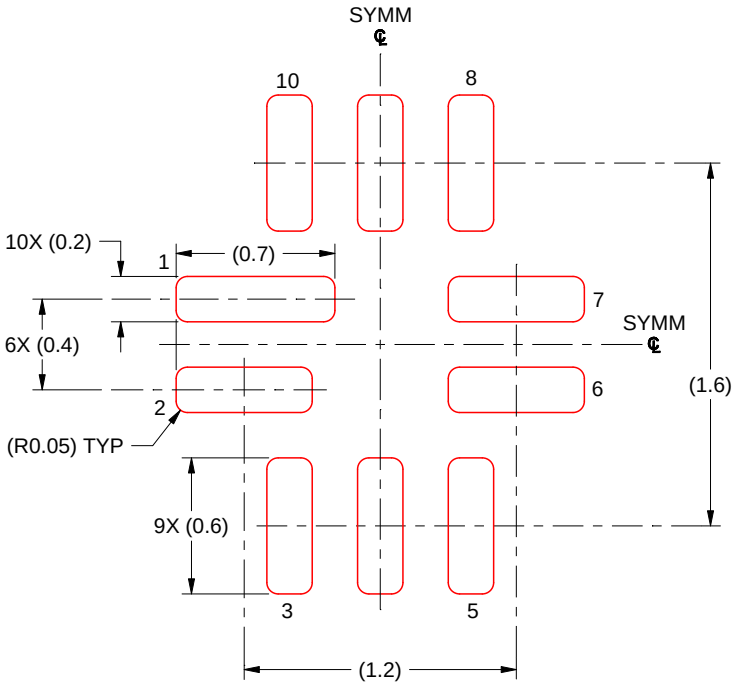


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

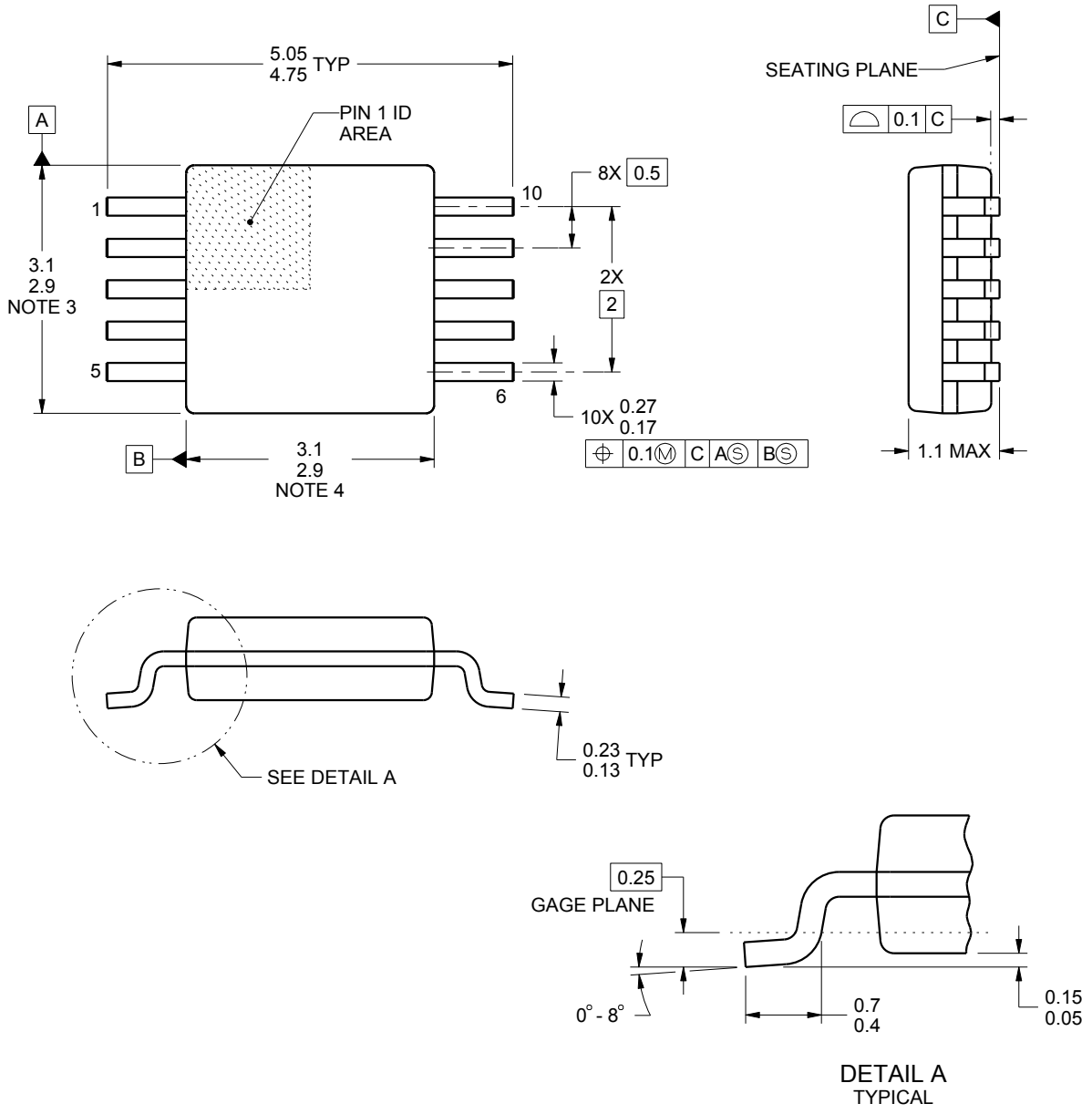
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

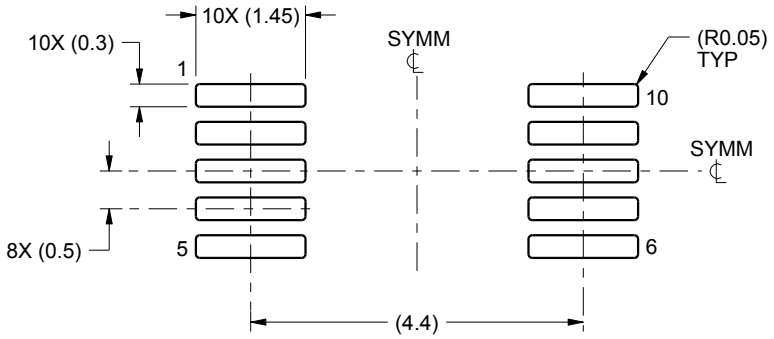
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

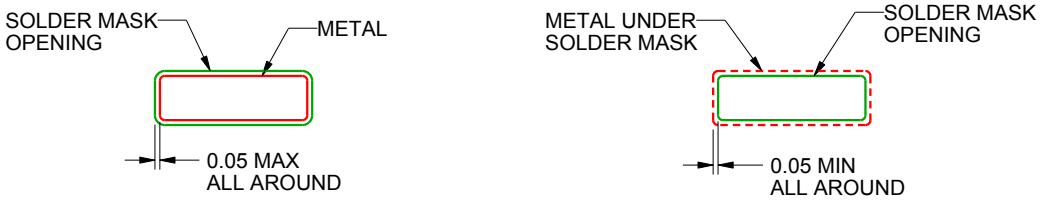


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

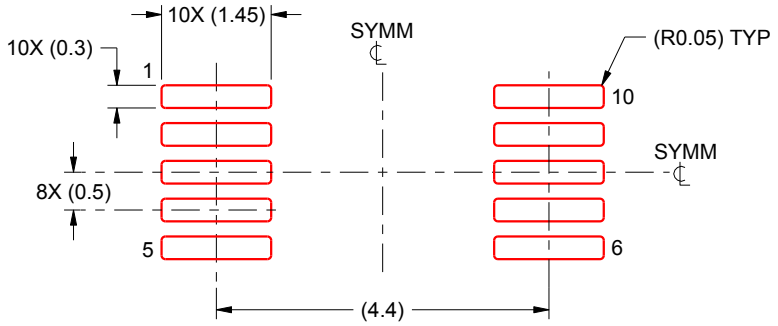


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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