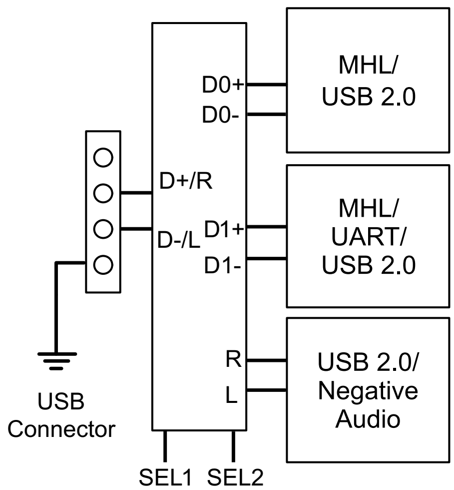
TS3USBA225 支持负信号且具有 1.8V 逻辑兼容性和省电模式的 USB 2.0 高速 (480Mbps) 音频开关

1 特性

- 2.7V 至 5.0V 的工作电源 (VCC)
- 高清链接 (MHL)/高速 USB (480Mbps) 开关：
  - V I/O 接受最高达 4.5V 的信号（与 VCC 无关）
  - 6.5Ω ON（典型值）
  - 3pF C_{ON}（典型值）
  - 1.9GHz 带宽 (-3dB)
- 音频开关：
  - 2.5Ω r_{ON}（典型值）
  - 支持低至 –1.8V 的负电源轨
  - 低总谐波失真 (THD)：< 0.05%
  - 内部分流电阻，用于减少喀哒声和噼啪声
- 1.8V 兼容控制输入（SEL1 和 SEL2）阈值
- 省电模式下可最大限度降低电流消耗（约 5μA）
- 掉电保护：V_{CC}= 0V 时所有 I/O 引脚呈高阻态
- 12 引脚四方扁平无引线 (QFN) 封装（2mm × 1.7mm，0.4mm 间距）
- 根据 JESD 22 测试得出的静电放电 (ESD) 性能
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 带电器件模型 (C101)

简化框图



2 应用

- 手机和智能电话
- 平板电脑
- 便携式仪表
- 数码相机
- 便携式导航器件 (GPS)
- USB 2.0、MIPI (CSI/DSI)、LVDS 开关

3 说明

TS3USBA225 是一款双通道单刀三掷 (SP3T) 多路复用器，可在全部 3 条差分通道中支持 USB 2.0 高速 (480Mbps) 信号。前两条高速差分通道还支持分辨率/视频帧速率高达 720p/60fps 和 1080i/30fps 的移动高清链接 (MHL) 信号传输。最后一条差分通道还可用作音频开关，允许模拟音频信号在负值区域摆动。该配置允许系统设计人员为音频数据和 USB 2.0/MHL 数据使用同一连接器。

TS3USBA225 的 V_{CC} 范围为 2.7V 至 5.0V，能够传输低至 –1.8V 的真正接地音频信号。该器件还支持省电模式，可在 SEL1 和 SEL2 控制输入为低电平时使能，从而最大限度地降低无信号传输时的电流消耗。另外，TS3USBA225 还在音频路径上 配有 内部分流电阻，用于减少在选择音频开关时可能听见的喀哒声和噼啪声。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3USBA225	UQFN (12)	2.00mm × 1.70mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

English Data Sheet: SCDS328

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

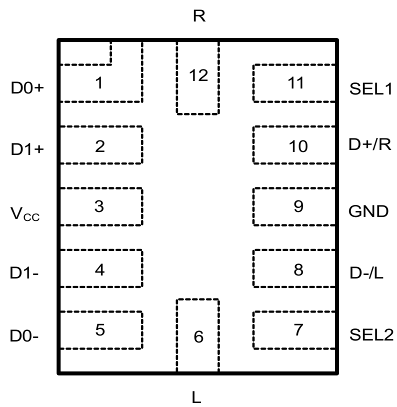
Changes from Revision B (July 2012) to Revision C	**Page**
• 已添加 *器件信息表*，*ESD 额定值表*，*热性能信息表*，*详细 说明部分*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分*	1
• 已更正印刷错误来对齐数据表信息。	1
• 已更改 "支持 -1.8V 至 VCC 的负电源轨"至"支持低至 –1.8V 的负电源轨" （特性部分）。	1
• Updated *Recommended Operating Conditions* table.	5
• Updated *Typical Characteristics* graphs.	9

Changes from Revision A (April 2012) to Revision B	**Page**
• 已更新应用框图。	1
• Updated MIN value in the Absolute Maximum Ratings table for V_R, V_L.	4
• Updated MIN value in the *Recommended Operating Conditions* table for V_R, V_L.	5

Changes from Original (October 2011) to Revision A	**Page**
• 已添加 MHL 规范至数据表。	1
• 已更新应用框图。	1
• Added MHL Eye Pattern graphics.	13

5 Pin Configuration and Functions

RUT Package
12-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D0+	1	I/O	MHL/USB/UART Data 1 (Differential +)
D1+	2	I/O	MHL/USB/UART Data 2 (Differential +)
V_{CC}	3	-	Power supply
D1–	4	I/O	MHL/USB/UART Data 2 (Differential –)
D0–	5	I/O	MHL/USB/UART Data 1 (Differential –)
L	6	I/O	USB-/Left Channel Audio
SEL2	7	I	Control Input Select Line 2. The default state for SEL2 is LOW.
D–/L	8	I/O	MHL/USB/UART/Audio Common Connector
GND	9	-	Ground
D+/R	10	I/O	MHL/USB/UART/Audio Common Connector
SEL1	11	I	Control Input Select Line 1. The default state for SEL1 is LOW.
R	12	I/O	USB+/Right Channel Audio

Function Table

SEL1	SEL2	V_{CC}	L,R	D0+, D0-	D1+, D1-	MODE
X	X	L	OFF	OFF	OFF	Hi-Z Mode
L	L	H	OFF	OFF	OFF	Power-Down Mode
L	H	H	OFF (1)	ON	OFF	MHL/USB Mode 1
H	L	H	ON	OFF	OFF	USB/Audio Mode
H	H	H	OFF (1)	OFF	ON	MHL/USB Mode 2

(1) 100 Ω shunt resistors are enabled in this state.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	6.0	V
V_{D0+}, V_{D0-}, V_{D1+}, V_{D1-}	High speed differential signal voltage		–0.3	4.6	V
V_R, V_L	Audio signal voltage		– 1.9	4.6	V
I_K	Analog port diode current	$V_{I/O+}$,$V_{I/O-}$ < 0	–50		mA
V_I	Digital input voltage (SEL1, SEL2)		–0.3	6.0	V
I_{IK}	Digital logic input clamp current(3)	V_I < 0	–50		
I_{CC}	Continuous current through VCC			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		2.7	5.0	V
V_{D0+}, V_{D0-}, V_{D1+}, V_{D1-}	High speed differential signal voltage range		0	4.5	V
V_R, V_L	Audio signal voltage range when not in power-down mode		–1.8	4.3 V or V_{CC} (1)	V
	Audio signal voltage range when in power-down mode		–1	1	
I_K	Analog port diode current	$V_{I/O+}$, $V_{I/O-}$ < 0	–50		mA
V_I	Digital input voltage range (SEL1, SEL2)		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) This rating is exclusive and the voltage on the pins must not exceed either 4.3 V or V_{CC}. E.g. if V_{CC} = 3.3 V the voltage on the pin must not exceed 3.3 V and if V_{CC} is = 5.0 V the voltage on the pin must not exceed 4.3 V.

6.4 Thermal Information

THERMAL METRIC (1)		TS3USBA225 RUT (UQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL/USB SWITCH							
r_{on}	ON-state resistance	V_{CC} = 3.0 V	$V_{I/O+,I/O-}$ = 0.4 V, I_{ON} = 15 mA		6.5	7.5	Ω
Δr_{on}	ON-state resistance match between channels	V_{CC} = 3.0 V	$V_{I/O+,I/O-}$ = 1.7 V, I_{ON} = 15 mA		0.1		Ω
$r_{on\ (flat)}$	ON-state resistance flatness	V_{CC} = 3.0 V	$V_{I/O+,I/O-}$ = 0 to 1.7 V, I_{ON} = 15 mA		0.5		Ω
I_{OZ}	OFF leakage current	V_{CC} = 3.6 V	Switch OFF , $V_{I/O+,I/O-}$ = 0 to 3.6 V, $V_{D+/R,\ D-/L}$ = 0 V			1	µA
USB/AUDIO SWITCH							
r_{on}	ON-state resistance	V_{CC} = 3.0 V	SEL1 = High, SEL2 = Low, $V_{L/R}$ = –1.8 V, 0 V, 0.7 V, I_{ON} = –26 mA		2.5	3.5	Ω
Δr_{on}	ON-state resistance match between channels	V_{CC} = 3.0 V	SEL1 = High, SEL2 = Low, $V_{L/R}$ = 0.7 V, I_{ON} = –26 mA		0.1		Ω
$r_{on\ (flat)}$	ON-state resistance flatness	V_{CC} = 3.0 V	SEL1 = High, SEL2 = Low, $V_{L/R}$ = –1.8 V, 0 V, 0.7 V, I_{ON} = –26 mA		0.1		Ω
r_{SHUNT}	Shunt resistance	V_{CC} = 2.7 V to 5.0 V	Switch OFF, $V_{L/R}$ = 0.7 V, I_{SHUNT} = 10 mA		100	200	Ω
DIGITAL CONTROL INPUTS (SEL1, SEL2)							
V_{IH}	Input logic high	V_{CC} = 3.3 V to 5.0 V		1.3			V
V_{IL}	Input logic low	V_{CC} = 2.7 V to 3.3 V				0.25	V
		V_{CC} = 3.3 V to 5.0 V				0.4	
I_{IN}	Input leakage current	V_{CC} = 2.7 V to 5.0 V	V_{IN} = 5.0 V			±3	µA
			V_{IN} = 0 V			±0.1	
r_{PD1}, r_{PD2}	Internal pulldown resistance	V_{CC} = 2.7 V to 5.0 V			3		MΩ

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL/USB SWITCH							
t_{pd}	Propagation Delay	V_{CC} = 2.7 V or 3.3 V			0.25		ns
t_{ON}	Turn-on time	RL = 50 Ω, CL = 35 pF	V_{CC} = 2.7 V			60	ns
t_{OFF}	Turn-off time	RL = 50 Ω, CL = 35 pF	V_{CC} = 2.7 V			20	ns
$t_{SK(O)}$	Channel-to-channel skew	V_{CC} = 2.7 V or 3.3 V		15			ps
$t_{SK(P)}$	Skew of opposite transitions of same output	V_{CC} = 2.7 V or 3.3 V		15			ps
$C_{I/O+(OFF)}$ $C_{I/O-(OFF)}$	OFF capacitance	V_{CC} = 2.7 V or 3.3 V, $V_{D0+/D0-}$ =0 or 3.3 V	Switch OFF		1		pF
$C_{I/O+(ON)}$ $C_{I/O-(ON)}$	ON capacitance	V_{CC} = 2.7 V or 3.3 V, $V_{D0+/D0-}$ = 0 or 3.3 V	Switch ON		3		pF
C_I	Digital input capacitance	V_{CC} = 2.7 V or 3.3 V, V_I = 0 or 3.3 V			2.5		pF
BW	Bandwidth	V_{CC} = 2.7 V or 3.3 V, R_L = 50 Ω	Switch ON		1.9		GHz
O_{ISO}	OFF Isolation	V_{CC} = 2.7 V or 3.3 V, R_L = 50 Ω, f = 240 MHz	Switch OFF		-35		dB
X_{TALK}	Crosstalk	V_{CC} = 2.5 V or 3.3 V, R_L = 50 Ω, f = 240 MHz	Switch ON		-45		dB
USB/AUDIO SWITCH							
t_{ON}	Turn-on time	R_L = 50 Ω, C_L = 35 pF	V_{CC} = 2.7 V		40		µs
t_{OFF}	Turn-off time	R_L = 50 Ω, C_L = 35 pF	V_{CC} = 2.7 V		15		ns
$C_{L(OFF)}$, $C_{R(OFF)}$	L , R OFF capacitance	V_{CC} = 2.7 V to 4.5 V, f = 20 kHz	Switch OFF		1.0		pF
$C_{L(ON)}$, $C_{R(ON)}$	L, R ON capacitance	V_{CC} = 2.7 V to 4.5 V, f = 20 kHz	Switch ON		3.5		pF
O_{ISO}	OFF Isolation	V_{CC} = 3.3 V, R_L = 50 Ω, f = 20 kHz	Switch OFF		-85		dB
X_{TALK}	Crosstalk	V_{CC} = 3.3 V, R_L = 50 Ω, f = 20 kHz	Switch ON		-95		dB
THD	Total harmonic distortion	V_{CC} = 3.3 V, SEL1 = High, SEL2 = Low, f = 20 Hz to 20 kHz, R_L = 600 Ω, V_{IN} = 2 Vpp	Switch ON		0.05%		
SUPPLY							
V_{CC}	Power supply voltage			2.7		5.0	V
I_{CC}	Positive supply current	V_{CC} = 2.7 V, 3.6 V, 5.0 V V_{IN}= V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF			25	50	µA
$I_{CC, PD}$	Positive supply current (Power-Down Mode)	V_{CC} = 2.7 V, 3.6 V, 5.0 V, $V_{I/O}$ = 0 V, SEL1 and SEL2 = Low			3	5	µA
PSRR	Power Supply Rejection Ratio	V_{CC} = 2.7 V, 3.6 V, 5.0 V V_{IN} = V_{CC} +/- 200 mVpp R_L = 50 Ω		-60			dB
I_{OFF}	Power off leakage current	V_{CC} = 0 V, D+/R, D-/L, D0+, D0-, D1+, D1-, L, V_{IN} = 0 to 4.5 V			±0.1		µA

6.7 Typical Characteristics

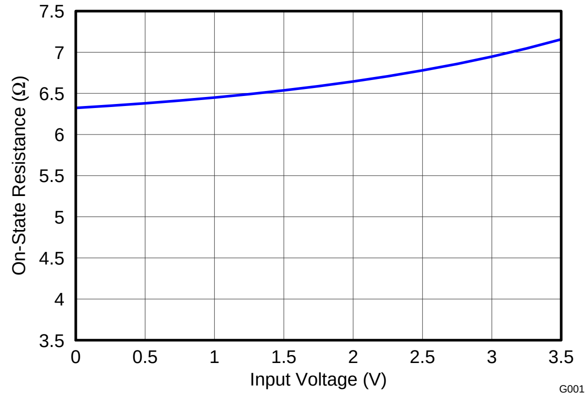


Figure 1. ON Resistance vs V_I for MHL/USB Switch

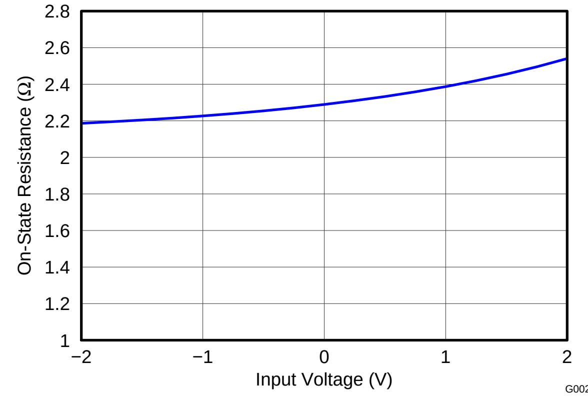


Figure 2. ON Resistance vs V_I for USB/Audio Switch

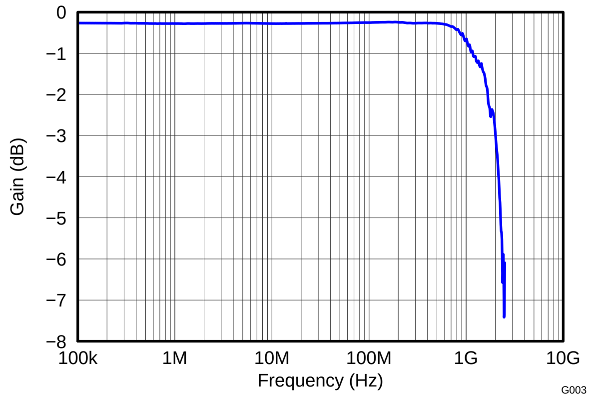


Figure 3. Gain vs Frequency for MHL/USB Switch

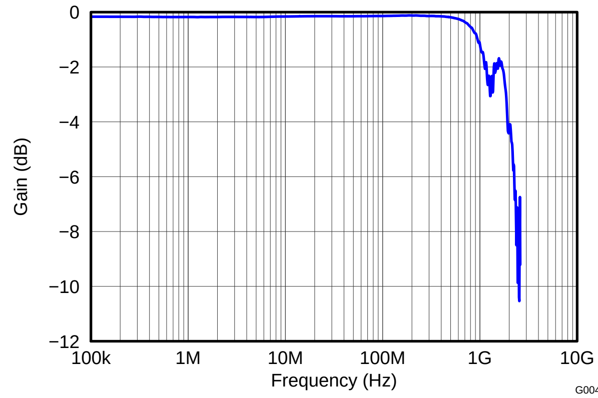


Figure 4. Gain vs Frequency for USB/Audio Switch

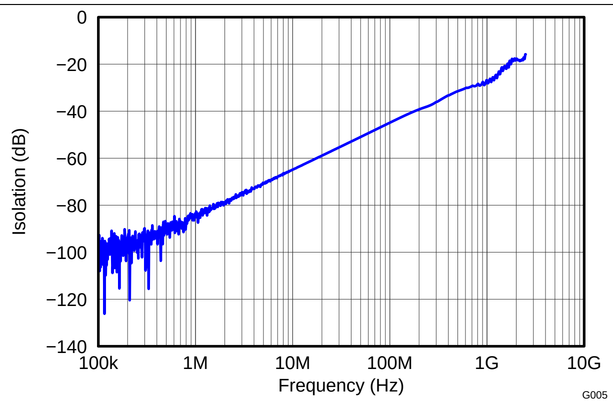


Figure 5. Off Isolation vs Frequency for MHL/USB Switch

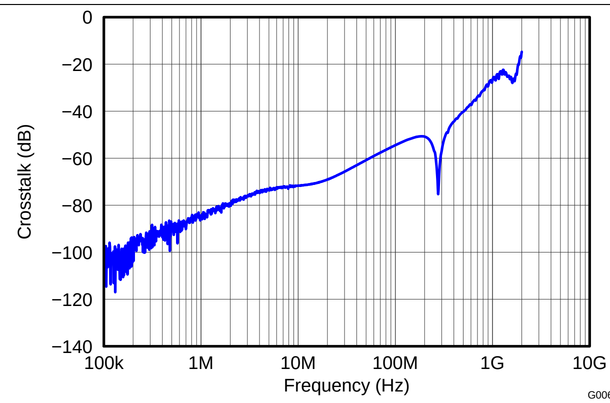


Figure 6. Cross Talk vs Frequency for MHL/USB Switch

Typical Characteristics (continued)

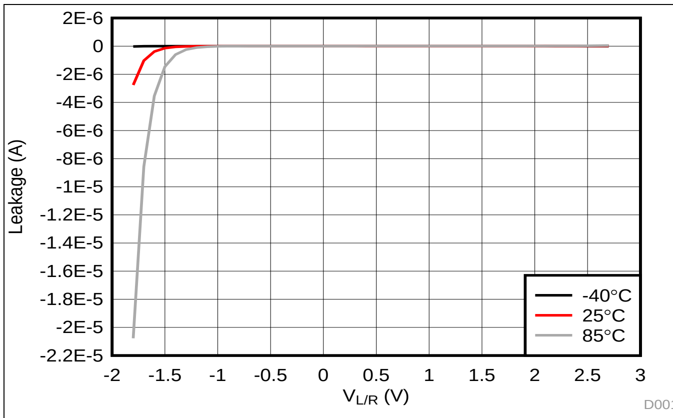


Figure 7. I_{ON}, V_{CC} = 2.7 V

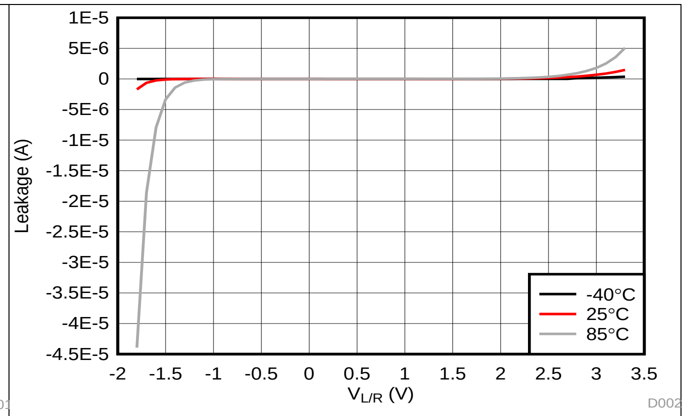


Figure 8. I_{ON}, V_{CC} = 3.3 V

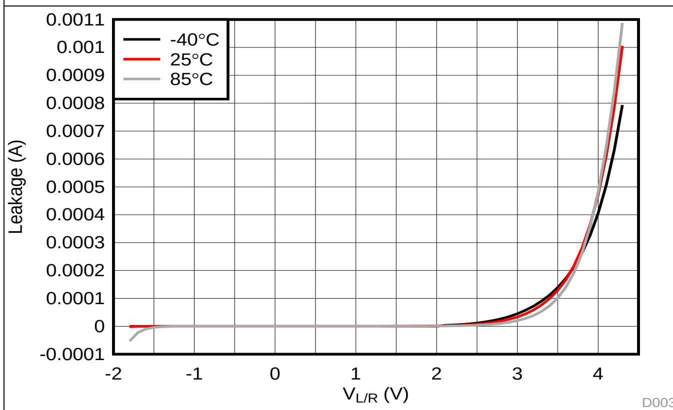


Figure 9. I_{ON}, V_{CC} = 5.0 V

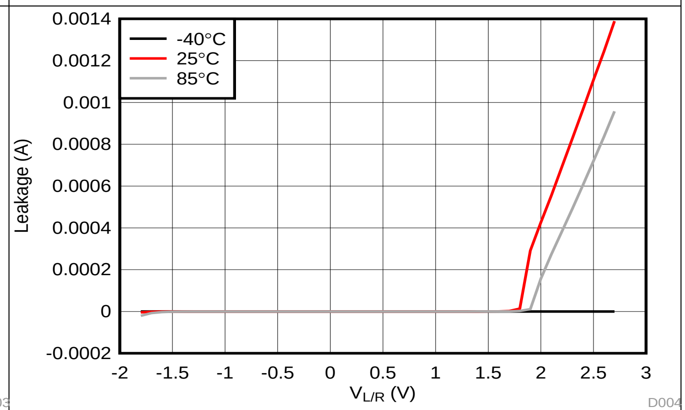


Figure 10. I_{OFF}, V_{CC} = 2.7 V

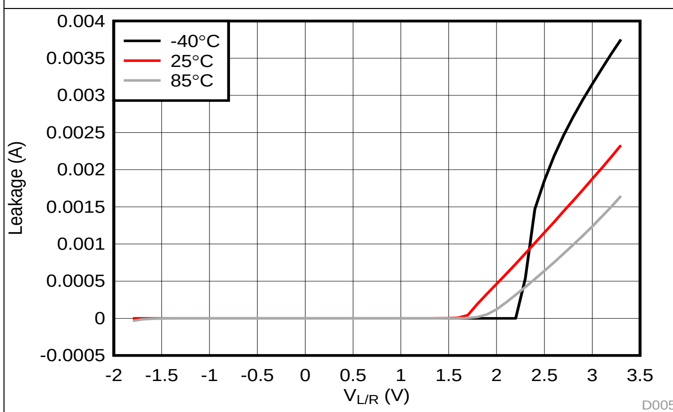


Figure 11. I_{OFF}, V_{CC} = 3.3 V

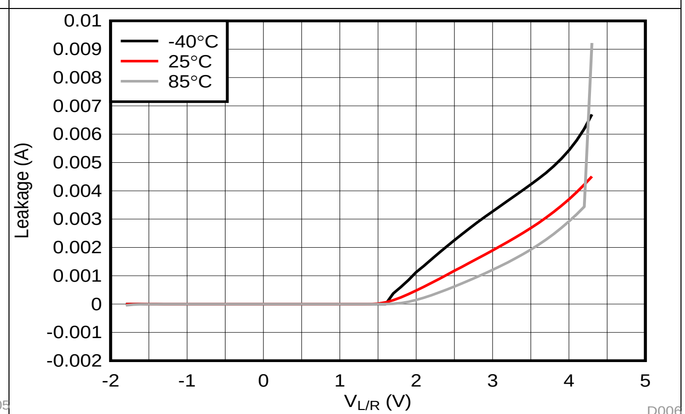


Figure 12. I_{OFF}, V_{CC} = 5.0 V

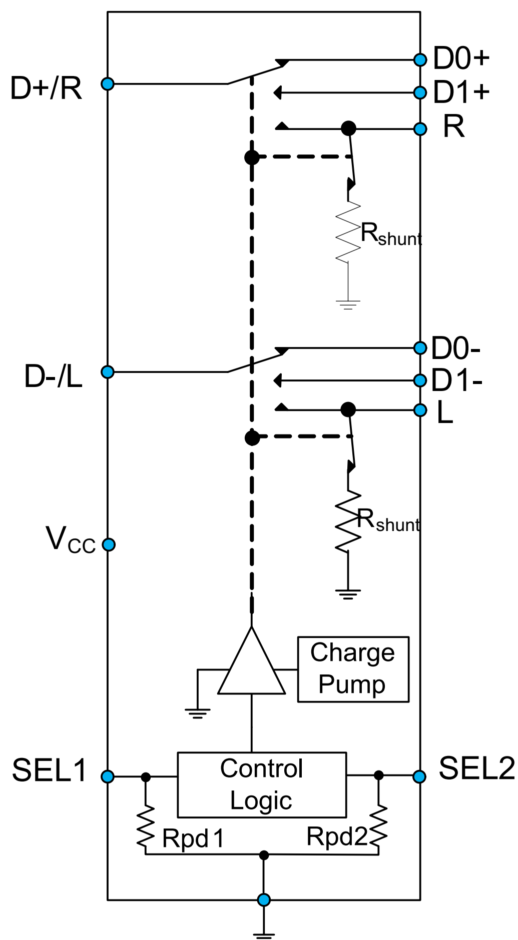
7 Detailed Description

7.1 Overview

The TS3USBA225 is a 2-channel single-pole triple-throw (SP3T) multiplexer that supports USB 2.0 High-Speed (480 Mbps) signals in all 3 differential channels. The first two high-speed differential channels also support Mobile High Definition Link (MHL) signaling with video resolution and frame rates up to 720p, 60 fps and 1080i, 30 fps. The remaining differential channel can also be used as an audio switch that is designed to allow analog audio signals to swing negatively. This configuration allows the system designer to use a common connector for audio and USB 2.0 or MHL data.

The TS3USBA225 has a V_{CC} range of 2.7 V to 5.0 V with the capability to pass true-ground audio signals down to –1.8 V. The device also supports a power-down mode that can be enabled when both SEL controls are low to minimize current consumption when no signal is transmitting. The TS3USBA225 also features internal shunt resistors on the audio path to reduce clicks and pops that may be heard when the audio switches are selected.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Click and Pop Reduction

The shunt resistors in the TS3USBA225 automatically discharge any capacitance at the L and R terminals when they are not connected to the common D-/L and D+/R paths. This reduces the audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

Feature Description (continued)

7.3.2 Negative Signal Swing Capability

The TS3USBA225 has an analog audio path L and R that can support negative signals that pass below ground without distortion. These analog switches operate from –1.8 V to 4.3 V.

7.4 Device Functional Modes

7.4.1 High Impedance (Hi-Z) Mode

The TS3USBA225 has a Hi-Z mode that places the device's signal paths in a high impedance state when there is no power supplied to the TS3USBA225 V_{CC} pin. This mode will isolate the signal bus in a powered off situation so that it may not interfere with other devices that maybe sharing the bus.

7.4.1.1 Power-Down Mode

The TS3USBA225 has a power-down mode that reduces the power consumption to 3 µA when the device is not in use. To put the device in power-down mode and disable the switch, the SEL1 and SEL2 pins must be supplied with a logic low signal.

7.4.2 Device Functional Modes

Table 1 is the function table for the TS3USBA225.

Table 1. Function Table

SEL1	SEL2	V_{CC}	L,R	D0+, D0-	D1+, D1-	MODE
X	X	L	OFF	OFF	OFF	Hi-Z Mode
L	L	H	OFF	OFF	OFF	Power-Down Mode
L	H	H	OFF (1)	ON	OFF	MHL/USB Mode 1
H	L	H	ON	OFF	OFF	USB/Audio Mode
H	H	H	OFF (1)	OFF	ON	MHL/USB Mode 2

(1) 100 Ω shunt resistors are enabled in this state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TS3USBA225 is typically used to route signals from one USB connector to multiple signal paths in a system including an analog audio/negative signal path. All signal paths through the device are unbuffered bidirectional path which can represented by perfect 0 Ω impedance wire in an ideal case. All signal paths can handle USB 2.0 signals but the L and R paths are the only paths that can support a negative signal.

8.2 Typical Application

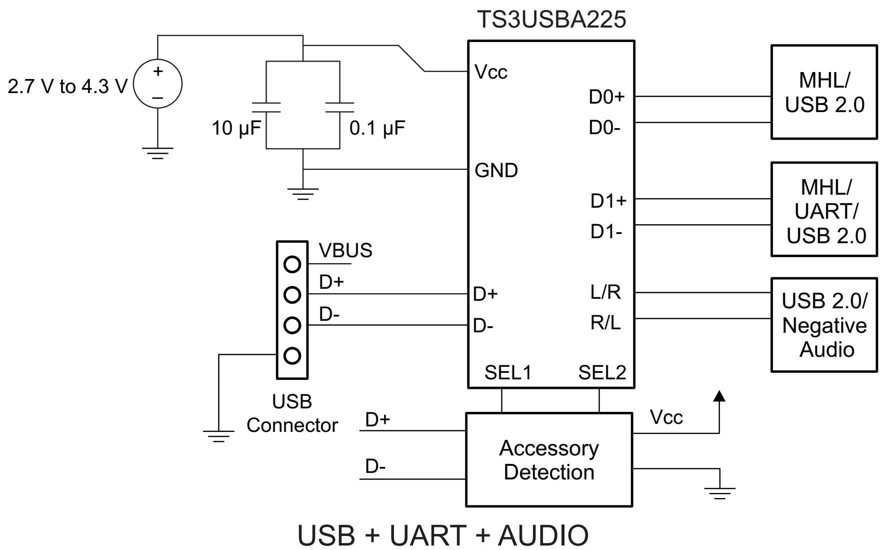


Figure 13. Application Block Diagram

8.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed.

TI recommends that the digital control pins SEL1 and SEL2 be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating logic pin.

8.2.2 Detailed Design Procedure

The TS3USB221 can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50 Ω resistor to prevent signal reflections back into the device.

Typical Application (continued)

8.2.3 Application Curves

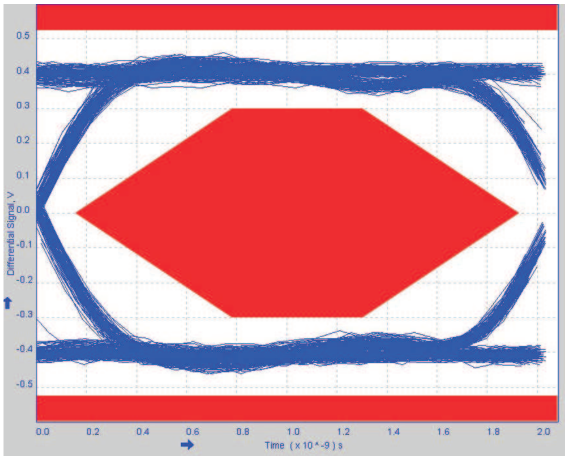


Figure 14. Eye Pattern: 480-Mbps USB 2.0 Eye Pattern (No Switch)

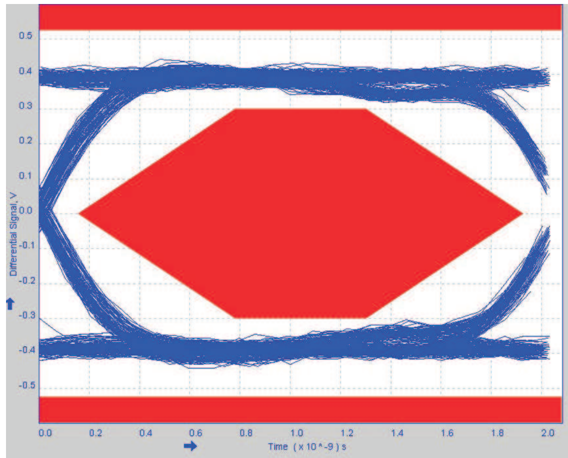


Figure 15. Eye Pattern: 480-Mbps USB 2.0 Eye Pattern for USB Switch

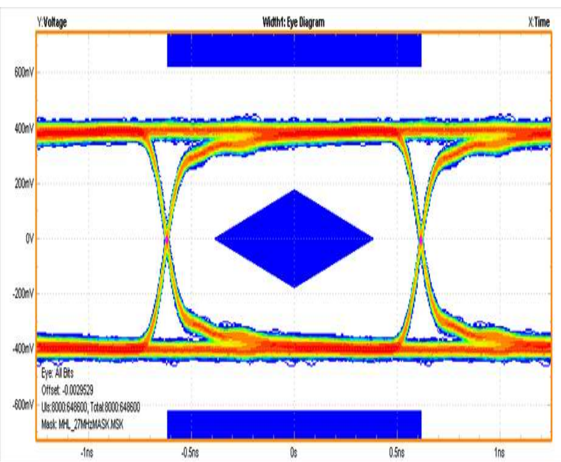


Figure 16. MHL Eye Pattern: 480p 60 fps (No Switch)

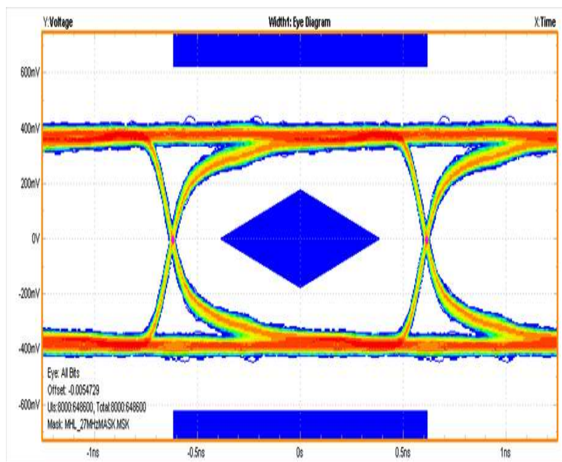


Figure 17. MHL Eye Pattern: 480p 60 fps (With Switch)

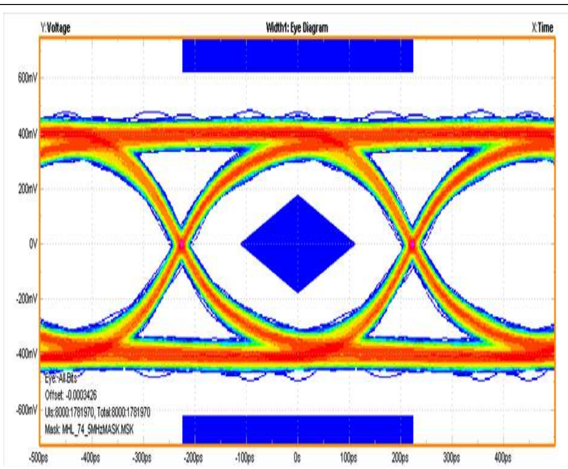


Figure 18. MHL Eye Pattern: 720p 60 fps, 1080i 30fps (No Switch)

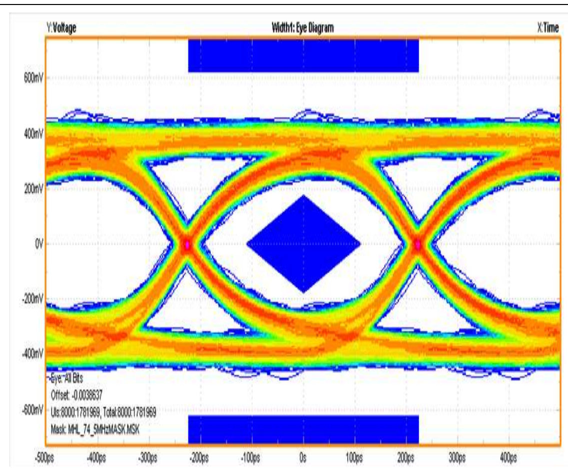


Figure 19. MHL Eye Pattern: 720p 60 fps, 1080i 30fps (With Switch)

9 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out low frequency noise to provide better load regulation across the frequency spectrum.

10 Layout

10.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+/D– traces.

The high-speed D+/D– traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Take precaution when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

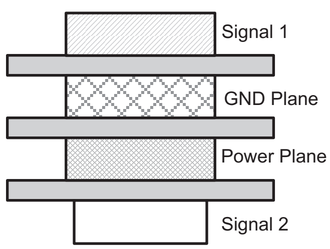


Figure 20. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

10.2 Layout Example

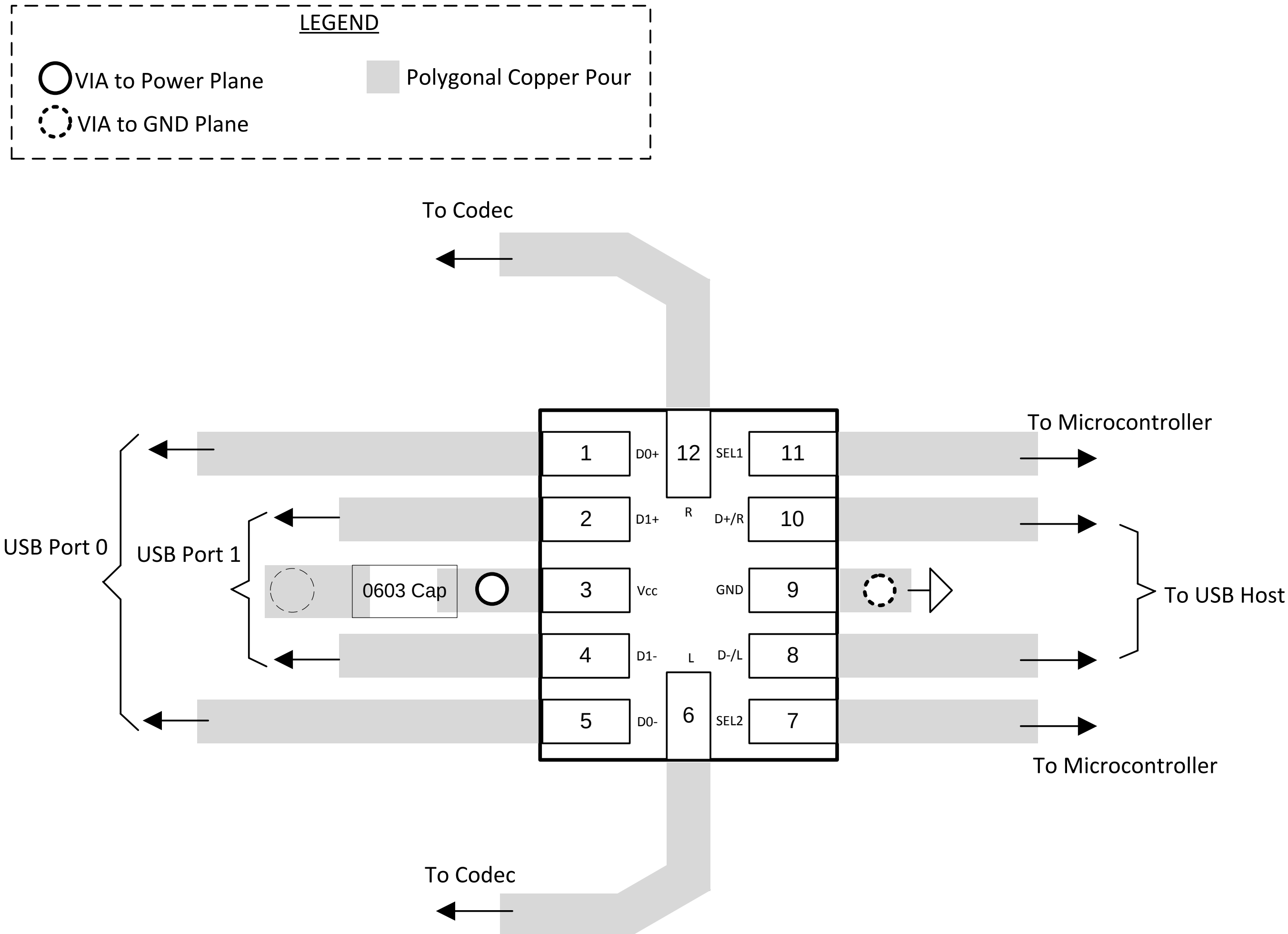


Figure 21. Layout Schematic

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USBA225RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(LQ7, LQR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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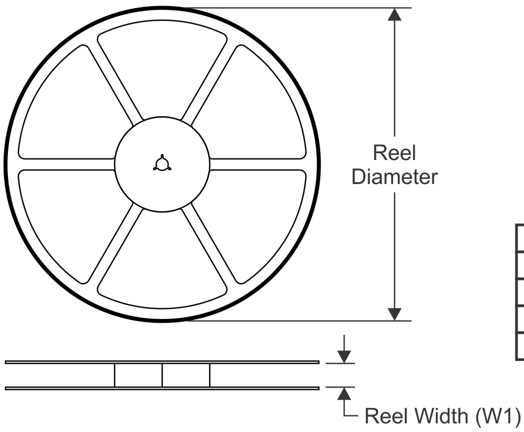
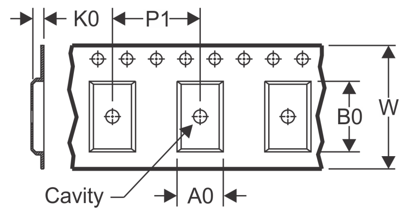
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

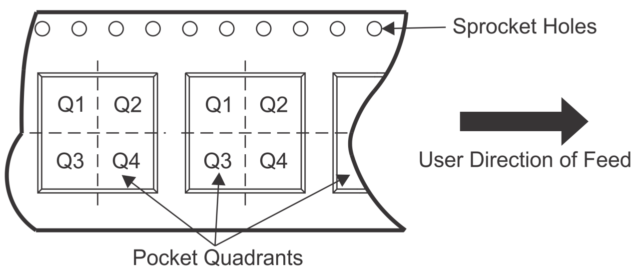


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

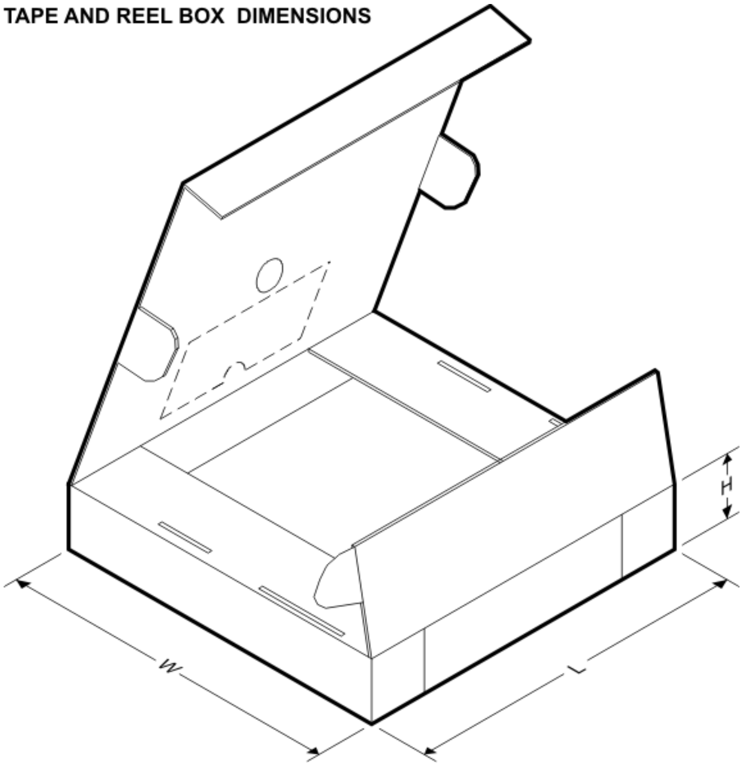
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

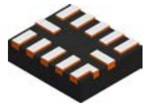
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USBA225RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TS3USBA225RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

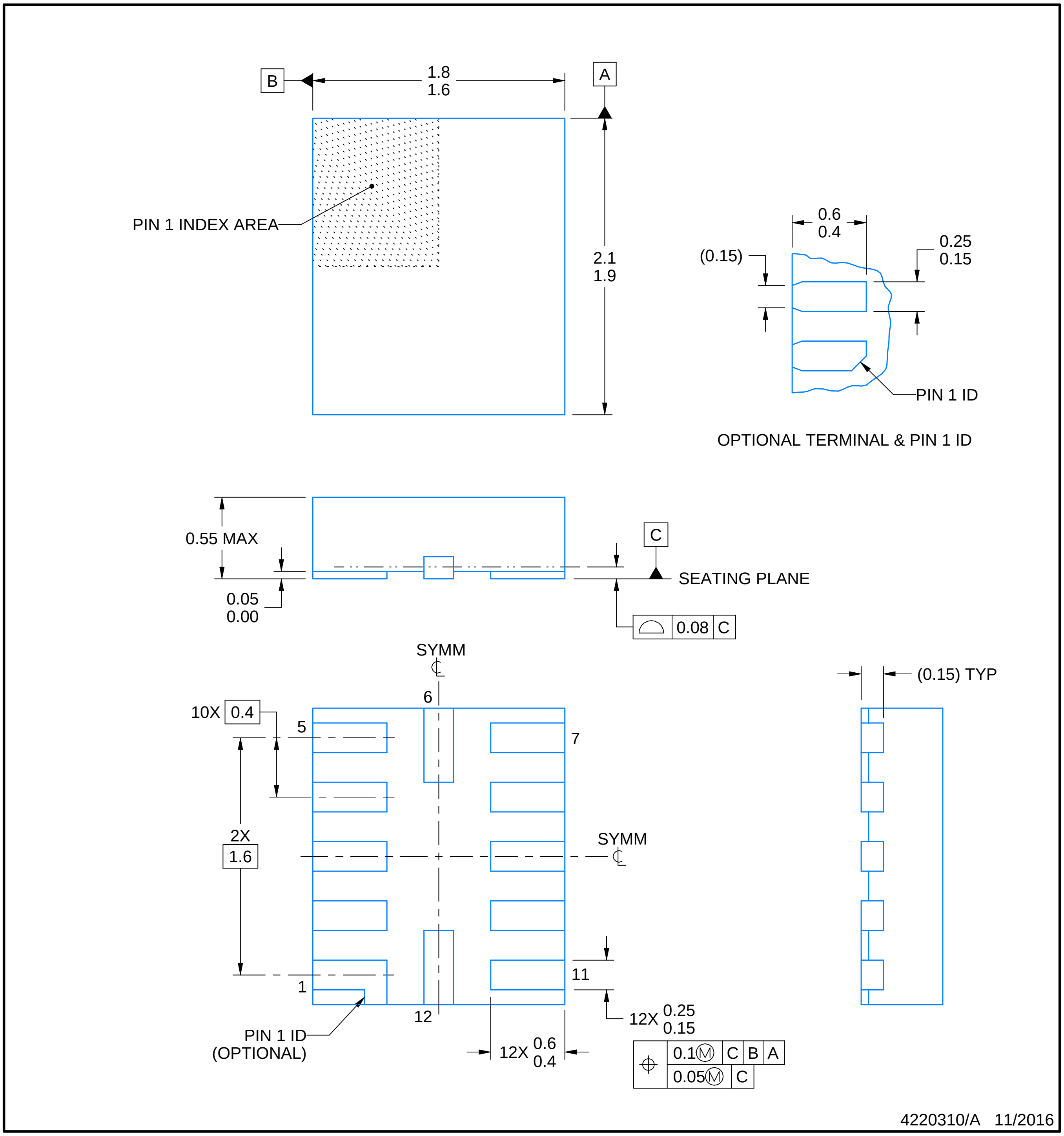
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USBA225RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TS3USBA225RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0



PACKAGE OUTLINE

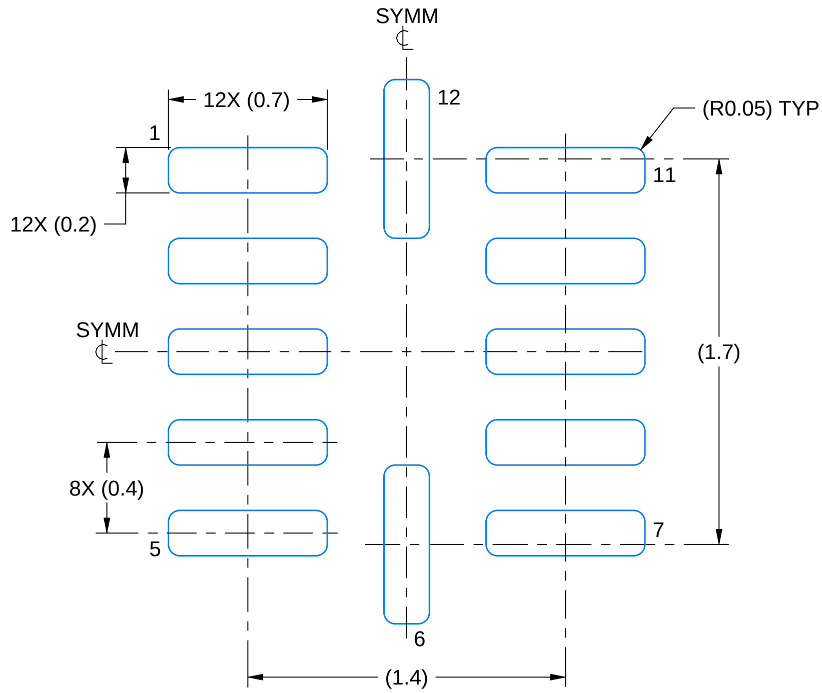
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

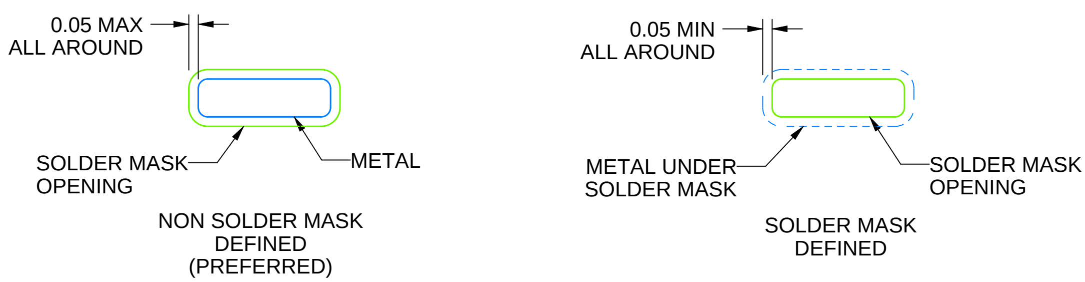


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

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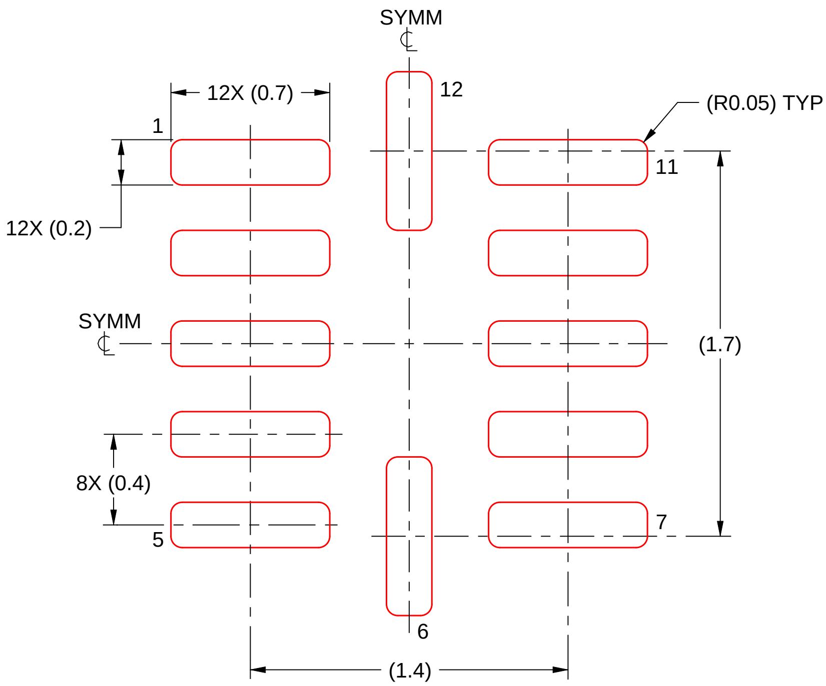
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.