TS5A23166 0.9Ω 双 SPST 模拟开关 5V 和 3.3V 双通道模拟开关

1 特性

- 在断电模式中提供了隔离，V_+ = 0
- 低导通电阻 (0.9Ω)
- 控制输入可承受 5.5V 电压
- 低电荷注入
- 出色的导通状态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- 便携式仪表
- 音频和视频信号路由
- 低压数据采集系统
- 通信电路
- 调制解调器
- 硬盘
- 计算机外设
- 无线终端和外设

3 说明

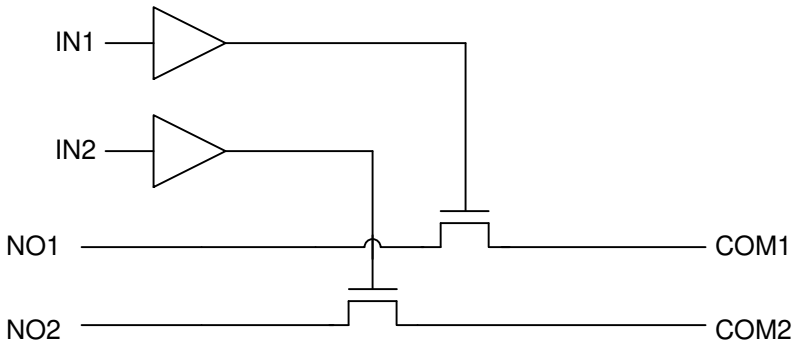
TS5A23166 器件是一款双单刀单掷 (SPST) 模拟开关，工作电压范围为 1.65V 至 5.5V。TS5A23166 器件具有较低的通态电阻和出色的通道间通态电阻匹配功能。TS5A23166 器件具有出色的总谐波失真 (THD) 性能和极低的功耗。这些 特性 再加上低功耗性能，使得这款器件适合于便携式音频 应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A23166	超薄小外形尺寸封装 (VSSOP)(8)	2.30mm × 2.00mm
	DSBGA (8)	1.91mm × 0.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (March 2018) to Revision J — **Page**

- Changed the *Thermal Information* table ... 4

Changes from Revision H (May 2015) to Revision I — **Page**

- Added Note: "Not tested in production" to leakage current at 25°C in the *Electrical Characteristics* tables ... 4

Changes from Revision G (February 2013) to Revision H — **Page**

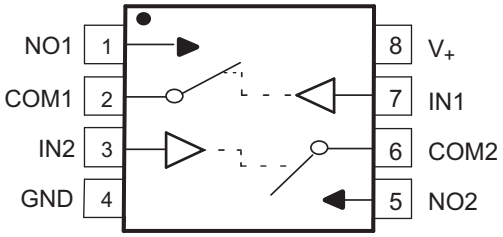
- 添加了*引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 将文档更新为新的 TI 数据表格式 - 无规格更改。 ... 1
- 删除了*订购信息* 表。 ... 1

Changes from Revision F (September 2012) to Revision G — **Page**

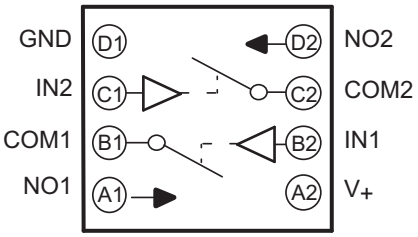
- Changed pin numbers for YZT or YZP package pinout. ... 3

5 Pin Configuration and Functions

DCU Package
8-Pin VSSOP
Top View



YZT or YZP Package
8-Pin DSBGA
Bottom View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP NO.	DSBGA NO.		
COM1	2	B1	I/O	Common port for switch 1
COM2	6	C2	I/O	Common port for switch 2
GND	4	D1	GND	Ground
IN1	7	B2	I	Active-high control pin connecting NO1 to COM1.
IN2	3	C1	I	Active-high control pin connecting NO2 to COM2.
NO1	1	A1	I/O	Normally open switch path 1
NO2	5	D2	I/O	Normally open switch path 2
V+	8	A2	PWR	Power supply pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	ON-state switch current	V_{NO}, V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)	V_{NO}, V_{COM} = 0 to V_+	–400	400	mA
V_I	Digital input voltage(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	V_+	V
V_+	Supply voltage	1.65	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TS5A23166			UNIT
		DCU (VSSOP)	YZP (DSBGA)	YZT (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.2	99.9	99.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.6	1.0	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	27.8	27.8	°C/W
φ_{JT}	Junction-to-top characterization parameter	7.1	0.4	0.5	°C/W
φ_{JB}	Junction-to-board characterization parameter	91.1	27.8	27.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.9	1.1	Ω
				Full				1.2	
r_{on}	ON-state resistance	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	4.5 V		0.2		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C			0.15	0.25	
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see Figure 12	25°C	5.5 V	0 V	4	20 (2)	nA
				Full		–150		150	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–10	0.2	10 (2)	µA
				Full		–50		50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Not tested in production.

Electrical Characteristics: 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, see Figure 12	25°C	5.5 V	0 V	4	20(2)	nA
				Full		–150		150	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 5.5 V, V_{NO} = 5.5 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–10	0.2	10(2)	µA
				Full		–50		50	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	5.5 V	–5	0.4	5(2)	nA
				Full		–50		50	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	5.5 V	–5	0.4	5(2)	nA
				Full		–50		50	
Digital Control Inputs (IN1, IN2)(3)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	5 V		6		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		35.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		35.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	5 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	5 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	5 V		0.005%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	µA
				Full				1	

(3) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Electrical Characteristics: 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C	3 V		0.04	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA	Switch ON, see Figure 11	25°C	3 V		0.3		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, see Figure 11	25°C			0.15	0.25	
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see Figure 12	25°C	3.6 V	–5	0.5	5(2)	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–5	0.1	5(2)	μA
				Full		–25		25	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see Figure 12	25°C	3.6 V	–5	0.5	5(2)	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–5	0.1	5(2)	μA
				Full		–25		25	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	3.6 V	–2	0.3	2(2)	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	3.6 V	–2	0.3	2(2)	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)(3)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Not tested in production.
(3) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics: 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	5 V		6		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		36		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	3.3 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	3.3 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	3.3 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	3.3 V		0.01%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	μA
				Full				0.3	

6.7 Electrical Characteristics: 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
r_{on}	ON-state resistance	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		0.04	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C	2.3 V		0.7		Ω
		V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 11	25°C			0.4	0.6	
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, see Figure 12	25°C	2.7 V	–5	0.3	5(2)	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–2	0.05	2(2)	μA
				Full		–15		15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2) Not tested in production.

Electrical Characteristics: 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 2.3 V, V_{COM} = 0.5 V, or V_{NO} = 0.5 V, V_{COM} = 2.3 V,	Switch OFF, see Figure 12	25°C	2.7 V	–5	0.3	5(2)	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 2.7 V, V_{NO} = 2.7 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–2	0.05	2(2)	µA
				Full		–15		15	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	2.7 V	–2	0.3	2(2)	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.3 V, V_{NO} = Open,	Switch ON, see Figure 13	25°C	2.7 V	–2	0.3	2(2)	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	2.5 V		4		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	2.5 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	2.5 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	2.5 V		0.02%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	µA
				Full				0.25	

6.8 Electrical Characteristics: 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 11	25°C	1.65 V		4.2	25	Ω
				Full				30	
r_{on}	ON-state resistance	V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 11	25°C	1.65 V		1.6	3.9	Ω
				Full				4	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 11	25°C	1.65 V		0.04	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 11	25°C	1.65 V		2.8		Ω
		V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 11	25°C			4.1	22	
				Full				27	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, see Figure 12	25°C	1.95 V	–5	0.3	5(2)	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–2	0.05	2(2)	µA
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 1.65 V, V_{COM} = 0.3 V, or V_{NO} = 0.3 V, V_{COM} = 1.65 V,	Switch OFF, see Figure 12	25°C	1.95 V	–5	0.3	5(2)	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 1.95 V, V_{NO} = 1.95 V to 0,	Switch OFF, see Figure 12	25°C	0 V	–2	0.05	(2)2	µA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 13	25°C	1.95 V	–2	0.3	2(2)	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NO} = Open, V_{COM} = 0.3 V, or V_{NO} = Open, V_{COM} = 1.65 V,	Switch ON, see Figure 13	25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	µA
				Full		–20		20	
Dynamic									
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 19	25°C	1.8 V		2		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		36.5		pF

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
(2) Not tested in production.

Electrical Characteristics: 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 14	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	1.8 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 20	25°C	1.8 V		0.055%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	μA
				Full				0.15	

6.9 Switching Characteristics: 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, see Figure 15	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.10 Switching Characteristics: 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, see Figure 15	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1		10	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.11 Switching Characteristics: 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.5 V	4.5	8	12.5	ns
				Full	2.3 V to 2.7 V	3		15	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.12 Switching Characteristics: 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.13 Typical Characteristics

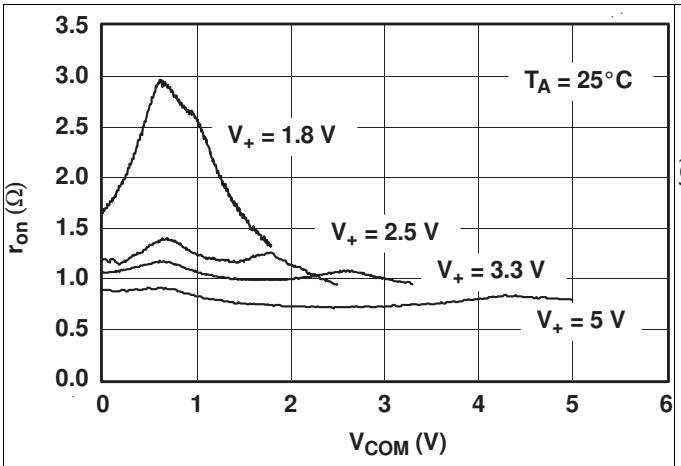


Figure 1. r_{on} vs V_{COM}

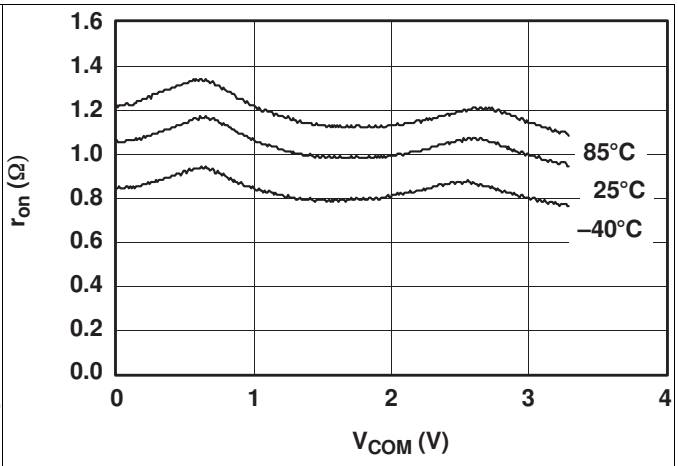


Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

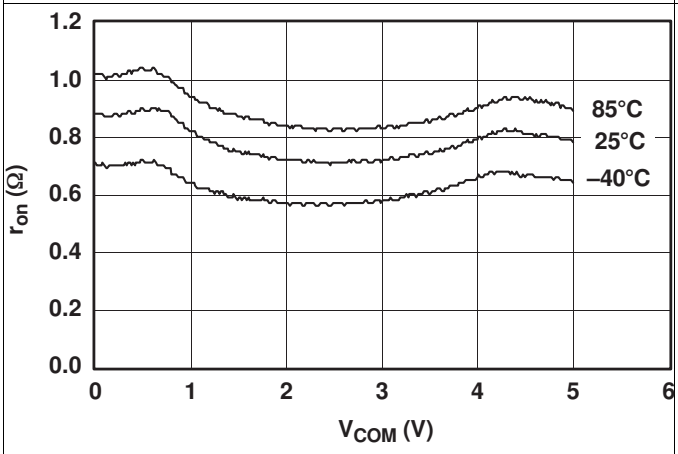


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

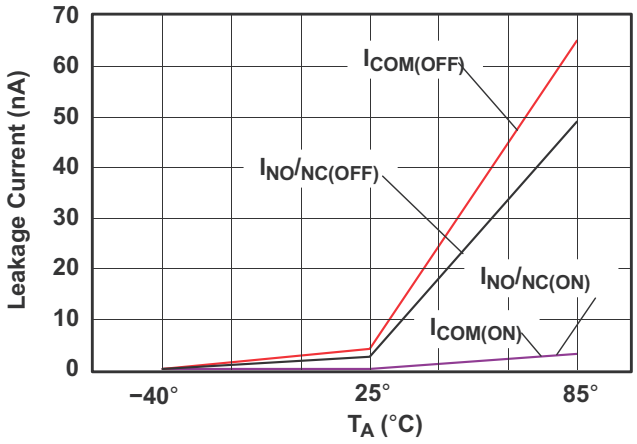


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

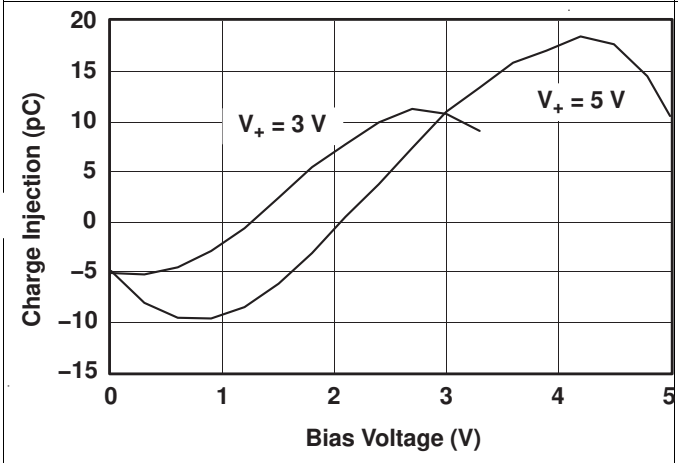


Figure 5. Charge Injection (Q_C) vs V_{COM}

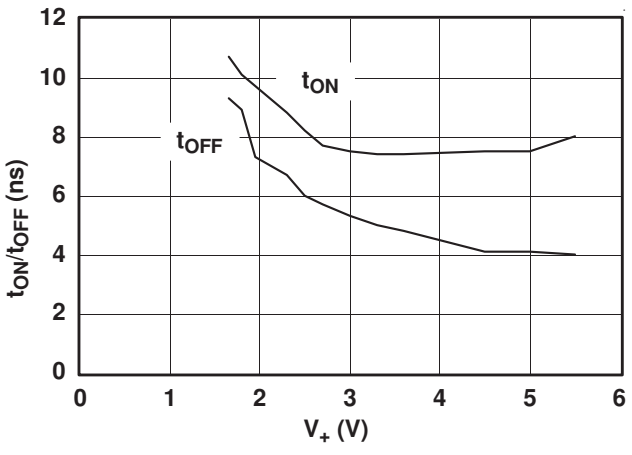


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

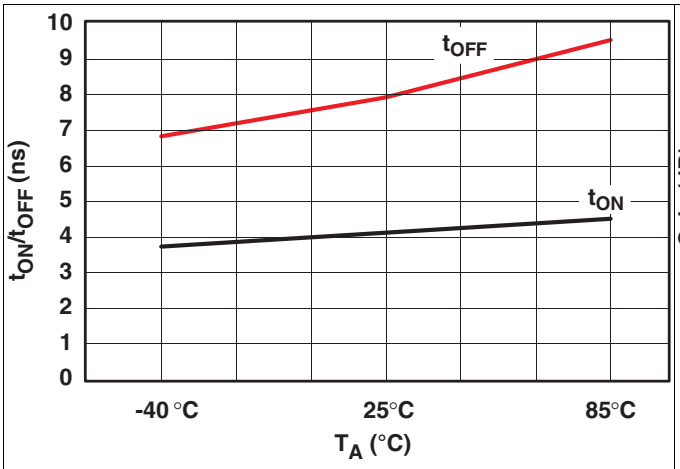


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

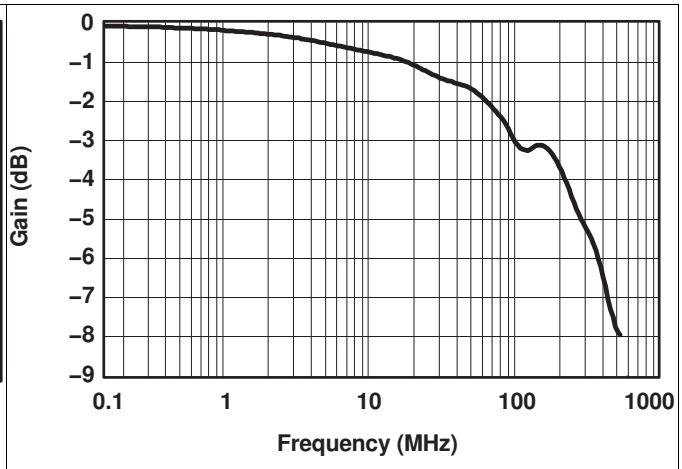


Figure 8. Bandwidth (V_+ = 5 V)

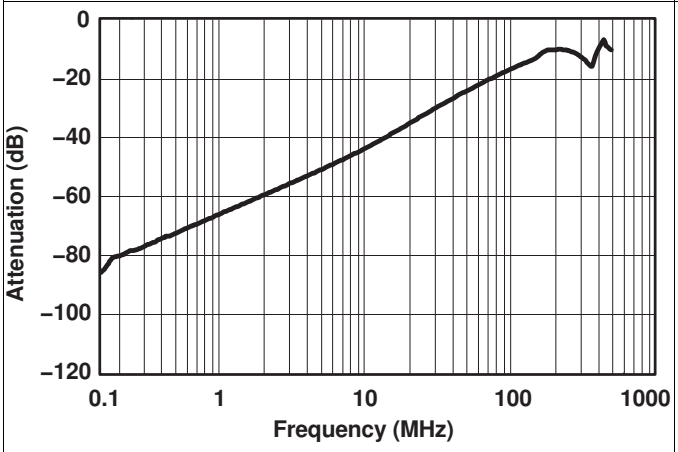


Figure 9. OFF Isolation and Crosstalk (V_+ = 5 V)

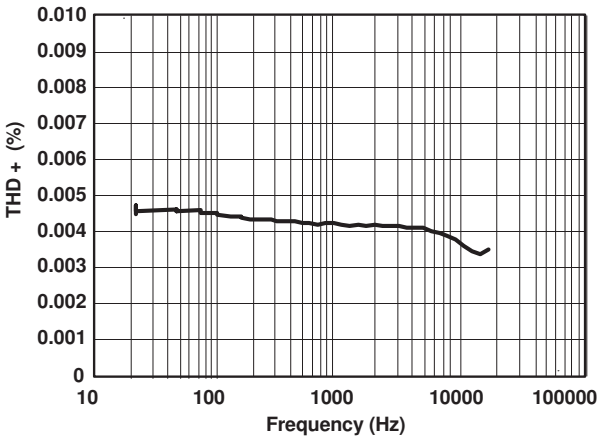


Figure 10. Total Harmonic Distortion vs Frequency

7 Parameter Measurement Information

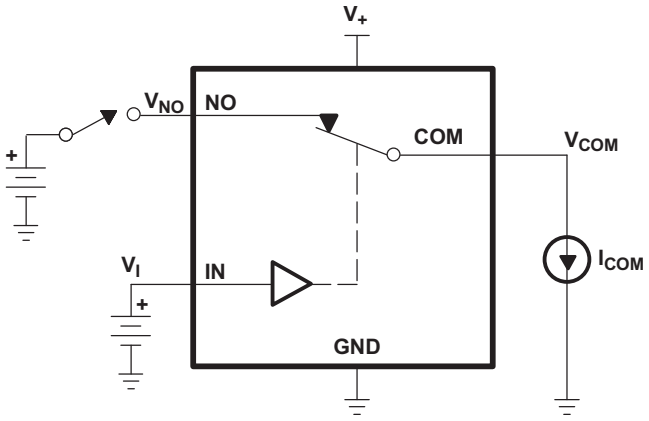


Figure 11. ON-State Resistance (r_{on})

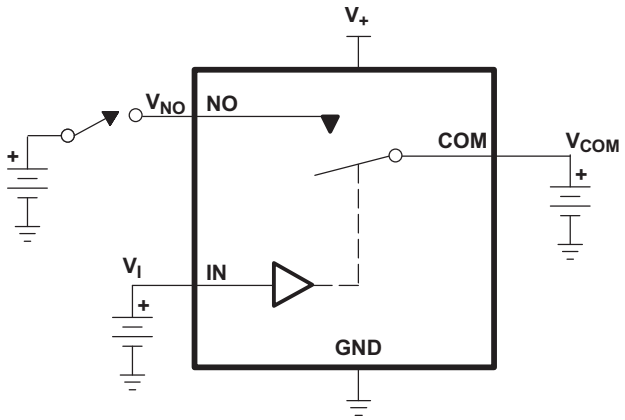


Figure 12. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWR(FF)}$)

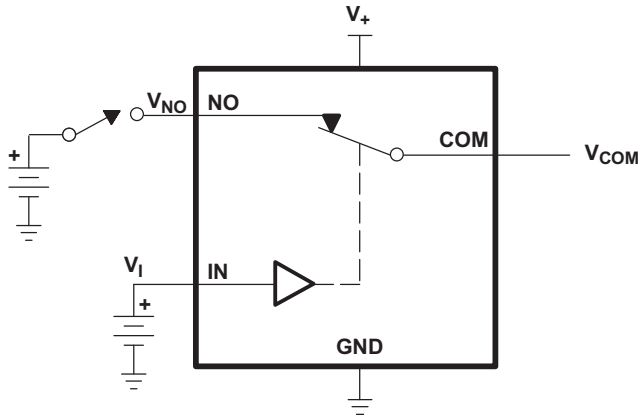


Figure 13. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

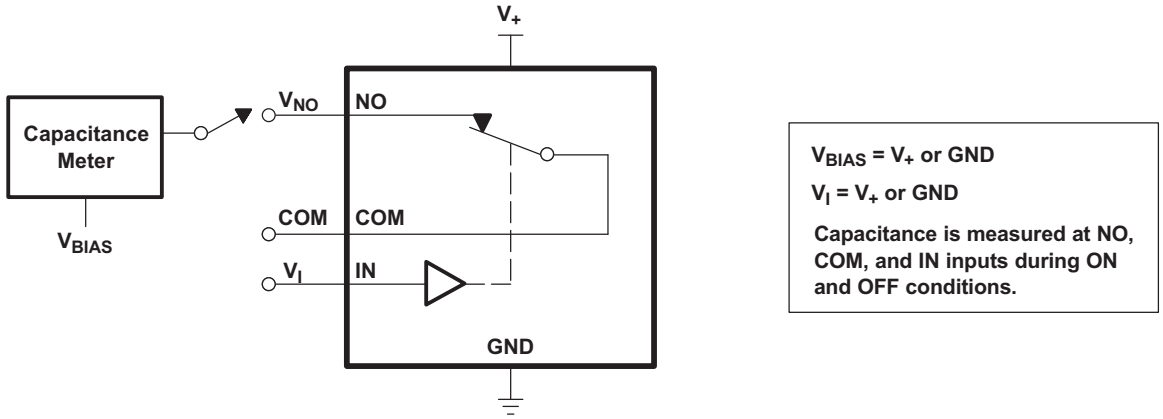
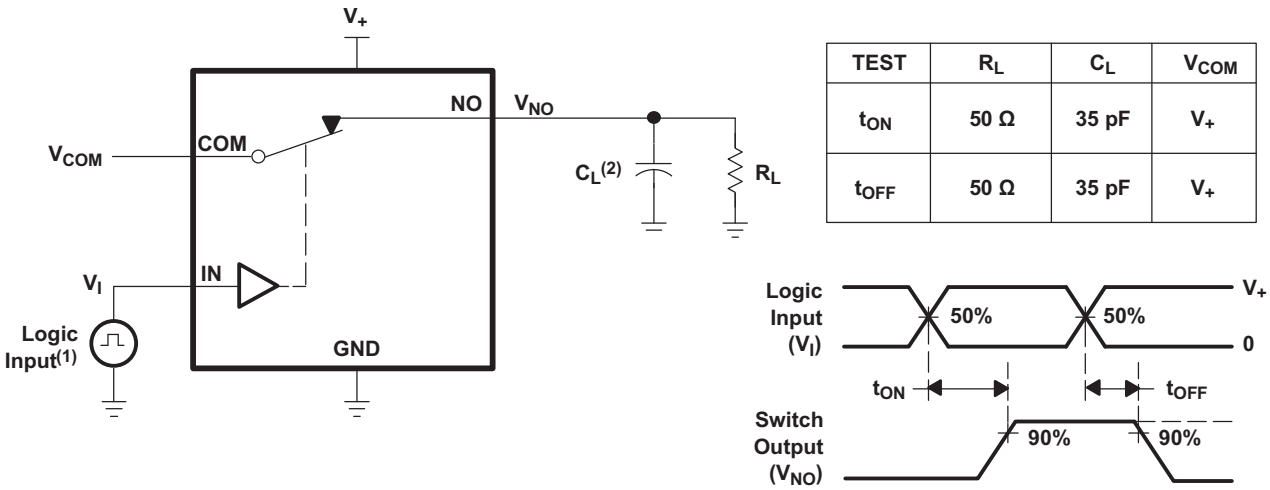


Figure 14. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

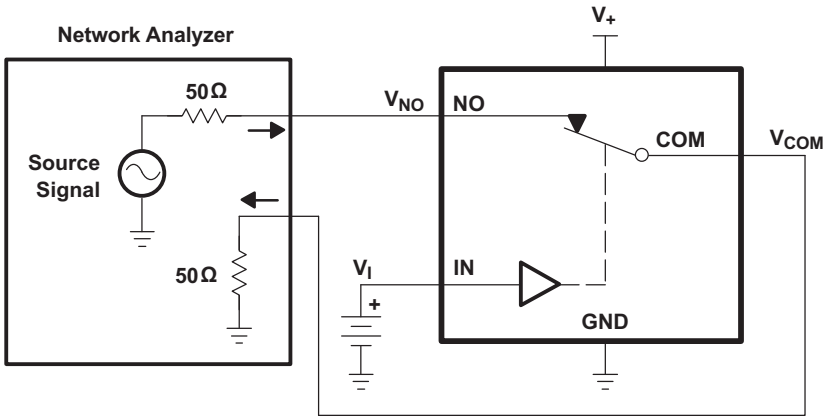


Figure 16. Bandwidth (BW)

Parameter Measurement Information (continued)

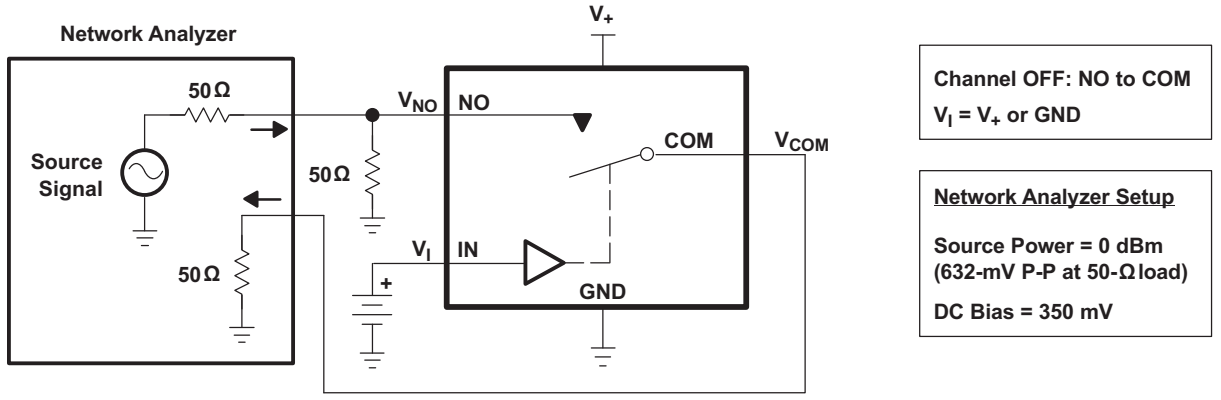


Figure 17. OFF Isolation (O_{ISO})

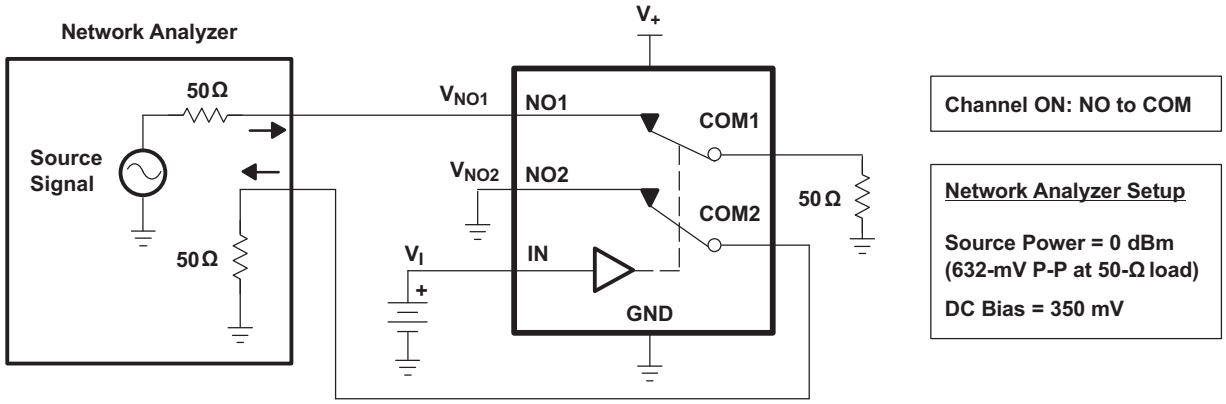
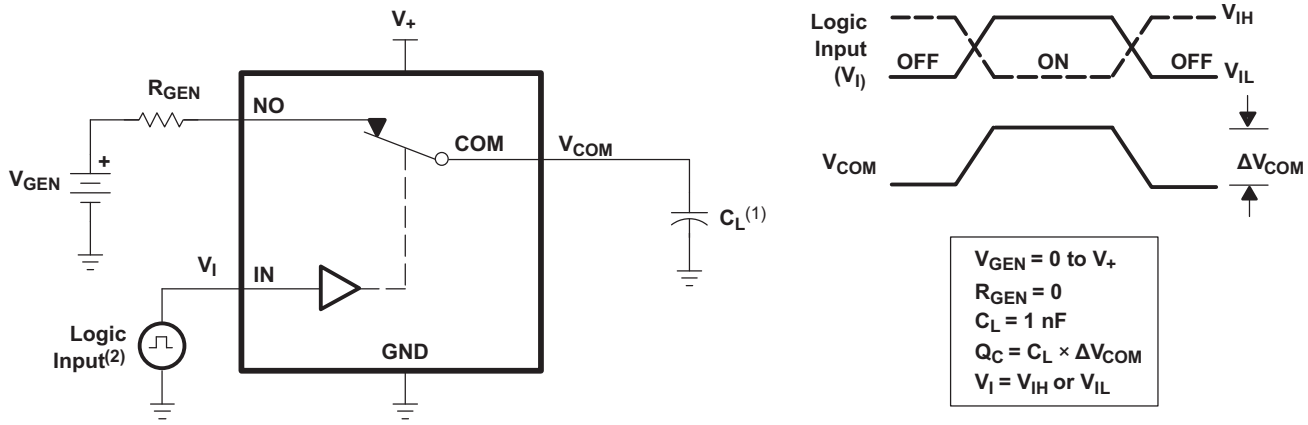


Figure 18. Crosstalk (X_{TALK})

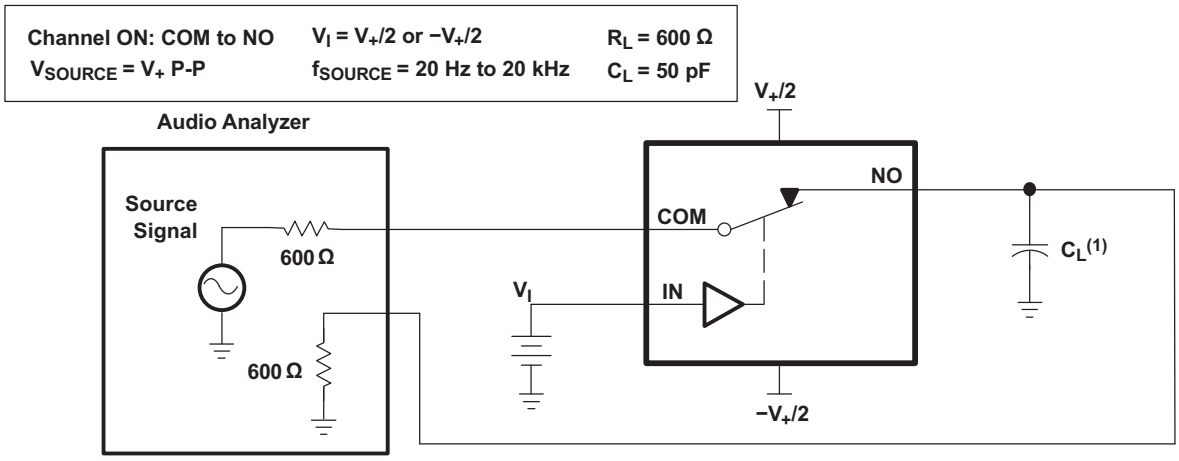


(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 19. Charge Injection (Q_C)

Parameter Measurement Information (continued)



(1) C_L includes probe and jig capacitance.

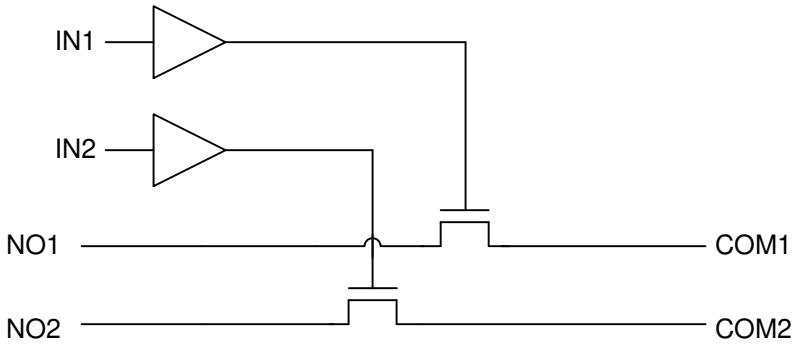
Figure 20. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A23166 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. 表 2 shows the descriptions of each parameter specified in the datasheet.

8.2 Functional Block Diagram



8.3 Feature Description

Tolerant control inputs allow 5-V logic levels to be present on the IN pin at any value of V_{CC}. Low ON-resistance allows minimal signal distortion through device.

8.4 Device Functional Modes

Table 1 shows the functional modes for TS5A23166.

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A23166 dual SPST analog switch is a basic component that could be used in any electrical system design. One example application is a gain selector, which is described in the *Typical Application* section.

9.2 Typical Application

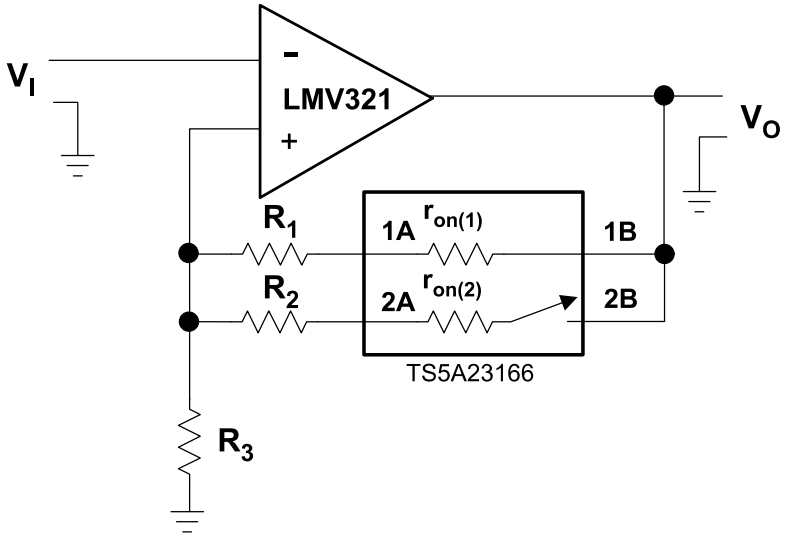


Figure 21. Gain-Control Circuit for OP Amplifier

9.2.1 Design Requirements

By selecting values of R1 and R2, such that Rx >> $r_{on(x)}$, r_{on} of TS5A23166 can be ignored. The gain of op amp can be calculated as follow:

$$Vo / VI = 1 + R|| / R3 \quad (1)$$

$$R|| = (R1+r_{on(1)}) \,||\, (R2+r_{on(2)}) \quad (2)$$

9.2.2 Detailed Design Procedure

Place a switch in series with the input of the op amp. Because the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

Typical Application (continued)

9.2.3 Application Curve

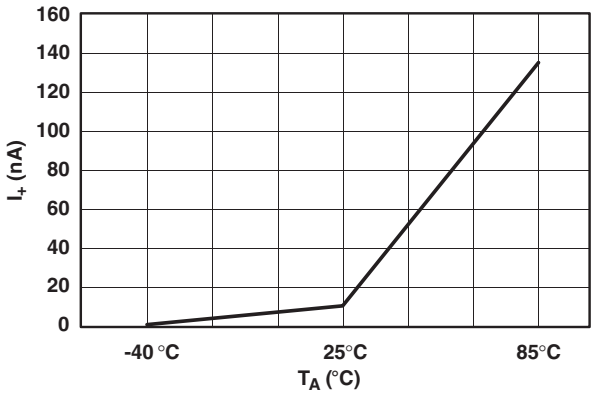


Figure 22. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 23 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

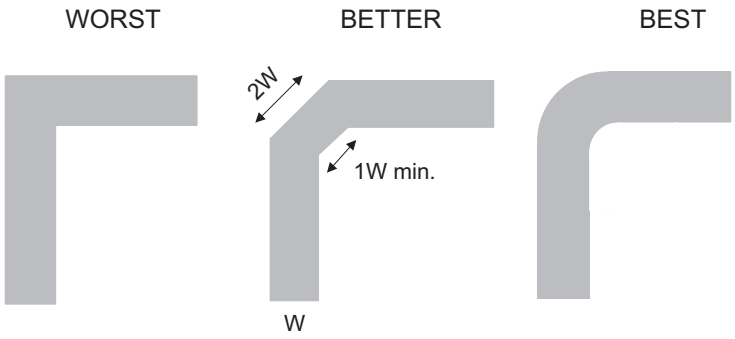


Figure 23. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压
V_{NO}	NO 处的电压
r_{on}	通道导通时 COM 和 NO 端口之间的电阻
r_{peak}	额定电压范围的通态电阻峰值
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NO(OFF)}$	在最不理想的输入和输出条件下，相应通道（NO 到 COM）处于关断状态时，在 NO 端口测得的泄漏电流
$I_{NO(PWROFF)}$	在电源关断状态下，V_+ = 0 时，在 NO 端口测量的泄漏电流
$I_{COM(OFF)}$	在最不理想的输入和输出条件下，相应通道（COM 到 NO）处于关断状态时，在 COM 端口测得的泄漏电流
$I_{COM(PWROFF)}$	在电源关断状态下，V_+ = 0 时，在 COM 端口测量的泄漏电流
$I_{NO(ON)}$	相应通道（NO 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NO 端口测得的泄漏电流
$I_{COM(ON)}$	相应通道（COM 到 NO）处于导通状态且输出 (NO) 处于开路状态时，在 COM 端口测得的泄漏电流
V_{IH}	控制输入 (IN) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN) 逻辑低电平的最大输入电压
V_I	控制输入 (IN) 处的电压
I_{IH}、I_{IL}	控制输入 (IN) 处测量的泄漏电流
t_{ON}	开关导通时间。此参数是在特定条件范围下，开关导通时，通过数字控制 (IN) 信号和模拟输出（COM 或 NO）信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在特定条件范围下，开关关断时，通过数字控制 (IN) 信号和模拟输出（COM 或 NO）信号之间的传播延迟测量得出。
Q_C	电荷注入是对从控制 (IN) 输入到模拟（NO 或 COM）输出产生的多余信号耦合的度量。电荷注入以库仑为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_{COM}$，$C_L$ 是负载电容，ΔV_{COM} 是模拟输出电压的变化。
$C_{NO(OFF)}$	相应通道（NO 到 COM）关断时 NO 端口的电容
$C_{COM(OFF)}$	相应通道（COM 到 NO）关断时 COM 端口的电容
$C_{NO(ON)}$	相应通道（NO 到 COM）导通时 NO 端口的电容
$C_{COM(ON)}$	相应通道（COM 到 NO）导通时 COM 端口的电容
C_I	控制输入 (IN) 电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NO 到 COM）处于关断状态时，在特定频率下测量得出。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。
THD	总谐波失真用于描述由模拟开关导致的信号失真。其定义为二次、三次和更高次谐波与基波绝对幅度之比的均方根 (RMS) 值。
I_+	静态电源电流，以及 V_+ 或 GND 的控制 (IN) 引脚

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A23166DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(AM, JAMQ, JAMR) JZ
TS5A23166DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AM, JAMQ, JAMR) JZ
TS5A23166DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAMR
TS5A23166DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAMR
TS5A23166YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZTR	Active	Production	DSBGA (YZT) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN
TS5A23166YZTR.B	Active	Production	DSBGA (YZT) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JMN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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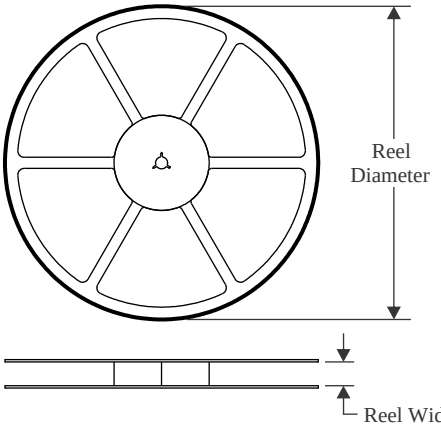
and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

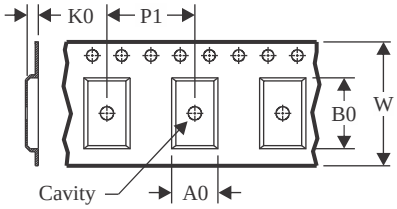
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

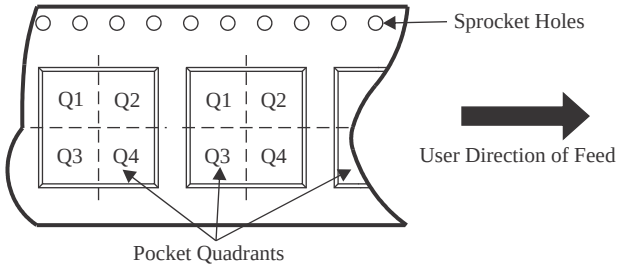


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

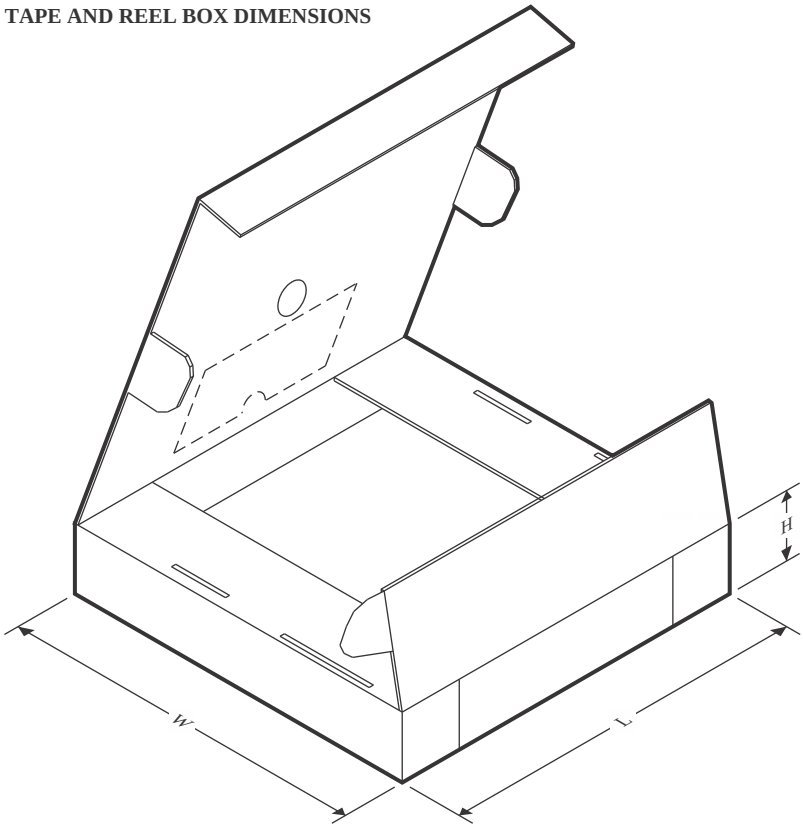
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23166DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A23166YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
TS5A23166YZTR	DSBGA	YZT	8	3000	178.0	9.2	1.02	2.02	0.75	4.0	8.0	Q1

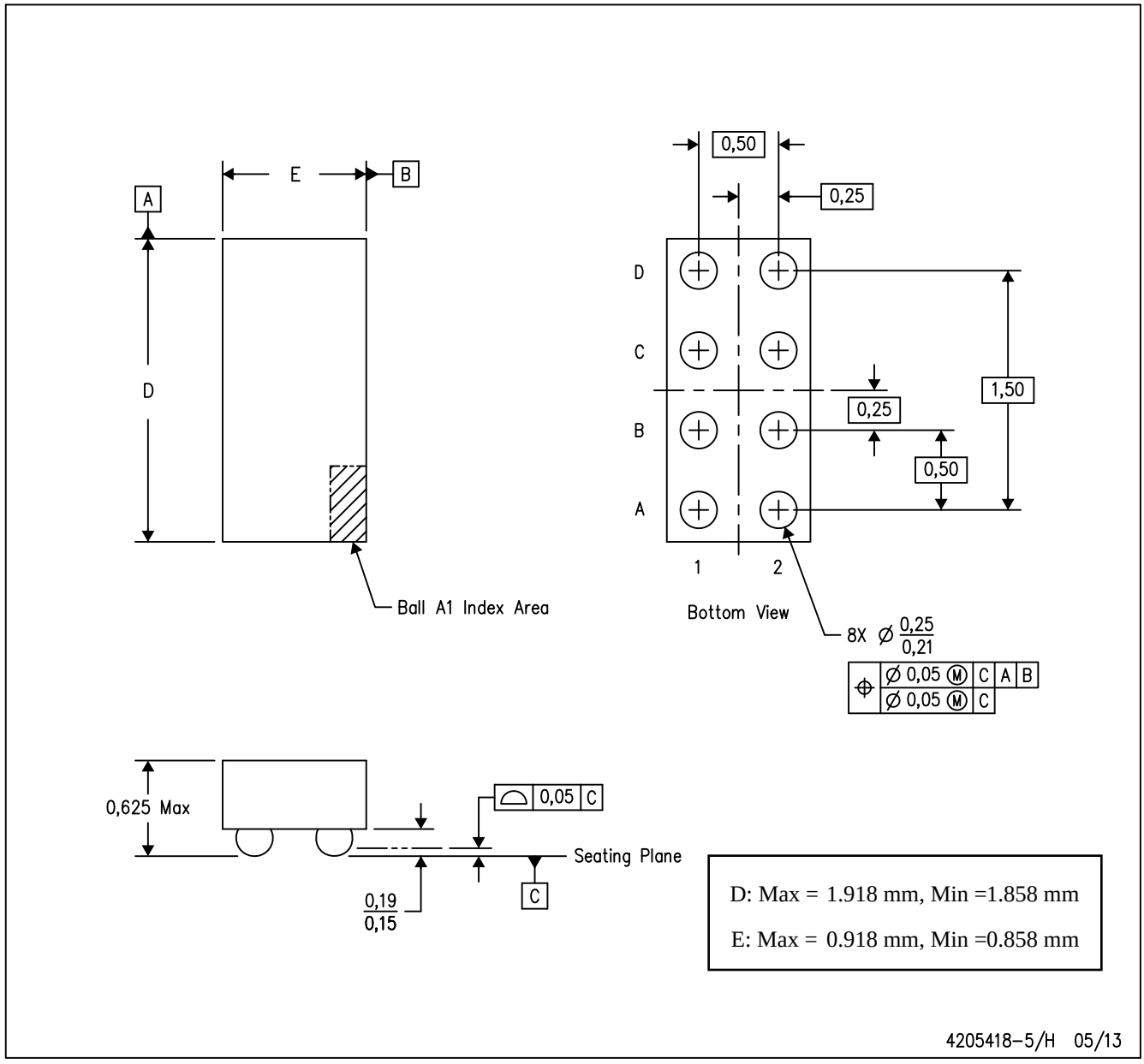
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A23166YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
TS5A23166YZTR	DSBGA	YZT	8	3000	220.0	220.0	35.0

YZT (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

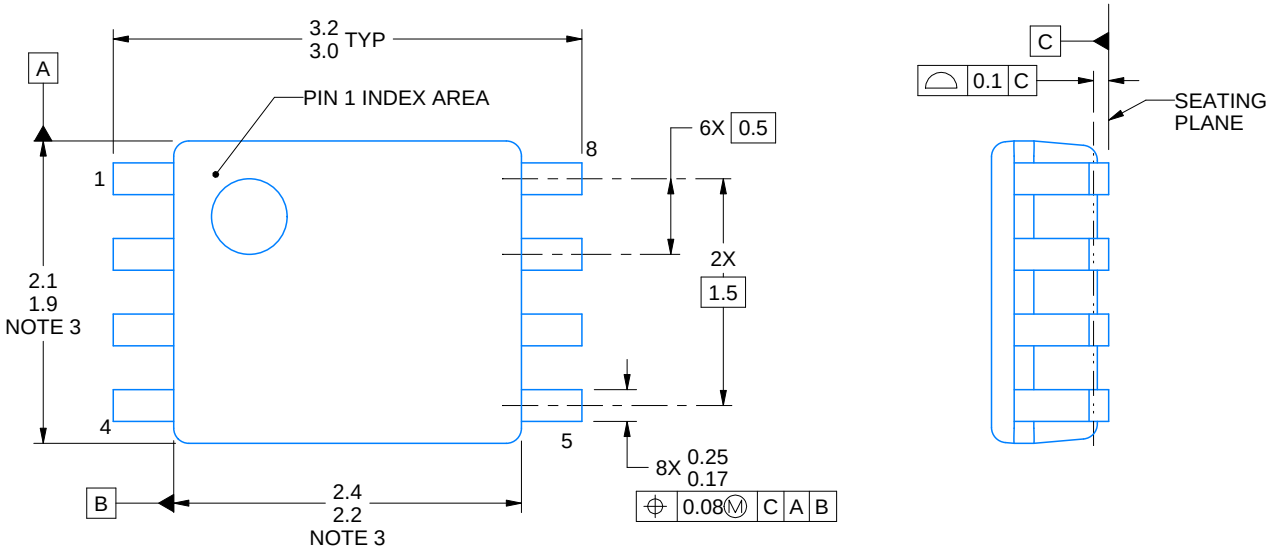
NanoFree is a trademark of Texas Instruments.

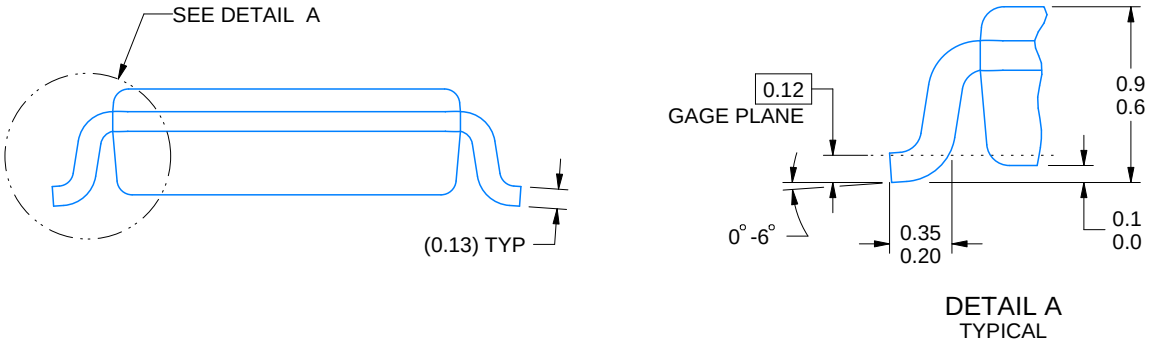
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

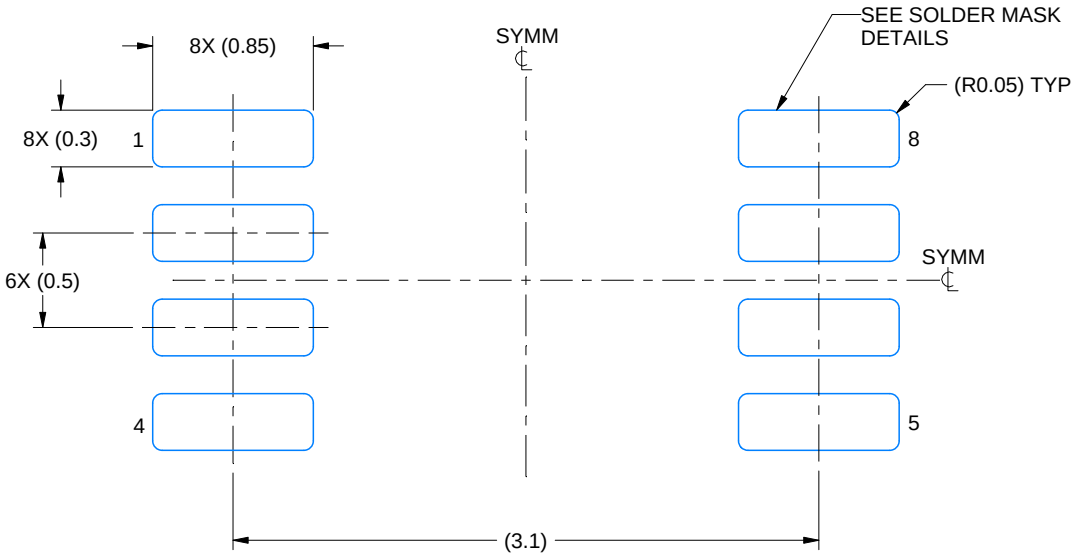




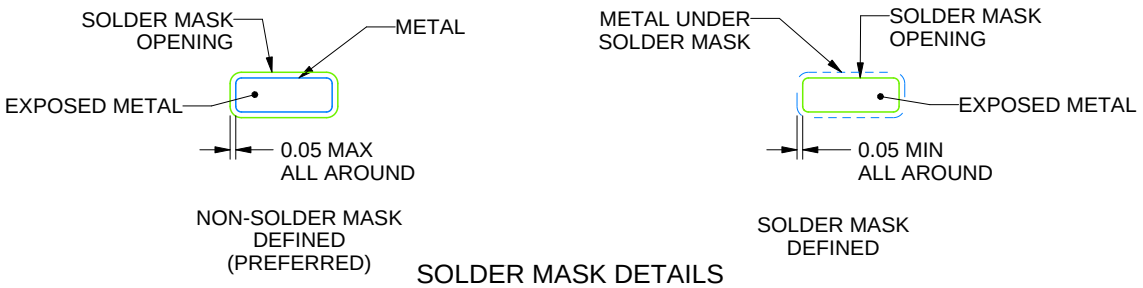
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

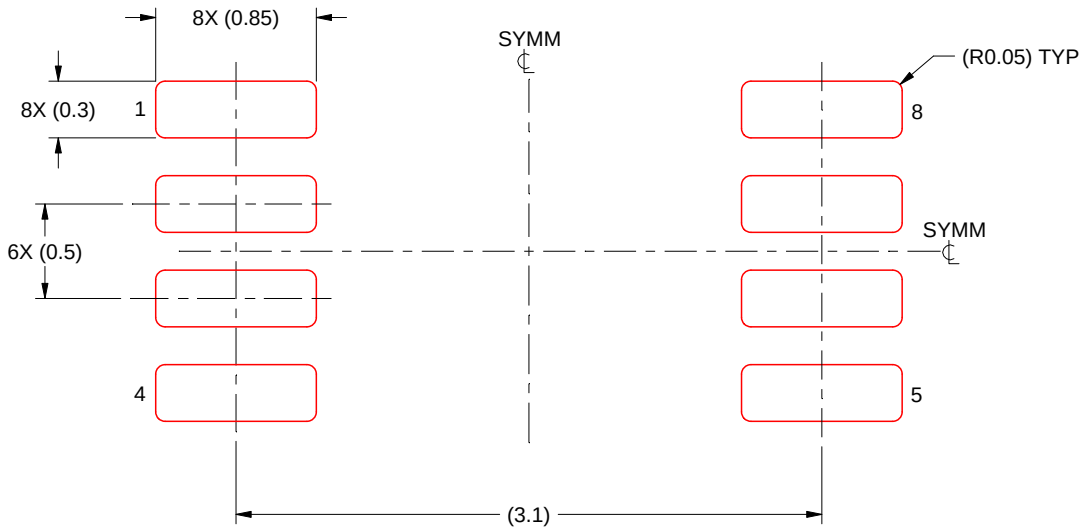


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

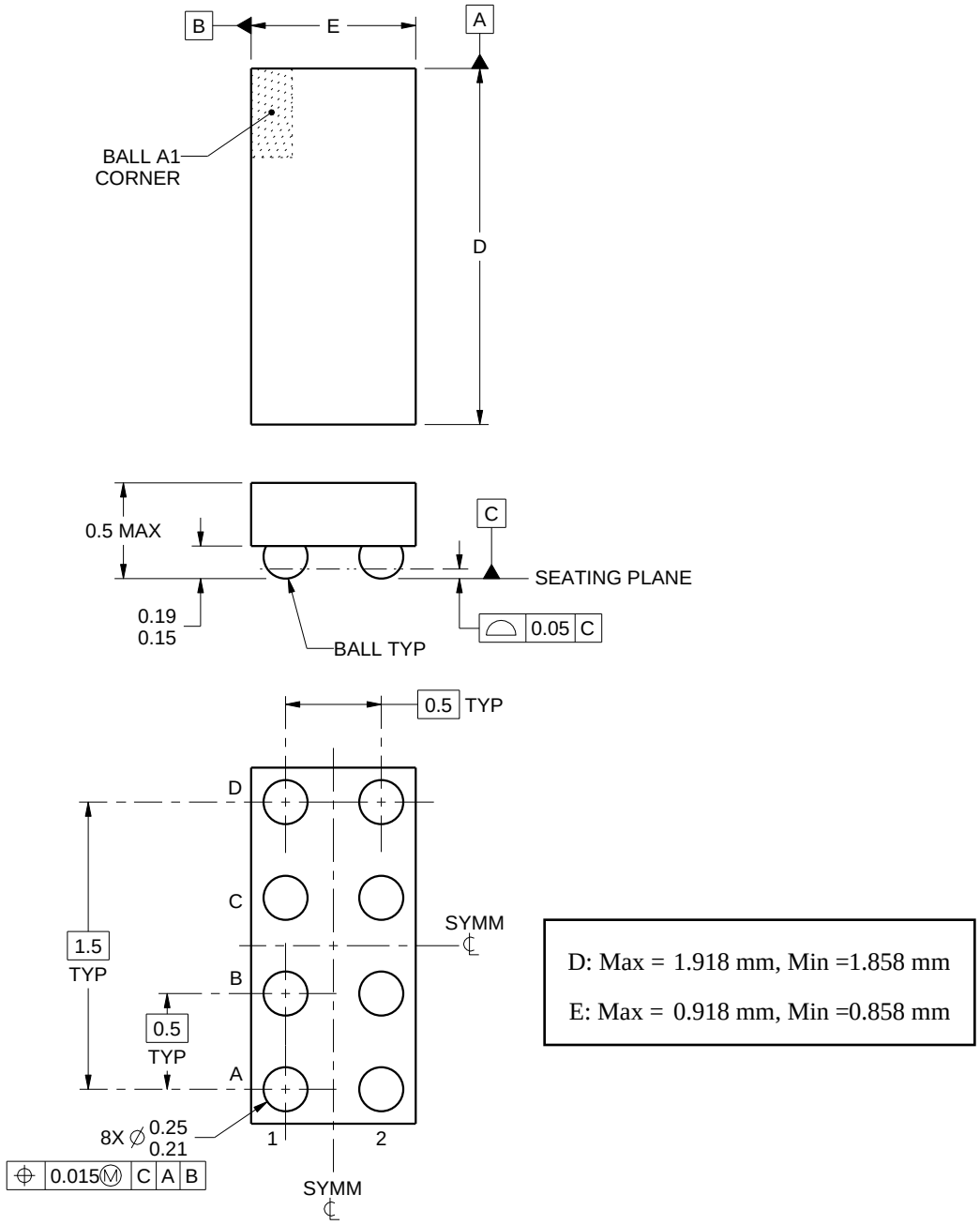
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

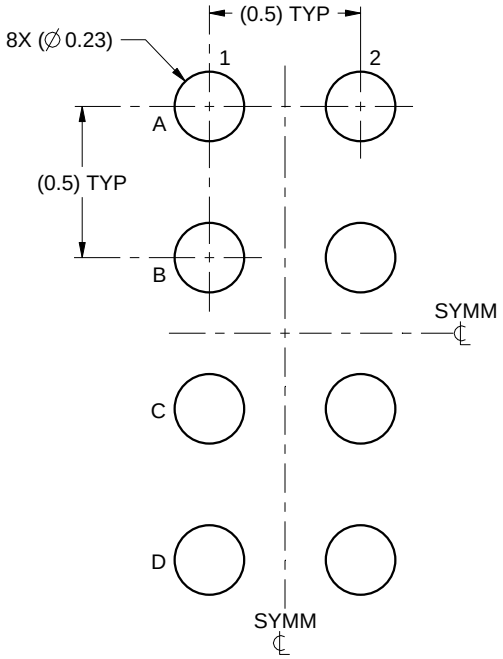
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

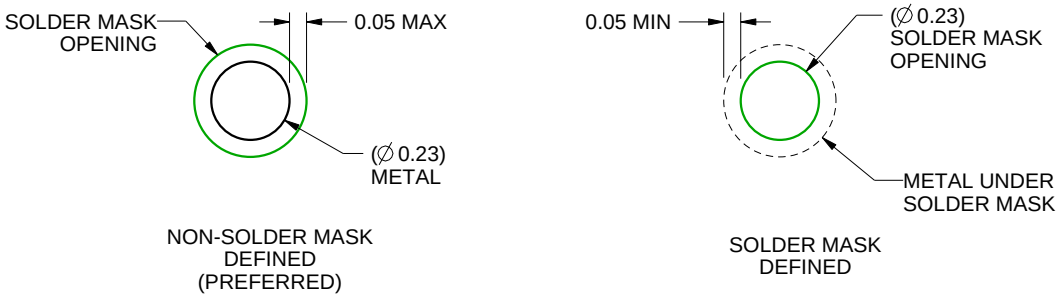


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

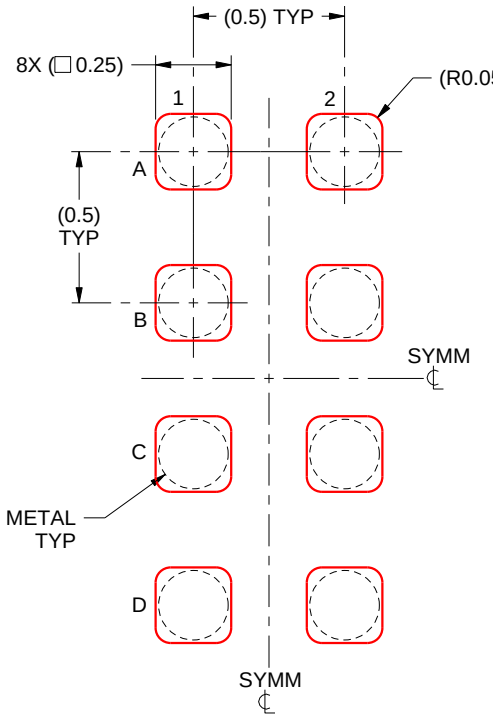


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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