DP3T开关是具有阻抗检测功能的微型USB开关可以支持USB, UART, 音频, 和充电设备检测

查询样品: TSU5611

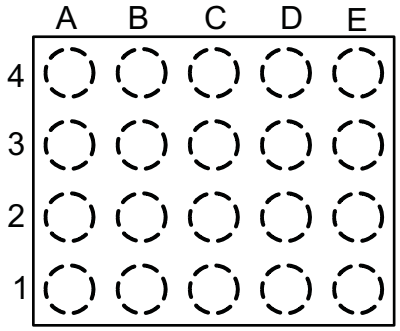
特性

- 兼容附件
  - **USB** 数据线缆
  - **UART** 线缆
  - 充电设备**(**专用充电设备或者主机**/**充电设备**)**
  - 有麦克风的立体声耳机
- 用于**VREF**和麦克偏置电压的集成低压线性稳压器**(LDOs)**
- **USB** 和**UART**路径支持 **USB 2.0**高速接口
- 音频通道提供负轨道支持和
- 支持工厂测试模式
- **1.8-V** 兼容 **I²C** 接口
- 控制输入符合 **1.8 V** 逻辑要求
  - **1500-V** 人体模型 **(A114-B, Class II)**
  - **1000 V** 充电器件模型（**C101**）

应用

- 手机与智能电话
- 平板 **PC**
- 数码相机与摄像机
- 全球卫星定位**(GPS)**导航系统
- 具有**USB/UART**的微型**USB**接口

YZP 封装
顶视图



针脚指定

	A	B	C	D	E
4	MIC	ISET	UART_TX	USB_DM	USB_DP
3	R2.2K	$\overline{INT}$	UART_RX	ID	DP
2	SDA	SCL	DSS	GND	数据手册
1	CLDO	$V_{供电}$	AUDIO_R	AUDIO_L	V_{BUS}

说明

TSU5611被设计成能够与手机UART,USB和通过微型USB连接器与外部设备连接的音频芯片进行连接。 这个开关特有阻抗检测功能用以识别通过微型USB端口的DP和DM连接的多种配件。 当一个配件插入到微型USB端口时, 这个开关使用侦测机制以识别这个配件(详细信息请参考State Machine期刊). 然后它将切换到合适的频道—数据, 音频, 或者UART。

TSU5611有一个 I2C接口用于与手机基带或者应用设备处理器进行通信。 当微型USB接口侦测到任何插入设时，一个中断会产生。 当设备拔出时，产生另外一个中断。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WSCP–YZP (0.5-mm pitch)	Tape and Reel	TSU5611YZPR	A7

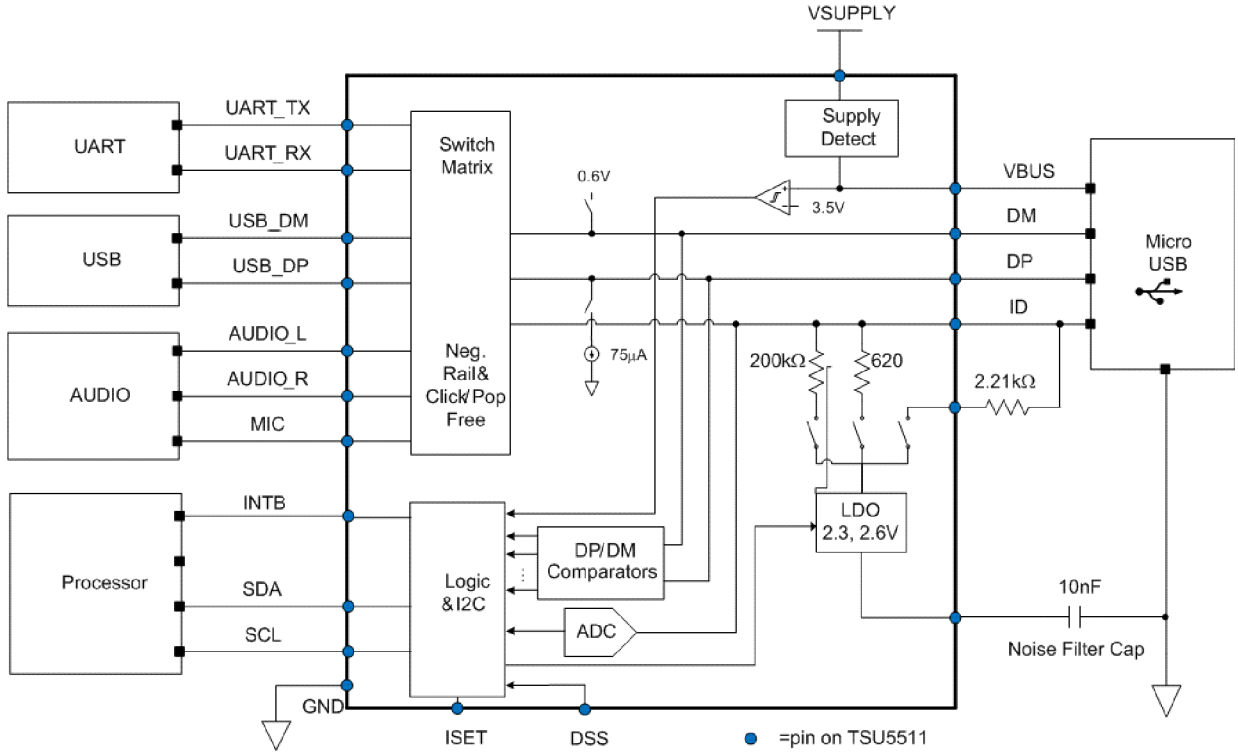
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

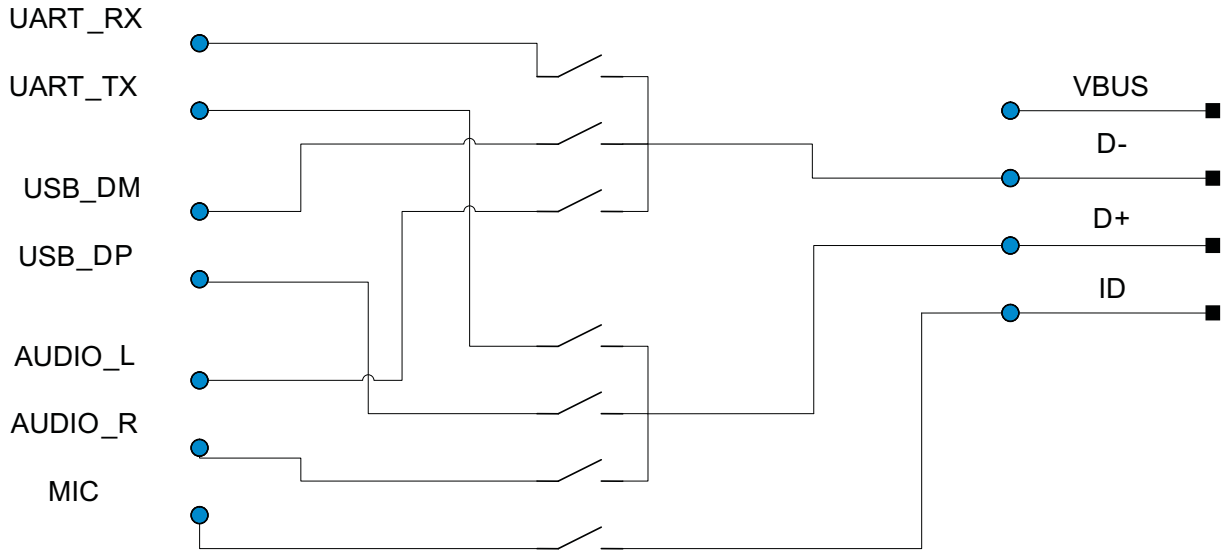
SUMMARY OF TYPICAL CHARACTERISTICS

	USB PATH	UART PATH	AUDIO PATH	MIC PATH
Number of switches	1	1	1	1
ON-state resistance (rON)	5 Ω	5 Ω	3 Ω	8.8 Ω
ON-state resistance match (ΔrON)	1 Ω	1 Ω	1.1 Ω	N/A
ON-state resistance flatness (rON(flat))	0.24 Ω	0.24 Ω	0.1 Ω	0.5 Ω
Turn-on/turn-off time (tON/tOFF)	1 ms	1 ms	1 ms	1 ms
Bandwidth (BW)	830 MHz	830 MHz	788 MHz	573 MHz
OFF isolation (OISO)	–22 dB	–22 dB	–75 dB	–100 dB
Crosstalk (XTALK)	–40 dB	–40 dB	–50 dB	–50 dB
Total harmonic distortion (THD)	N/A	N/A	0.05%	0.0017%
Leakage current (INO(OFF)/INC(OFF))	100 nA	100 nA	100 nA	100 nA
Package options	YZP package, 0.5-mm pitch			

APPLICATION BLOCK DIAGRAM



SWITCH MATRIX BLOCK DIAGRAM



PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
AUDIO_L	D1	I/O	Stereo audio left channel
AUDIO_R	C1	I/O	Stereo audio right channel
CLDO	A1	O	Capacitor connection for LDO noise filtering
DM	E2	I/O	Common I/O port for USB, UART, Audio. Connected to USB receptacle.
DP	E3	I/O	Common I/O port for USB, UART, Audio. Connected to USB receptacle.
DSS	C2	I	Pulldown or pullup resistor connection to determine default switch
GND	D2	GND	Ground
ID	D3	I/O	Common I/O port for microphone, ID detection
INT	B3	O	Open-drain interrupt output. Connect an external pullup resistor.
ISET	B4	O	Output to charger for high-current charging mode. Open-drain output.
MIC	A4	I/O	Microphone signal
R2.2K	A3	I	2.21 kΩ connection for microphone bias
SCL	B2	I	I2C clock input. Connect an external pullup resistor.
SDA	A2	I/O	I2C data. Connect an external pullup resistor.
UART_RX	C3	I/O	UART receive data
UART_TX	C4	I/O	UART transmit data
USB_DM	D4	I/O	USB D– connected to host
USB_DP	E4	I/O	USB D+ connected to host
V_{BUS}	E1	Power	VBUS power supply from USB receptacle
V_{SUPPLY}	B1	Power	2.8-V to 4.4-V battery supply voltage

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BUS}	Supply voltage from USB connector		–0.5	28	V
V_{SUPPLY}	Supply voltage from battery		–0.5	6	
V_{USBIO}	Switch I/O voltage range	USB Switch	–0.5	V_{SUPPLY}+0.5	V
V_{UARTIO}		UART Switch	–0.5	V_{SUPPLY}+0.5	
V_{AUDIO}		Audio Switch	–1.5	V_{SUPPLY}+0.5	
V_{MICIO}		Mic Switch	–0.5	V_{SUPPLY}+0.5	
$V_{LOGICI\ O}$	Logic input, output and I/O voltage ranges	DSS, SCL, SDA	–0.5	V_{SUPPLY}+0.5	V
I_{BUS}	Input current on V_{BUS} pin			100	mA
I_{SUPPLY}	Input current on V_{SUPPLY} pin			100	mA
I_{GND}	Continuous current through GND			100	mA
I_K	Analog port diode current		–50	50	mA
I_{SW-DC}	ON-state continuous switch current		–60	60	mA
I_{SWPEAK}	ON-state peak switch current		–150	150	mA
I_{IK}	Digital logic input clamp current	V_L < 0		–50	mA
I_{LOGIC_O}	Continuous current through logic output		–50	50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance	YZP package	75.5	°C/W

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{BUS}	Supply voltage from USB connector		4.35	6.7	V
V_{SUPPLY}	Supply voltage from battery		2.8	4.4	V
V_{USBIO}	Switch I/O Voltage Range	USB Switch	0	3.6	V
V_{UARTIO}		UART Switch	0	3.6	V
V_{AUDIO}		Audio Switch	–1.3	1.3	V
V_{MICIO}		Mic Switch	0	2.3	V
$V_{LOGICI\ O}$	Logic input, output and I/O voltage ranges	DSS, SCL, SDA	0	V_{SUPPLY}	V
I_{SW-DC}	ON-state continuous switch current				mA
$I_{SW¬PEAK}$	ON-state peak switch current				mA
T_A	Ambient Temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS(1)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VSUPPLY}$	VSUPPLY supply current	V_{SUPPLY} = 4.2 V, V_{BUS} = 0 V, SEMREN = 0, All switches open		14	18	µA
		V_{SUPPLY} = 4.2 V, V_{BUS} = 0 V, SEMREN = 1, All switches open		14	18	
		V_{SUPPLY} = 4.2 V, V_{BUS} = 0 V, SEMREN = 1, USB or Audio switches closed		60	70	
I_{VBUS}	VBUS supply current	V_{BUS} = 5.0 V, V_{SUPPLY} = 3.6 V, SEMREN=0, All switches open		45	60	µA
		V_{BUS} = 5.0 V, V_{SUPPLY} = 3.6 V, SEMREN=1, All switches open		45	60	
		V_{BUS} = 5.0 V, V_{SUPPLY} = 3.6 V, SEMREN=1, USB or Audio switches closed		80	98	
$V_{VBUSDET}$	VBUS Detect threshold	V_{BUS} = 2.5 V to 5 V with DP-DM short, Read the INT	3.0	3.5	4.0	V
V_{MRCOMP}	Microphone removal threshold	LDO Voltage = 2.6 V, Ramp ID down, Read the INT			2.20	V
		LDO Voltage = 2.3 V, Ramp ID down, Read the INT			1.95	
V_{SECOMP}	SEND/END threshold	LDO Voltage = 2.6 V or 2.3 V, Ramp ID up from 0 V, Read the INT		0.15		V
R_{ID1}	ID resistance1	ID_200 = 1, V_{SUPPLY} = 3.6 V	160	200	240	kΩ
R_{ID2}	ID Resistance2	ID_620 = 1, V_{SUPPLY} = 3.6 V		620	850	Ω

(1) V_O is equal to the asserted voltage on DP_CON and DM_CON pins. V_I is equal to the asserted voltage on DP_HT and DM_HT pins. I_O is equal to the current on the DP_CON and DM_CON pins. I_I is equal to the current on the DP_HT and DM_HT pins.

LDO ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS}	Input voltage		4.35	5	6.7	V
V_{SUPPLY}			2.8		4.4	
V_{OUT-26}	Output voltage	I_O = 0 mA	2.54	2.6	2.65	V
I_{O-26}	Max output current	Measured at R2.2K pin			10	µA
V_{OUT-23}	Output voltage	I_O = 0mA	2.2	2.3	2.35	V
I_{O-23}	Max output current	Measured at R2.2K pin			500	µA
PSR_{217}	Power supply rejection	V_{OUT} = 2.3 V, V_{SUPPLY} = 3.2 V, I_O = 150 µA to 450 µA, f = 217 Hz		–60		dB
PSR_{1k}		V_{OUT} = 2.3V, V_{SUPPLY} = 3.2 V, I_O = 150 µA to 450 µA, f = 1kHz		–60		dB
e_{n-OUT}	Integrated output noise	V_{OUT} = 2.3 V, V_{SUPPLY} = 3.2 V, I_O = 150 µA to 450 µA, f = 20 Hz to 20 kHz (A-weighted)		3	10	µV
$T_{r\ 1}$	Rise time1	I_O = 20 µA, R2.2K = 0 V to 2.6 V		178		µs
$t_{r\ 2}$	Rise time2	I_O = 20 µA, R2.2K = 2.3 V to 2.6 V		260		µs
t_f	Fall time	I_O = 0 µA, R2.2K = 2.6 V to 2.3 V		2.5		ms

USB SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V TO 4.4 V SUPPLY(1)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_{USBIO}	Analog signal range			0		3.6	V
r_{ON}	ON-state resistance	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		4.5	10	Ω
Δr_{ON}	ON-state resistance match between channels	V_I = 0.4 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		1	1.5	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		0.5	1.5	Ω
$I_{IO(OFF)}$	V_I or V_O OFF leakage current	V_I = 0.3 V, V_O = 2.5 V or V_I = 2.5 V, V_O = 0.3 V, V_{SUPPLY} = 4.4 V,	Switch OFF		25	360	nA
$I_{IO(ON)}$	V_O ON leakage current	V_I = OPEN, V_O = 0.3 V or 2.5 V, V_{SUPPLY} = 4.4 V	Switch ON		10	360	nA
DYNAMIC							
t_{ON}	Turn-on time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		100		µs
t_{OFF}	Turn-OFF time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		20		µs
$C_{I(OFF)}$	V_I OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		6.5		pF
$C_{O(OFF)}$	V_O OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		3		pF
$C_{I(ON)}$, $C_{O(ON)}$	V_I, V_O ON capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz,	Switch ON		9		pF
BW	Bandwidth	R_L = 50 Ω	Switch ON		920		MHz
O_{ISO}	OFF Isolation	f = 240 MHz, R_L = 50 Ω	Switch OFF		–29		dB
X_{TALK}	Crosstalk	f = 240 MHz, R_L = 50 Ω	Switch ON		–40		dB

(1) V_I = asserted voltage on DP & DM pin. V_O = Asserted voltage on USB_DP & USB_DM pin. I_O = current on the USB_DP or USB_DM pin

UART SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V TO 4.4 V SUPPLY(1)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_{USBIO}	Analog signal range			0		3.6	V
r_{ON}	ON-state resistance	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		4.5	10	Ω
Δr_{ON}	ON-state resistance match between channels	V_I = 0.4 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		1	1.5	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{SUPPLY} = 3.6 V	Switch ON		0.5	1.5	Ω
$I_{IO(OFF)}$	V_I or V_O OFF leakage current	V_I = 0.3 V, V_O = 2.5 V or V_I = 2.5 V, V_O = 0.3 V, V_{SUPPLY} = 4.4 V	Switch OFF		25	360	nA
$I_{IO(ON)}$	V_O ON leakage current	V_I = OPEN, V_O = 0.3 V or 2.5 V, V_{SUPPLY} = 4.4 V	Switch ON		10	360	nA
DYNAMIC							
t_{ON}	Turn-on time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		100		µs
t_{OFF}	Turn-OFF time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		20		µs
$C_{I(OFF)}$	V_I OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		6.5		pF
$C_{O(OFF)}$	V_O OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		3		pF
$C_{I(ON)}$, $C_{O(ON)}$	V_I, V_O ON capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch ON		9		pF
BW	Bandwidth	R_L = 50 Ω	Switch ON		920		MHz
O_{ISO}	OFF Isolation	f = 240 MHz, R_L = 50 Ω	Switch OFF		–29		dB
X_{TALK}	Crosstalk	f = 240 MHz, R_L = 50 Ω	Switch ON		–40		dB

(1) V_I = asserted voltage on DP & DM pin. V_O = Asserted voltage on UART_RX & UART_TX pin. I_O = current on the UART_RX and UART_TX pin

AUDIO SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V TO 4.4 V SUPPLY(1)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
$V_{AUDIO\ IO}$	Analog signal range			–1.3		1.3	V
r_{ON}	ON-state resistance	V_I = +1.3 V, –1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V	AUDIO_L or AUDIO_R DM or DP		3.8	6	Ω
Δr_{ON}	ON-state resistance match between channels	V_I = 1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V	AUDIO_L or AUDIO_R DM or DP		1	1.3	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_I = +1.3 V, –1.3 V, I_O = –20 mA, V_{SUPPLY} = 2.8 V	AUDIO_L or AUDIO_R DM or DP		0.1	0.25	Ω
$I_{IO(OFF)}$	V_I or V_O OFF leakage current	V_I = 0 V, V_O = 1.3 V or V_I = 1.3 V, V_O = –1.3 V, V_{SUPPLY} = 4.4 V	Switch OFF		25	400	nA
$I_{IO(ON)}$	V_O ON leakage current	V_I = OPEN, V_O = –1.3 V or 1.3 V, V_{SUPPLY} = 4.4 V	Switch ON		25	400	nA
DYNAMIC							
t_{ON}	Turn-on time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		100		µs
t_{OFF}	Turn-OFF time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		20		µs
$C_{I(OFF)}$	V_I OFF capacitance	DC bias = 0 V or 2.6 V, f = 10 MHz	Switch OFF		4.5		pF
$C_{O(OFF)}$	V_O OFF capacitance	DC bias = 0 V or 2.6 V, f = 10 MHz	Switch OFF		6.5		pF
$C_{I(ON)}$, $C_{O(ON)}$	V_I, V_O ON capacitance	DC bias = 0 V or 2.6 V, f = 10 MHz	Switch ON		9		pF
BW	Bandwidth	R_L = 50 Ω	Switch ON		900		MHz
O_{ISO}	OFF Isolation	f = 20 MHz, R_L = 50 Ω	Switch OFF		–100		dB
X_{TALK}	Crosstalk	f = 20 MHz, R_L = 50 Ω	Switch ON		–100		dB
THD	Total harmonic distortion	R_L = 16 Ω, C_L = 20 pF, f = 20 Hz~20 kHz, 2.6 Vpp			0.03	0.04	%

(1) V_O = asserted voltage on DP & DM pin. V_I = Asserted voltage on AUDIO_R & AUDIO_L pin. I_O = current on the DP and DM pin. I_I = current on the AUDIO_R & AUDIO_L pin.

MIC SWITCH ELECTRICAL CHARACTERISTICS FOR 2.8 V TO 4.4 V SUPPLY(1)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_{MICIO}	Analog signal range			0		2.3	V
r_{ON}	ON-state resistance	V_I = 2.3 V, I_O =– 20 mA, V_{SUPPLY} = 2.8 V	MIC ID		9	12	Ω
Δr_{ON}	ON-state resistance match between channels	V_I = 2.3 V, I_O = –2 mA, V_{SUPPLY} = 2.8 V	MIC ID		0.5	1	Ω
$r_{ON(flat)}$	ON-state resistance flatness	V_I = 2.3 V, I_O = –2 mA, V_{SUPPLY} = 2.8 V			0.1	0.25	Ω
$I_{IO(OFF)}$	V_I or V_O OFF leakage current	V_I = 0.3 V, V_O = 2.3 V or V_I = 2.3 V, V_O = 0.3 V,V_{SUPPLY} = 4.4 V	Switch OFF		5	200	nA
$I_{IO(ON)}$	V_O ON leakage current	V_I = OPEN, V_O = 0.3 V or 1.8V, V_{SUPPLY} = 4.4 V	Switch ON		5	200	nA
DYNAMIC							
t_{ON}	Turn-on time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		100		µs
t_{OFF}	Turn-OFF time	V_I or V_O = VSUPPLY, R_L = 50 Ω, C_L = 35 pF	From receipt of I^2C ACK bit		20		µs
$C_{I(OFF)}$	V_I OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		6		pF
$C_{O(OFF)}$	V_O OFF capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch OFF		6		pF
$C_{I(ON)}$, $C_{O(ON)}$	V_I, V_O ON capacitance	DC bias = 0 V or 3.6 V, f = 10 MHz	Switch ON		12		pF
BW	Bandwidth	R_L = 50 Ω	Switch ON		573		MHz
O_{ISO}	OFF Isolation	f = 20 kHz, R_L = 50 Ω	Switch OFF		–55		dB
X_{TALK}	Crosstalk	f = 20 kHz, to audio input, R_L = 50 Ω	Switch ON		–100		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 20 pF, f = 20 Hz~20 kHz, 100 mVpp			0.03	0.04	%

(1) V_I = asserted voltage on ID pin. V_O = Asserted voltage on MIC pin. I_I = current on the ID pin. I_O = current on the MIC pin.

DIGITAL SIGNALS (DSS)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{IH}	Input Logic High		V_{SUPPLY} x 0.7	V_{SUPPLY}	V
V_{IL}	Input Logic Low		0	V_{SUPPLY} x 0.3	V
I_{INLEAK}	Input Leakage current	V_I = 0 V to V_{SUPPLY}		16	µA

DIGITAL SIGNALS (SCL, SDA)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{IH}	Input Logic High		1.4		V
V_{IL}	Input Logic Low			0.4	V
I_{INLEAK}	Input Leakage current	V_I = 0 V to V_{SUPPLY}	–1	1	µA

DIGITAL SIGNALS ($\overline{INT}$, ISET)

T_A = –40°C to 85°C, (unless otherwise noted), Typical values are at V_{SUPPLY} = 3.6V, V_{BUS}=5.0V, T_A=25°C

PARAMETER		TEST CONDITION	MIN	MAX	UNIT
V_{ODOL}	Open drain low	I_{ODL} = 4 mA		0.4	V

APPLICATION INFORMATION

Default Switch Position

The DSS (Default Switch State) pin determines if the USB switches or UART switches are selected at startup. An internal pull-down resistor is present on the DSS pin, which selects the USB switches as the default at start-up. If the user wants to default to the UART switches at startup, the DSS pin must be pulled high to V_{SUPPLY}. If the user wants to disable the switches, this must be done using an I^2C write to the SW_Control register after initialization is complete.

DSS PIN	SWITCH STATES
Open / PD	USB
PU	UART

ID Impedance Detection

The TSU5611 features impedance detection for identification of various accessories that might be attached to the microUSB port. Each accessory is identified by a unique resistor value connected between the ID pin and Ground. During impedance detection, the device auto-calibrates an internal current source using an external 2.21k±1% resistor. The current source is then applied to the ID pin while an internal voltage reference is incremented till it matches the ID pin voltage. This produces a 4-bit ADC value that corresponds to the ID resistance found.

ID Resistor	Tolerance	ID No.	ADC Value
0	1%	0	0000
24k	1%	1	0001
56k	1% or 20%	2	0010
100k	1%	3	0011
130k	1%	4	0100
180k	1%	5	0101
240k	1%	6	0110
330k	1%	7	0111
430k	1%	8	1000
620k	1%	9	1001
910k	1%	10	1010
Open	N/A	11	1011

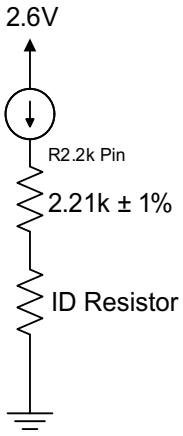


Figure 1. Impedance Detection Circuitry

Supply Detection

The TSU5611 can be powered by either V_{SUPPLY} or V_{BUS}. The TSU5611 will select V_{BUS} as the power source when present and otherwise will select V_{SUPPLY} as the power source when V_{SUPPLY} is present and V_{BUS} is not.

Table 1. Supply Selection and Shut Down Sequence

	V_{SUPPLY}	HANDSET STATUS	MUIC STATUS	POWER SUPPLY
Normal Case	Yes	ON	Active	V_{SUPPLY}
	Yes	OFF(S/W Off)	Shut down	
Sudden Power Loss	Yes	ON	Active	V_{SUPPLY}
	No	OFF	Shut down	
No Battery	No	OFF	Shut down	
	No	ON(V_{BUS})	Active	V_{BUS}
USB Charging	Yes(Charging)	ON(VBUS)	Active	V_{BUS}

Standard I2C Interface Details

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 2). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

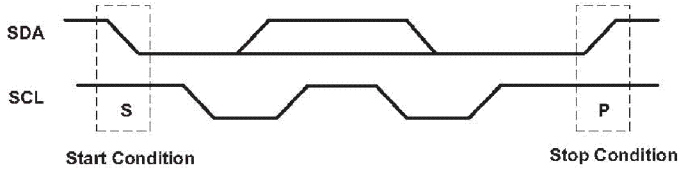


Figure 2. Definition of Start and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP) (see Figure 3).

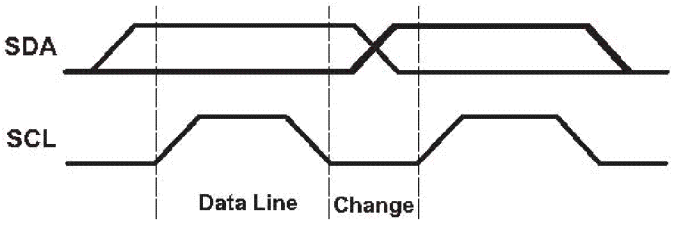


Figure 3. Bit Transfer

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 2).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 4). Setup and hold times must be taken into account.

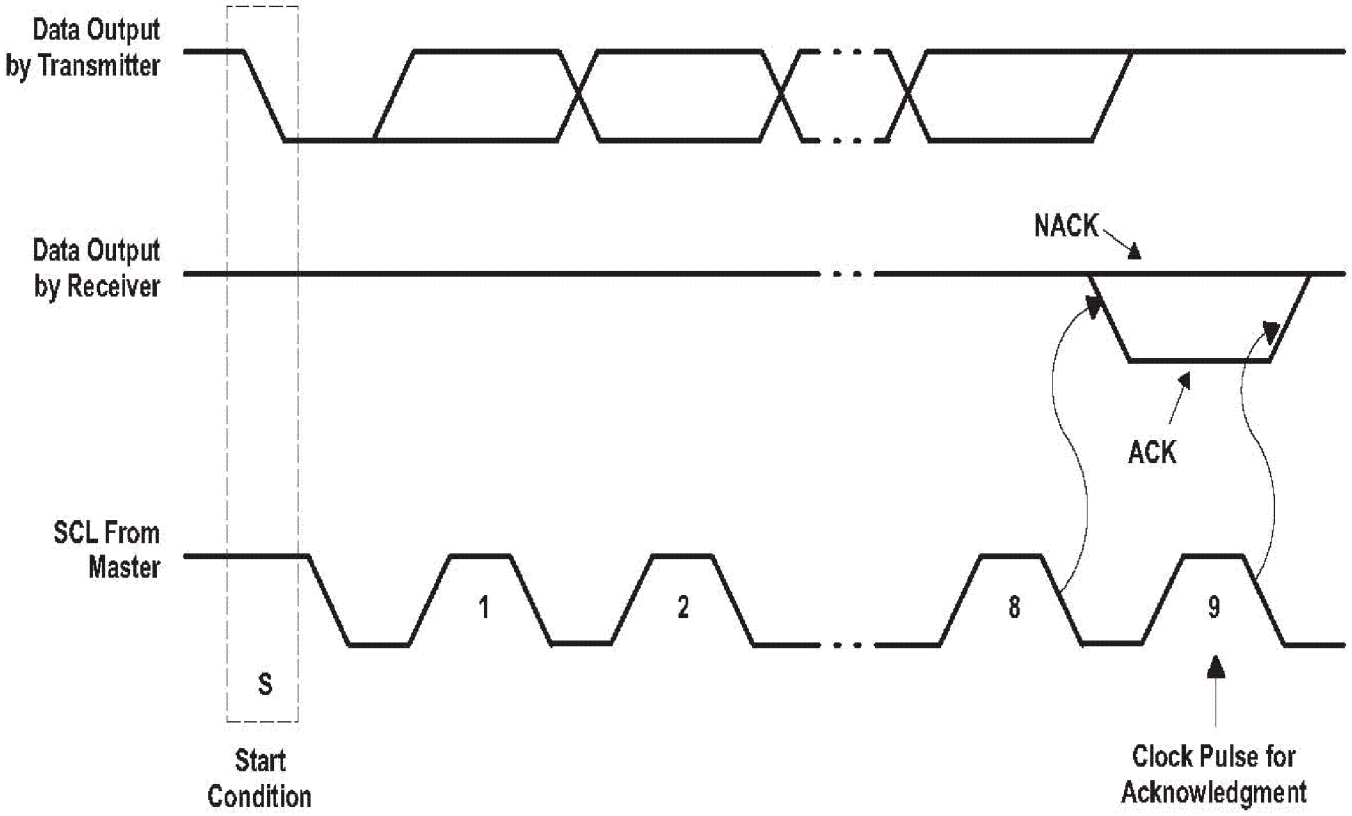


Figure 4. Acknowledgment on I²C Bus

Writes

Data is transmitted to the TSU5611 by sending the device slave address and setting the LSB to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

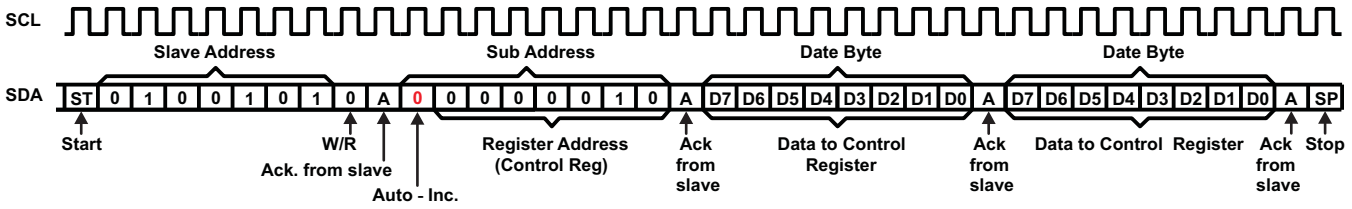


Figure 5. Repeated Data Write to a Single Register

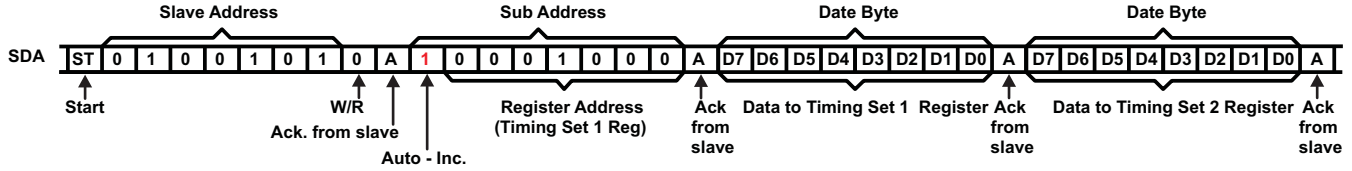


Figure 6. Burst Data Write to Multiple Registers

Reads

The bus master first must send the TSU5611 slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU5611. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse. See Figure 7.

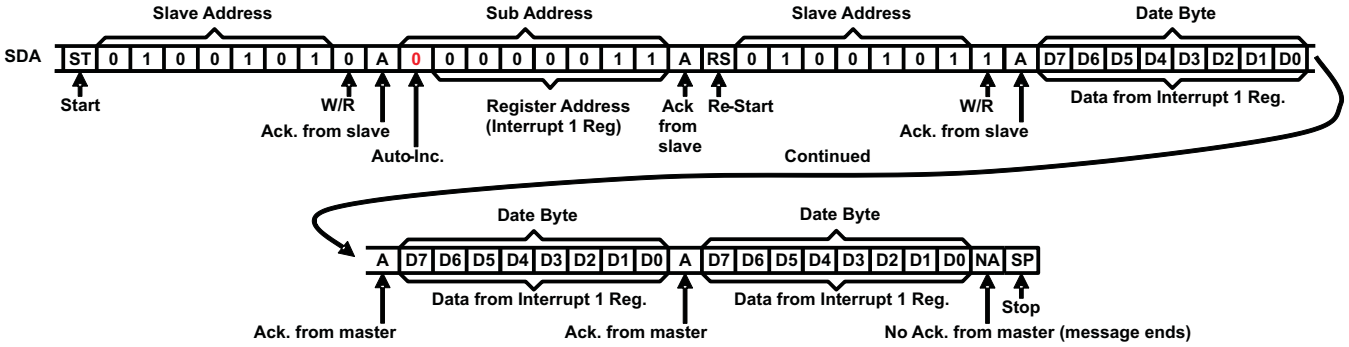


Figure 7. Repeated Data Read from a Single Register – Combined Mode

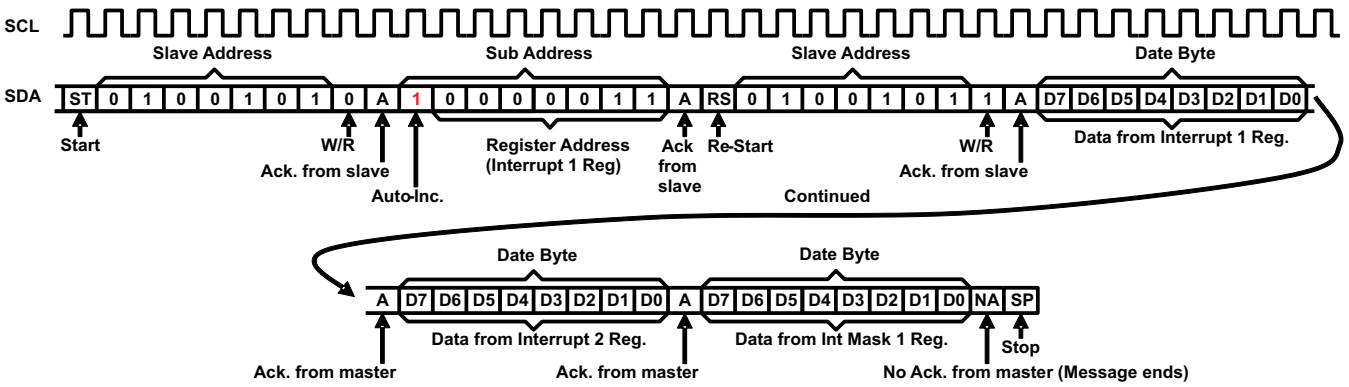


Figure 8. Burst Data Read from Multiple Registers – Combined Mode

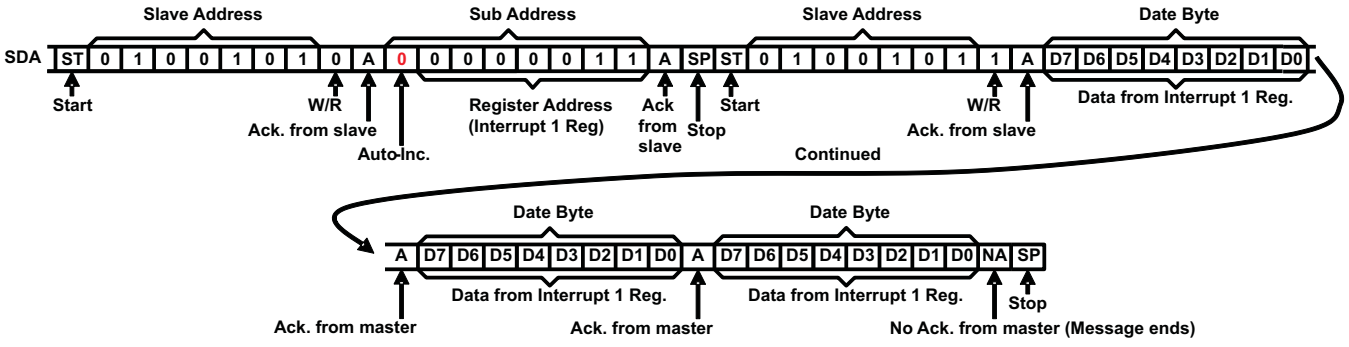


Figure 9. Repeated Data Read from a Single Register – Split Mode

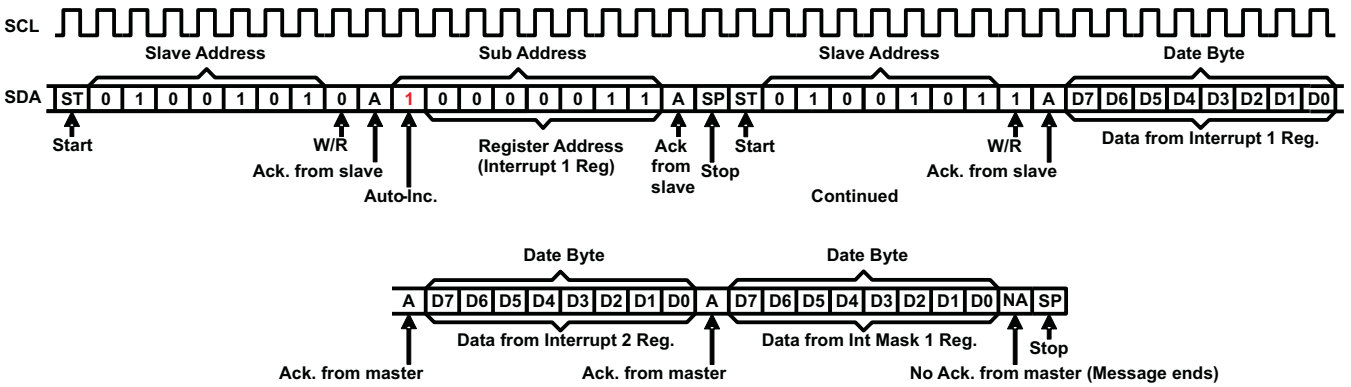


Figure 10. Burst Data Read from Multiple Registers – Split Mode

Notes (Applicable to Figure 5–Figure 10):

- SDA is pulled low on Ack. from slave or Ack. from master.
- Register writes always require sub-address write before first data byte.
- Repeated data writes to a single register continue indefinitely until Stop or Re-Start.
- Repeated data reads from a single register continue indefinitely until No Ack. from master.
- Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur, though no data are changed by the writes. After register 14h is written, writing resumes to register 01h and continues until Stop or Re-Start.
- Burst data reads start at the specified register address, then advance to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No Ack. from master.

SOFTWARE FLOWCHART

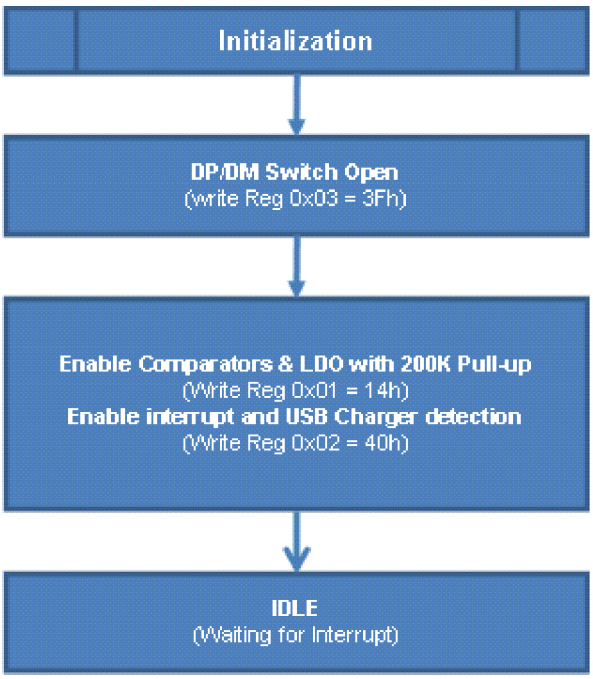


Figure 11. Initialization

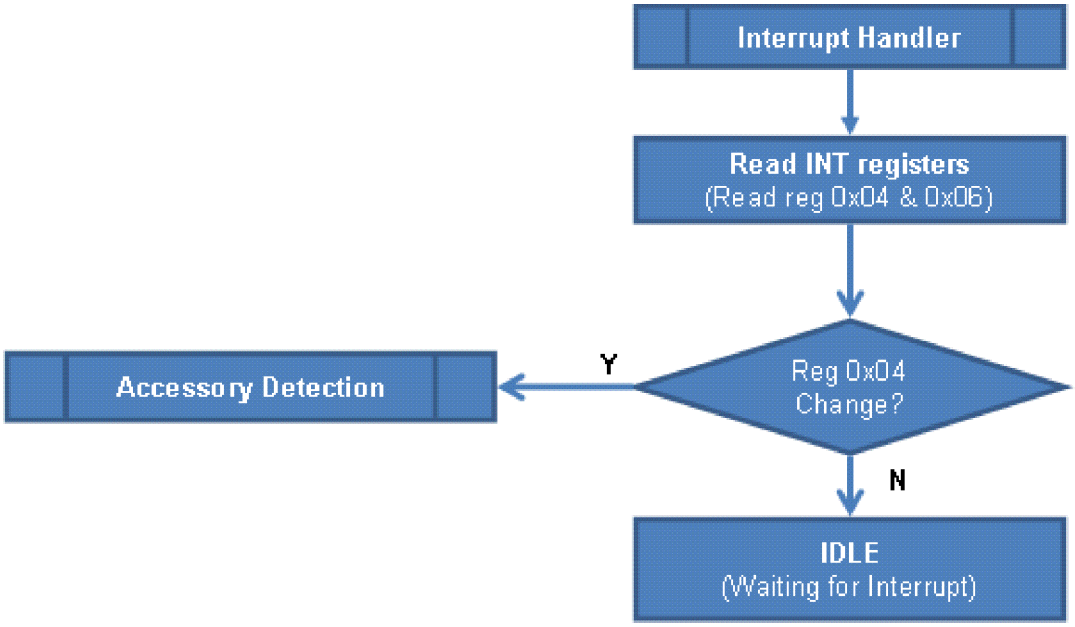


Figure 12. Interrupt Handler

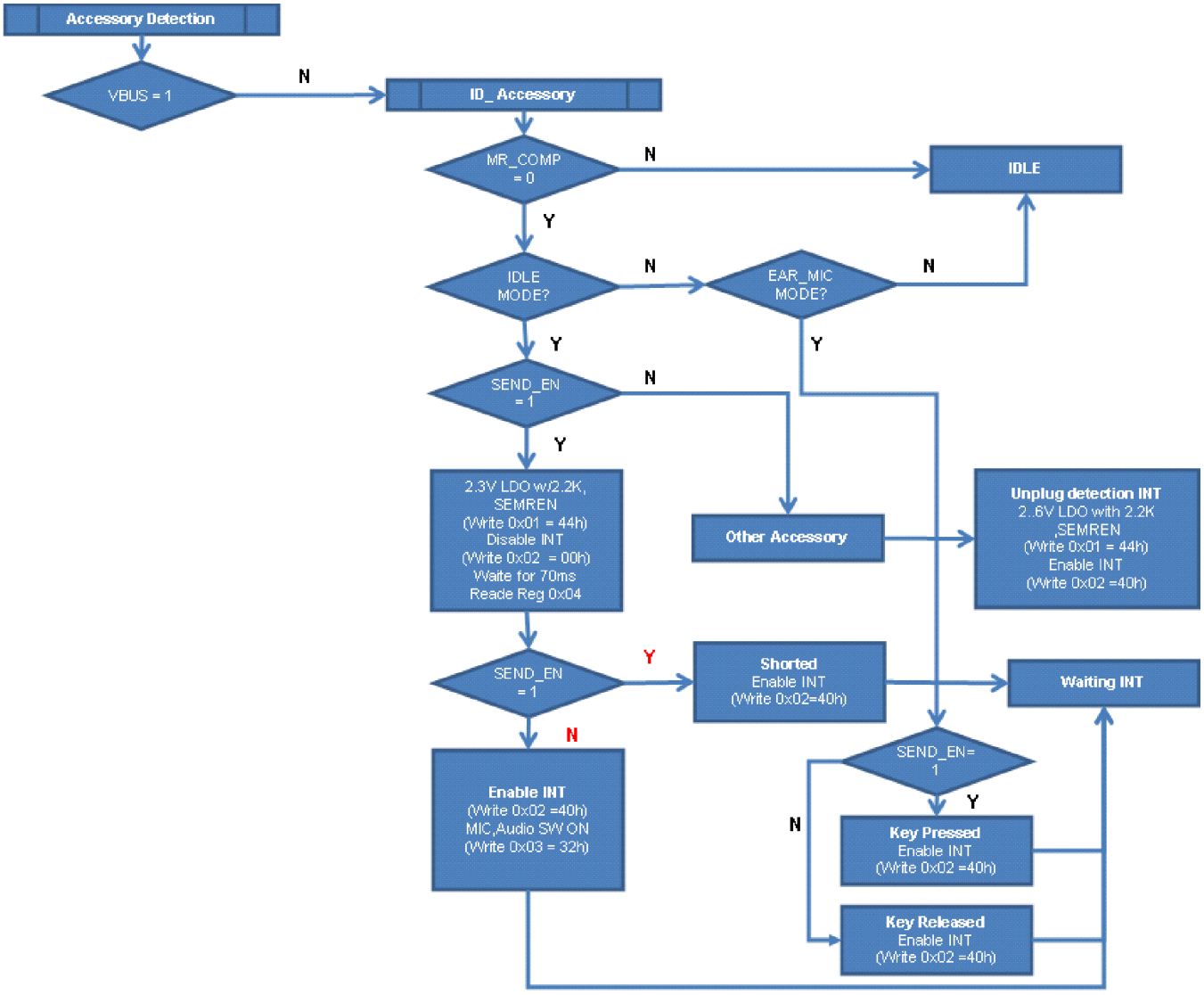


Figure 13. Accessory Detection (1/2)

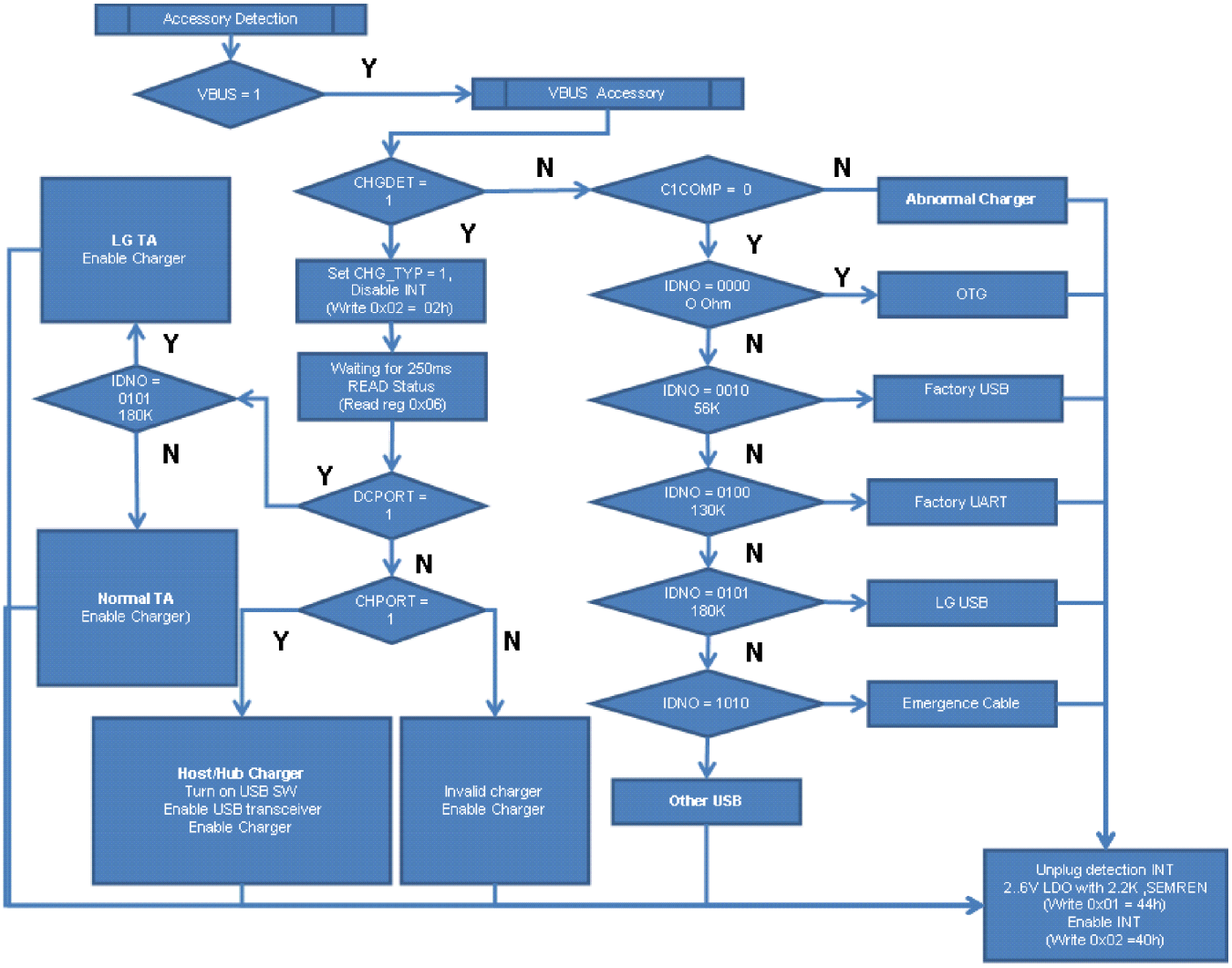


Figure 14. Accessory Detection (2/2)

I²C Register Map(1)(2)

Address (xxh)	Name	TYPE	Reset Value	b7	b6	b5	b4	b3	b2	b1	b0
00	Device ID	R	00011000	VENDOR ID BITS (TI=0001)				REVISION BITS			
01	Control 1	R/W	X0000000	SEMREN2	ID_2P2	ID_620	ID_200	VLDO	SEMREN		
02	Control 2	R/W	0000XX01	INTPOL	INT1_EN	MIC_LP	CP_AUD	MB 200	INT2 EN	CHG_TYP	USB_DET_DIS
03	SW Control	R/W	See (1)		MIC_ON	DP[2:0]		DM[2:0]			
04	INT_Status1	R	00000000(2)	CHGDET	MR_COMP	SEND/END	VBUS	IDNO[3: 0]			
05	INT_Status2	R	00000000							MR_COMP2	SEND/END2
06	Status	R	00XXXXX0	DCPORT	CHPORT						TIMEOUT_CD

(1) Refer SW_Control register description.
(2) Refer INT_Status1 Note2.
(1) Refer SW_Control register description.
(2) Refer INT_Status1 Note2.

Slave Address

NAME	SIZE (BITS)	DESCRIPTION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Slave address	8	1	0	0	0	1	0	0	R/W

Register Descriptions

1. Device ID
Address: 00H
Type: Read

NAME	SIZE (BITS)	DESCRIPTION
Device ID	8	A unique number for chip version
		00011000 bits 0-3 = chip revision, bits 4-7 = Vendor ID (TI=0001b)

2. Control 1
Address: 01H
Type: **Read and Write**

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
01	Control 1	R/W	SEMREM2	ID_2P2	ID_620	ID_200	VLDO	SEMREN1		
Reset Value			X	0	0	0	0	0	0	0

NAME	SIZE (BITS)	DESCRIPTION
SEMREN2	1	0: Disable Send/End2 and MIC Removal2 Comparators and LDO
		1: Enable Send/End2 and MIC Removal2 Comparators and LDO
ID_2P2	1	0: 2.21 kΩ switch open
		1: Connect LDO to ID through 2.21 kΩ external resistor
ID_620	1	0: 620 Ω switch open
		1: Connect LDO to ID through 620 Ω internal resistor (Used for Video)
ID_200	1	0: 200 kΩ switch open
		1: Connect LDO to ID through 200 kΩ internal resistor
VLDO	1	0: LDO voltage = 2.6V (If Manual Switching Mode)
		1: LDO voltage = 2.3V (If Manual Switching Mode)
SEMREN1	1	0: Disable Send/End and MIC Removal Comparators and LDO
		1: Enable Send/End and MIC Removal Comparators and LDO

3. Control 2
Address: 02H

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
02	Control 2	R/W	INTPOL	INT1_EN	MIC_LP	CP_AUD	MB_200	INT2_EN	CHG_TYP	USB_DET_DIS
Reset Value			0	0	0	0	0	0	0	1

NAME	SIZE (BITS)	DESCRIPTION
INT_POL	1	0: Interrupt Polarity = Active Low
		1: Interrupt Polarity = Active High
INT1_EN	1	0: All Interrupts on INT_Status1 disabled (masked)
		1: All Interrupts on INT_Status1 enabled
MIC_LP	1	0: Low Power mode - MIC power pulsing disabled
		1: Low Power mode - MIC power pulsing enabled
CP_AUD	1	0: Click/Pop resistors on AUDIO_L and AUDIO_R disabled
		1: Click/Pop resistors on AUDIO_L and AUDIO_R enabled
MB_200	1	0: 200 kΩ switch to MIC line open
		1: Connect LDO to MIC through 200 kΩ internal resistor
INT2_EN	1	0: All Interrupts on INT_Status2 disabled (masked)
		1: All Interrupts on INT_Status2 enabled
CHG_TYP	1	0: Charger type detection disabled
		1: Charger type detection enabled
USB_DET_DIS	1	0: USB Detection Enabled
		1: USB Detection Disabled

4. SW_Control
Address: 03H

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
03	SW Control	R/W		MIC_ON	DP[2:0]			DM[2:0]		
Reset Value			X	0	See (1)			See (1)		

(1) The reset value depends on V_{BUS} status at power up. If V_{BUS} presents, the default value depends on DSS pin state (refer **Error! Reference source not found.** session). If V_{BUS} does not present, the default value is 111b (DM/DP switch is open)

NAME	SIZE (BITS)	DESCRIPTION
MIC_ON	1	0: MIC switching path open
		1: MIC switching path connected to ID line
DP	3	000: DP connected to USB_DP
		001: DP connected to UART_TX
		010: DP connected to AUDIO_R
		011: Future Use (right Audio for Video)
		100-111: DP switching path open
DM	3	000: DM connected to USB_DM
		001: DM connected to UART_RX
		010: DM connected to AUDIO_L
		011: Future Use (left Audio for Video)
		100-111: DM switching path open

5. INT_Status1
Address: 04H

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
04	INT_Status1	R	CHGDET	MR_COMP	SEND/END	VBUS	IDNO[3:0]			
Reset Value			0	0	0	0	See (1)			

(1) ADC value of the ID pin

NAME	SIZE (BITS)	DESCRIPTION
CHGDET	1	0: High Current Charger Not Detected
		1: High Current Dedicated Charger Detected. The dedicated charger has DP-DM short with less than 50Ω
MR_COMP	1	0: MIC removal comparator low
		1: MIC removal comparator high
SEND/END	1	0: ID line not grounded
		1: ID line grounded (Send/End button pressed)
VBUS	1	0: No power detected on VBUS
		1: Power detected on VBUS
IDNO	4	0000: ADC determined ID impedance = 0 ohms (grounded)
		0001: ADC determined ID impedance = 24 K-ohms
		0010: ADC determined ID impedance = 56 K-ohms
		0011: ADC determined ID impedance = 100 K-ohms
		0100: ADC determined ID impedance = 130 K-ohms
		0101: ADC determined ID impedance = 180 K-ohms
		0110: ADC determined ID impedance = 240 K-ohms
		0111: ADC determined ID impedance = 330 K-ohms
		1000: ADC determined ID impedance = 430 K-ohms
		1001: ADC determined ID impedance = 620 K-ohms
		1010: ADC determined ID impedance = 910 K-ohms
		1011: ADC determined ID impedance = open

6. INT_Status2
Address: 05H

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
05	INT_Status2	R							MR_COMP2	SEND/END2
Reset Value									N/A	N/A

NAME	SIZE (BITS)	DESCRIPTION
MR_COMP2	1	0: MIC removal comparator2 low
		1: MIC removal comparator2 high
SEND/END2	1	0: MIC line not grounded
		1: MIC line grounded (Send/End button pressed)

7. Status
Address: 06H

Address (xxh)	Name	TYPE	b7	b6	b5	b4	b3	b2	b1	b0
06	Status	R	DCPORT	CHPORT						TIMEOUT_CD
Reset Value			0	0	X	X	X	X	X	0

NAME	SIZE (BITS)	DESCRIPTION
DCPORT	1	0: No Dedicated charger detected
		1: Dedicated charger detected
CHPORT	1	0: No Charging host port detected
		1: Charging host port detected
TIMEOUT_CD	1	0: No timeout for DP/DM contact detection.
		1: Timeout occurred for DP/DM contact detection.

PARAMETER MEASUREMENT INFORMATION

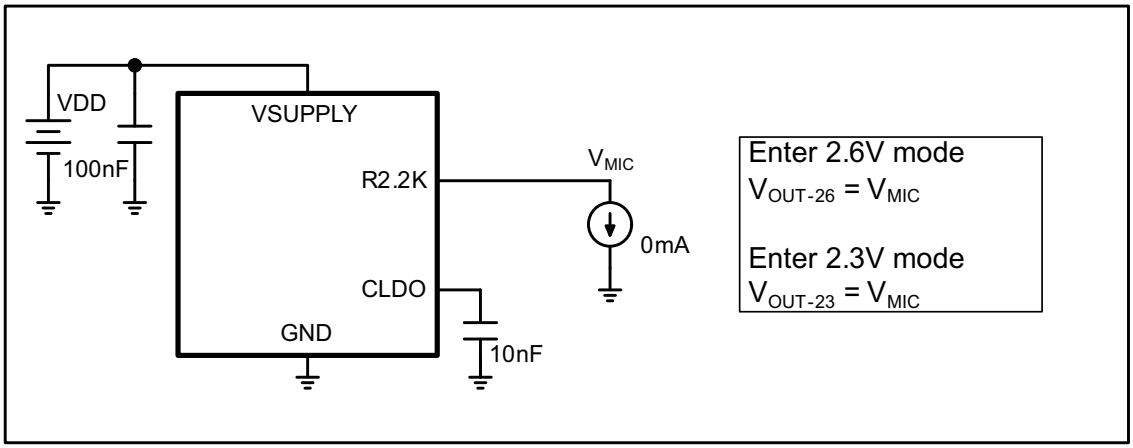


Figure 15. LDO Output Voltage

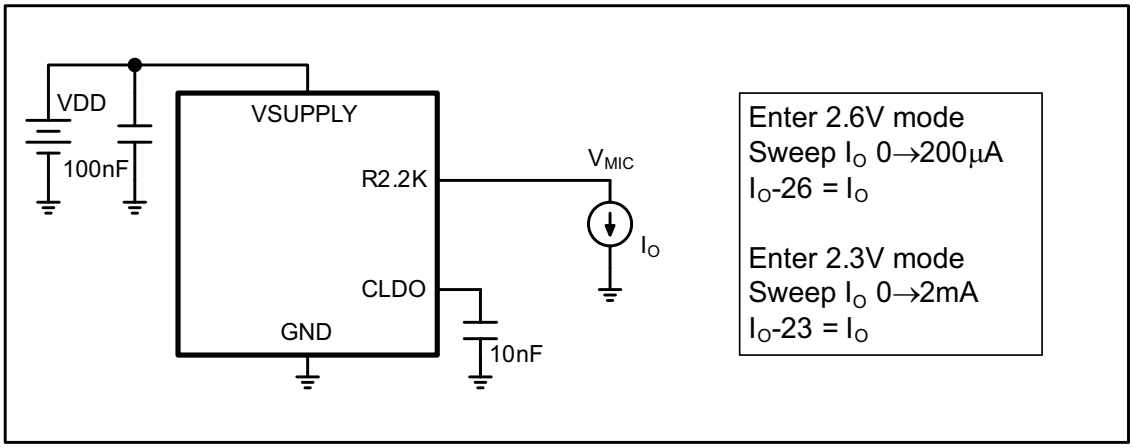


Figure 16. Max Output Current

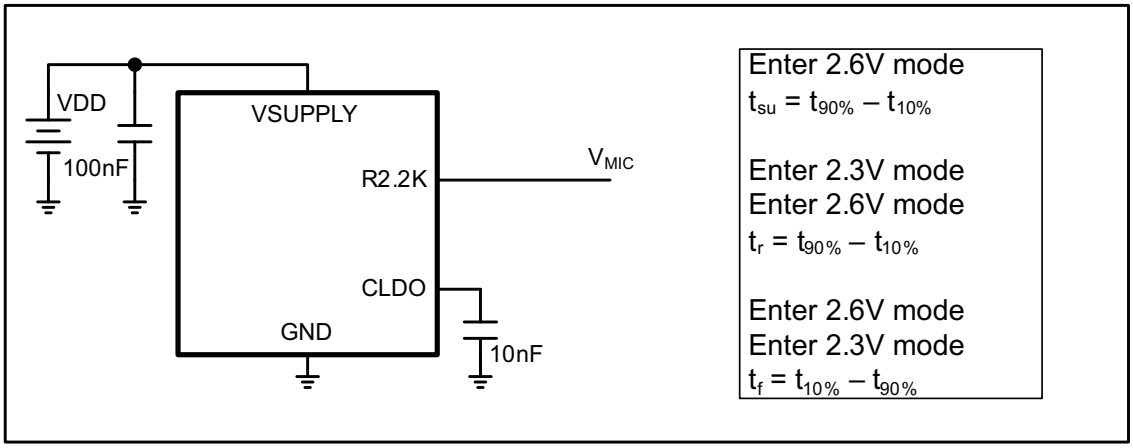


Figure 17. LDO Rise/Fall Time

PARAMETER MEASUREMENT INFORMATION (continued)

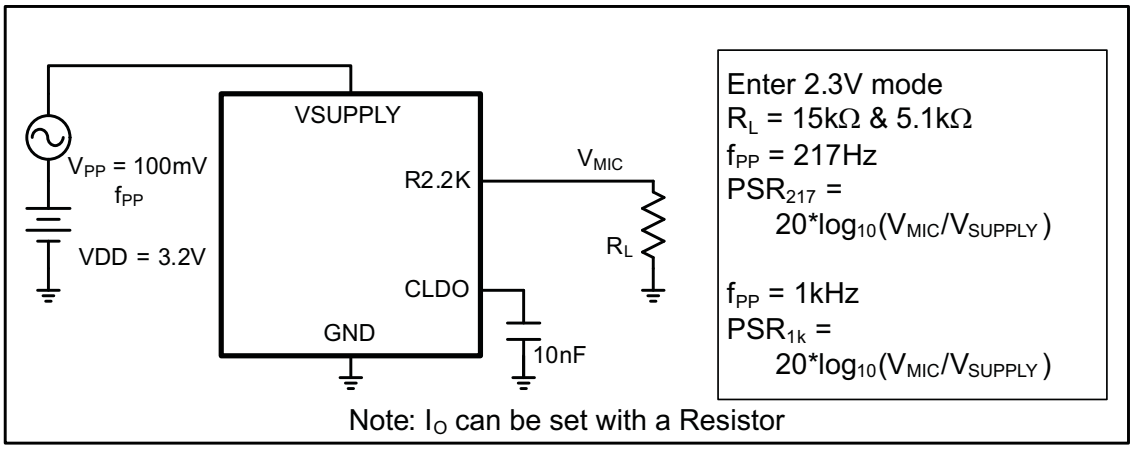


Figure 18. Power Supply Rejection

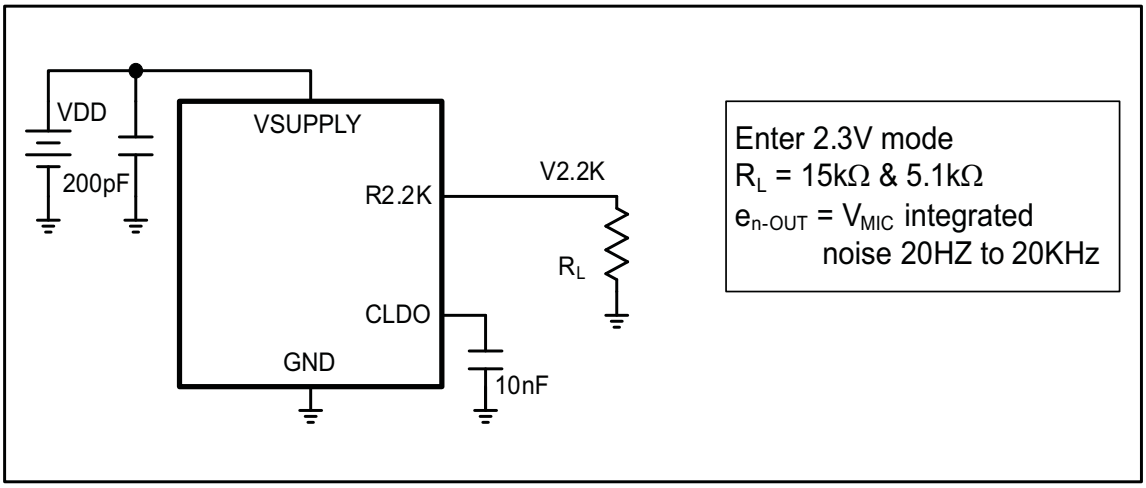


Figure 19. Integrated Output Noise

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU5611YZPR	ACTIVE	DSBGA	YZP	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

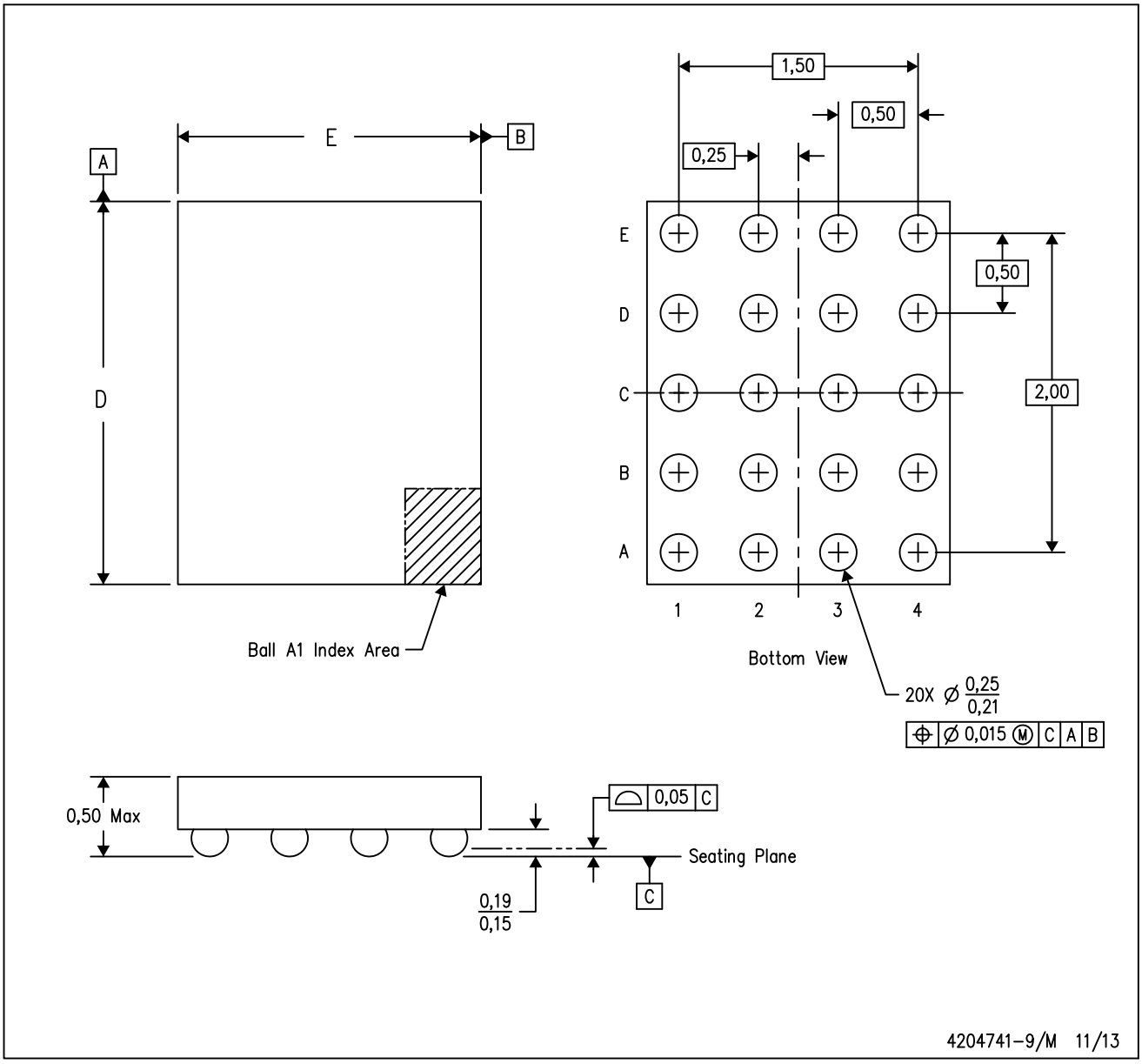
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YZP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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