

# TUSB217-Q1 USB 高速信号调节器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 2:
    - 40°C 至 105°C T<sub>A</sub>
- 宽电源电压范围: 2.3 - 6.5V
- 超低 USB 断开和关断功耗
- 可提供 USB 2.0 高速信号调节
- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 支持低速、全速和高速信号传输
- 主机/设备无关
- 支持长达 5m 的电缆
  - 通过外部下拉电阻器实现四种可选的信号增强（边沿升压与直流升压）设置
  - 通过上拉或下拉可配置引脚实现三种可选的 RX 灵敏度，以补偿高损耗应用中的 ISI 抖动
- 可扩展解决方案 - 用于高损耗应用的菊花链器件
- 与 TUSB213 (5V) 引脚兼容

## 2 应用

- 汽车信息娱乐系统
- 汽车音响主机
- 汽车媒体中心
- 笔记本电脑/台式计算机/扩展坞
- 平板电脑/手机
- 电视
- 有源电缆、电缆扩展器
- 背板

## 3 说明

TUSB217-Q1 是第三代 USB 2.0 高速信号调节器，旨在补偿传输通道中的交流损失（由于电容性负载）和直流损失（由于电阻性负载）。

TUSB217-Q1 采用了专利设计，可通过边缘加速器来对 USB 2.0 高速信号的传输边缘进行加速，并通过直流升压功能来提高静态电平。此外，TUSB217-Q1 还具有预均衡功能，可提高接收器的灵敏度并补偿较长线缆应用中的 ISI 抖动。USB 低速和全速信号特征不受 TUSB217-Q1 的影响。

TUSB217-Q1 可在不改变数据包计时或增加传播延迟的情况下提高信号质量，是需要低延迟的应用的理想选择。

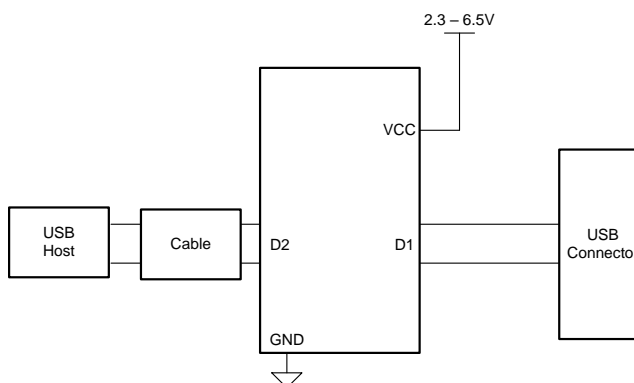
TUSB217-Q1 可使用长达 5 米的线缆帮助系统通过 USB 2.0 高速电气近端眼图合规性测试。

TUSB217-Q1 与 USB On-The-Go (OTG) 和电池充电 (BC 1.2) 协议兼容。

### 器件信息

器件编号	封装	封装尺寸 (标称值)
TUSB217-Q1	VQFN (14)	3.50mm x 3.50mm

### 简化原理图



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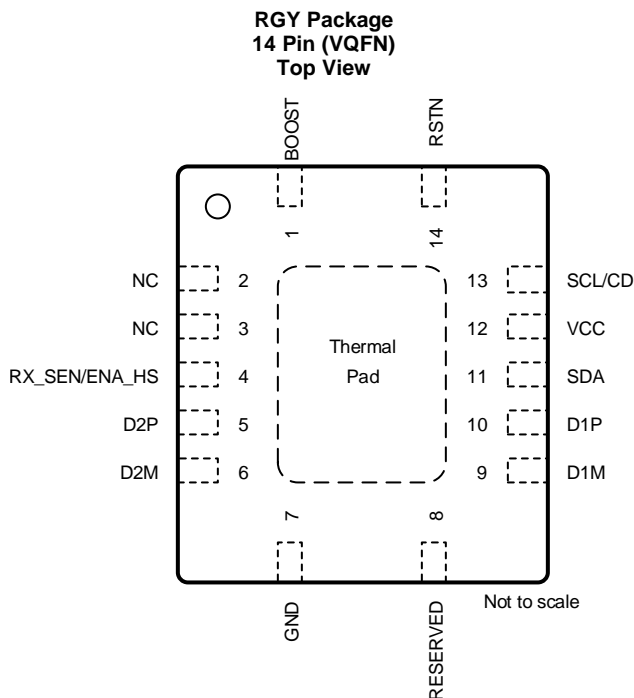
## 4 修订历史记录

### Changes from Original (September 2018) to Revision A

**Page**

- |                              |          |
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| • 将文档状态从 预告信息 更改为 生产数据 ..... | <b>1</b> |
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
BOOST	1	I	N/A	USB High Speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
NC	2,3	I		Leave unconnected
RESERVED	8	O		Leave unconnected or connect a decoupling cap 0.1µF
RX_SEN <sup>(1)</sup> /ENA_HS	4	I/O	N/A	In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High Speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) – high RX sensitivity (high loss channel) M (pin is left floating) – medium RX sensitivity (medium loss channel) L (pin is pulled low) – low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].
D2P	5	I/O	N/A	USB High Speed positive port.
D2M	6	I/O	N/A	USB High Speed negative port.
GND	7	P	N/A	Ground
D1M	9	I/O	N/A	USB High Speed negative port..
D1P	10	I/O	N/A	USB High Speed positive port.

(1) Pull-down and pull-up resistors for RX\_SEN pin must follow  $R_{RXSEN1}$  and  $R_{RXSEN2}$  resistor recommendations in non I<sup>2</sup>C mode.

**Pin Functions (continued)**

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO. (RGY)			
SDA <sup>(2)</sup>	11	I/O	500 kΩ PU 1.8 MΩ PD	I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
VCC	12	P	N/A	Supply power
RSTN	14	I	500 kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-μF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
SCL <sup>(2)/CD</sup>	13	I/O	When RSTN asserted there is a 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
Thermal Pad	TPAD	N/A	N/A	Thermal Pad is electrically not connected to device ground. Connection to board ground is optional.

- (2) Pull-up resistors for SDA and SCL pins in I<sup>2</sup>C mode should be R<sub>Pull-up</sub> (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I<sup>2</sup>C mode.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VCC	-0.3	7	V
Voltage range USB data	DxP, DxM	-0.3	5.5	V
Voltage range on BOOST pin	BOOST	-0.3	1.98	V
Voltage range other pins	SCL, SDA, RX_SEN, RSTN	-0.3	5	V
Storage temperature, T <sub>stg</sub>		-65	150	°C
Maximum junction temperature, T <sub>J(max)</sub>			125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4A	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5	6.5	V
T <sub>A</sub>	Operating free-air temperature (AEC-Q100)	-40		105	°C
T <sub>J</sub>	Junction temperature (AEC-Q100)			115	°C
V <sub>I2C_BUS</sub>	I2C Bus Voltage	1.62		3.6	V

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
SCL, SDA, RX_SEN, RSTN	Voltage range other pins (SCL, SDA, RX_SEN, RSTN)	0		3.6	V

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RGY (VQFN)	UNIT
		14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	49.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	52.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	24.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	24.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>POWER</b>						
I <sub>ACTIVE_HS</sub>	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V <sub>CC</sub> supply stable, with Boost = Max		22	36	mA
I <sub>IDLE_HS</sub>	High Speed Idle Current	USB channel = HS mode, no traffic. V <sub>CC</sub> supply stable, Boost = Max		22	36	mA
I <sub>HS_SUSPEND</sub>	High Speed Suspend Current	USB channel = HS Suspend mode. V <sub>CC</sub> supply stable		0.75	1.4	mA
I <sub>FS</sub>	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V <sub>CC</sub> supply stable		0.75	1.4	mA
I <sub>DISCONN</sub>	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I <sub>SHUTDOWN</sub>	Shutdown Power	RSTN driven low, V <sub>CC</sub> supply stable		35	95	µA
<b>CONTROL PIN LEAKAGE</b>						
I <sub>LKG_FS</sub>	Pin failsafe leakage current for SDA, RSTN	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>		10	15	µA
I <sub>LKG_FS</sub>	Pin failsafe leakage current for BOOST, RX_SEN	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>		6	10	µA
I <sub>LKG_FS</sub>	Pin failsafe leakage current for SCL	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>			70	nA
<b>INPUT RSTN</b>						
V <sub>IH</sub>	High level input voltage		1.5		3.6	V
V <sub>IL</sub>	Low-level input voltage		0		0.5	V
I <sub>IH</sub>	High level input current	V <sub>IH</sub> = 3.6 V, R <sub>PU</sub> enabled			±15	µA
I <sub>IL</sub>	Low level input current	V <sub>IL</sub> = 0V, R <sub>PU</sub> enabled			±20	µA
<b>INPUT RX_SEN (3-level input, for mid level leave pin floating)</b>						
V <sub>IH</sub>	High level input voltage R <sub>RXSEN1</sub> =47kΩ, R <sub>RXSEN2</sub> =10kΩ	V <sub>CC</sub> <=4.3V	1.8		3.6	V
V <sub>IH</sub>	High level input voltage R <sub>RXSEN1</sub> =37kΩ, R <sub>RXSEN2</sub> =47kΩ	V <sub>CC</sub> >4.3V	2.0		3.6	V

(1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IL</sub>	Low level input voltage 22kΩ ≤ R <sub>RXSEN1</sub> ≤ 33kΩ				0.4	V
<b>INPUT BOOST</b>						
R <sub>BOOST_LVL0</sub>	External pulldown resistor for BOOST Level 0				160	Ω
R <sub>BOOST_LVL1</sub>	External pulldown resistor for BOOST Level 1		1.5	1.8	2	kΩ
R <sub>BOOST_LVL2</sub>	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	kΩ
R <sub>BOOST_LVL3</sub>	External pulldown resistor for BOOST Level 3		7.5			kΩ
<b>OUTPUTS CD, ENA_HS</b>						
V <sub>OH</sub>	High level output voltage	I <sub>O</sub> = -50 μA, V <sub>CC</sub> ≥ 3.0V	2.5			V
V <sub>OH</sub>	High level output voltage	I <sub>O</sub> = -50 μA, V <sub>CC</sub> = 2.3V	1.8			V
V <sub>OL</sub>	Low level output voltage	I <sub>O</sub> = 50 μA			0.3	V
<b>I2C</b>						
C <sub>I2C_BUS</sub>	I <sup>2</sup> C Bus Capacitance		4		150	pF
I <sub>OL</sub>	I <sup>2</sup> C open drain output current	V <sub>OL</sub> = 0.4V	1.5			mA
V <sub>IL</sub>	V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IL</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IH</sub>	V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>	75			%
V <sub>IH</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>	75			%
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 1.8V +/-10%		1.6	2	2.5	kΩ
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%		2.8	4.7	7	kΩ
SCL Frequency					100	kHz
<b>DxP, DxM</b>						
C <sub>IO_DXX</sub>	Capacitance to GND	Measured with VNA at 240 MHz, V <sub>CC</sub> supply stable, Redriver off		2.5		pF

## 6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DxP, DxM USB Signals</b>						
F <sub>BR_DXX</sub>	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V <sub>CC</sub> supply stable			480	Mbps
t <sub>R/F_DXX</sub>	Rise/Fall time		100			ps

 (1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### 6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>POWER UP TIMING</b>					
$T_{RSTN\_PW}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			$\mu s$
$T_{STABLE}$	VCC must be stable before RSTN de-assertion	300			$\mu s$
$T_{READY}$	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	$\mu s$
$T_{RAMP}$	VCC ramp time	0.2		100	ms
<b>I2C (STD)</b>					
$t_{SUSTO}$	Stop setup time, SCL ( $T_r=600ns-1000ns$ ), SDA ( $T_f=6.5ns-106.5ns$ ), 100kHz STD	4			$\mu s$
$t_{HDSTA}$	Start hold time, SCL ( $T_r=600ns-1000ns$ ), SDA ( $T_f=6.5ns-106.5ns$ ), 100kHz STD	4			$\mu s$
$t_{SUSTA}$	Start setup time, SCL ( $T_r=600ns-1000ns$ ), SDA ( $T_f=6.5ns-106.5ns$ ), 100kHz STD	4.7			$\mu s$
$t_{SUDAT}$	Data input or False start/stop, setup time, SCL ( $T_r=600ns-1000ns$ ), SDA ( $T_f=6.5ns-106.5ns$ ), 100kHz STD	250			ns
$t_{HDDAT}$	Data input or False start/stop, hold time, SCL ( $T_r=600ns-1000ns$ ), SDA ( $T_f=6.5ns-106.5ns$ ), 100kHz STD	5			$\mu s$
$t_{BUF}$	Bus free time between START and STOP conditions	4.7			$\mu s$
$t_{LOW}$	Low period of the I2C clock	4.7			$\mu s$
$t_{HIGH}$	High period of the I2C clock	4			$\mu s$
$t_F$	Fall time of both SDA and SCL signals			300	ns
$t_R$	Rise time of both SDA and SCL signals			1000	ns

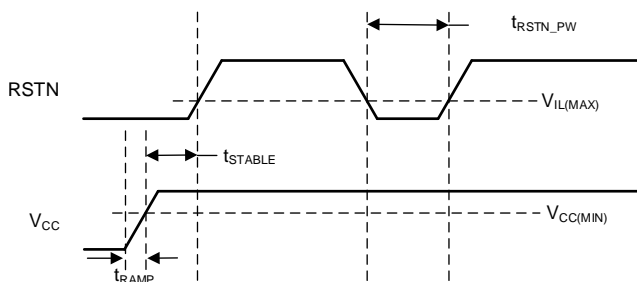


图 1. Power On and Reset Timing

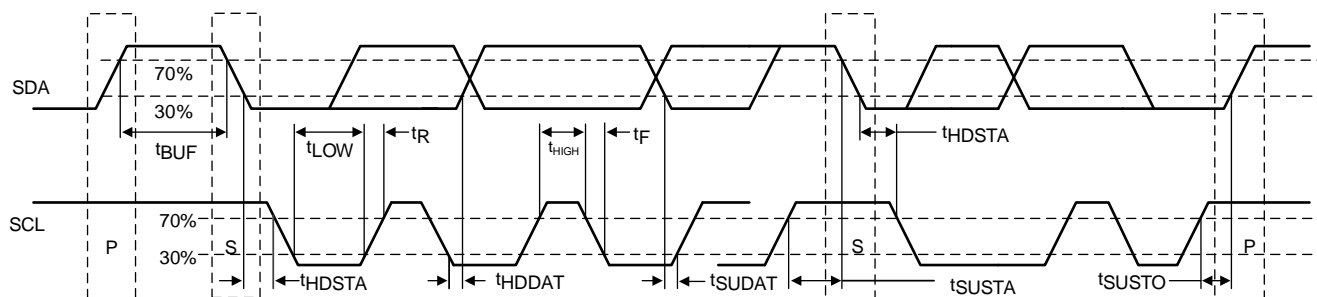


图 2. I2C Timing

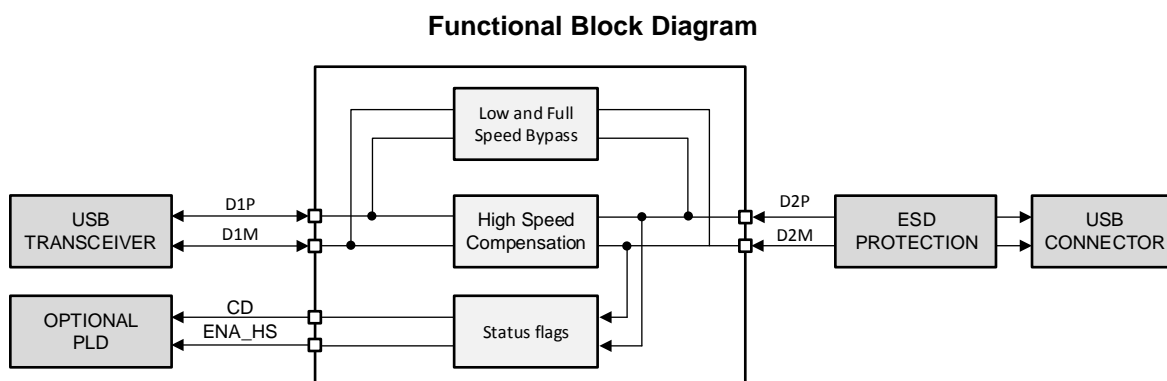
## 7 Detailed Description

### 7.1 Overview

The TUSB217-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB217-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB217-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 High speed boost

The high speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set via I<sup>2</sup>C register according to [I<sup>2</sup>C mode](#). Internal circuitry of the signal conditioner reduces possible overshoot.

#### 7.3.2 RX Sensitivity

The RX\_SEN pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

### 7.4 Device Functional Modes

#### 7.4.1 Low Speed (LS) mode

TUSB217-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low.

#### 7.4.2 Full Speed (FS) mode

TUSB217-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low



## Device Functional Modes (接下页)

### 7.4.3 High Speed (HS) mode

TUSB217-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX\_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA\_HS pin are asserted high when high speed boost is active.

### 7.4.4 High Speed downstream port electrical compliance test mode

TUSB217-Q1 will detect HS compliance test fixture and enter downstream port high speed eye diagram test mode. CD pin will be low and ENA\_HS pin is asserted high when TUSB217-Q1 is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB217-Q1 is operating in HS functional mode, TUSB217-Q1 will transition to HS eye compliance test mode and CD asserts low and ENA\_HS remains high. When this occurs signal compensation is enabled.

### 7.4.5 Shutdown mode

TUSB217-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

**表 1. CD and ENA\_HS Pins in Different Modes**

MODE	CD	ENA_HS
Low speed	HIGH	LOW
Full speed	HIGH	LOW
High speed	HIGH	HIGH
High speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

### 7.4.6 I<sup>2</sup>C mode

TUSB217-Q1 supports 100 KHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification 2.1, 2001 – STANDARD MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG\_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high speed mode.

## 7.5 TUSB217 Registers

[Table 2](#) lists the memory-mapped registers for the TUSB217 registers. All register offset addresses not listed in [Table 2](#) should be considered as reserved locations and the register contents should not be modified.

**Table 2. TUSB217 Registers**

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	<a href="#">Go</a>
0x3	CONFIGURATION	This register is selecting device mode.	<a href="#">Go</a>
0xE	DC_BOOST	This register is setting DC BOOST level.	<a href="#">Go</a>
0x25	RX_SEN	This register is setting RX Sensitivity level.	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 3](#) shows the codes that are used for access types in this section.

**Table 3. TUSB217 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
RH	H R	Set or cleared by hardware Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

### 7.5.1 EDGE\_BOOST Register (Offset = 0x1) [reset = X]

EDGE\_BOOST is shown in [Figure 3](#) and described in [Table 4](#).

Return to [Summary Table](#).

This register is setting EDGE BOOST level.

**Figure 3. EDGE\_BOOST Register**

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

**Table 4. EDGE\_BOOST Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting) 0x3 = BOOST PIN LEVEL 1 0x6 = BOOST PIN LEVEL 2 0x8 = BOOST PIN LEVEL 3 0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

### 7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in [Figure 4](#) and described in [Table 5](#).

Return to [Summary Table](#).

This register is selecting device mode.

**Figure 4. CONFIGURATION Register**

7	6	5	4	3	2	1	0
RESERVED						CFG_ACTIVE	
RH/W-X						RH/W-0x1	

**Table 5. CONFIGURATION Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

**Table 5. CONFIGURATION Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode.  0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

### 7.5.3 DC\_BOOST Register (Offset = 0xE) [reset = X]

DC\_BOOST is shown in [Figure 5](#) and described in [Table 6](#).

Return to [Summary Table](#).

This register is setting DC BOOST level.

**Figure 5. DC\_BOOST Register**

7	6	5	4	3	2	1	0
RESERVED				DCB_LVL			
RH/W-X				RH/W-X			

**Table 6. DC\_BOOST Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range  0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting) 0x2 = BOOST PIN LEVEL 1 and 2 0x6 = BOOST PIN LEVEL 3 0xF = (highest dc boost setting)

### 7.5.4 RX\_SEN Register (Offset = 0x25) [reset = X]

RX\_SEN is shown in [Figure 6](#) and described in [Table 7](#).

Return to [Summary Table](#).

This register is setting RX Sensitivity level.

**Figure 6. RX\_SEN Register**

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

**Table 7. RX\_SEN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range  0x0 = RX_SEN LEVEL LOW 0x44 = RX_SEN LEVEL MID 0x77 = RX_SEN LEVEL HIGH 0xFF = (highest setting)

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

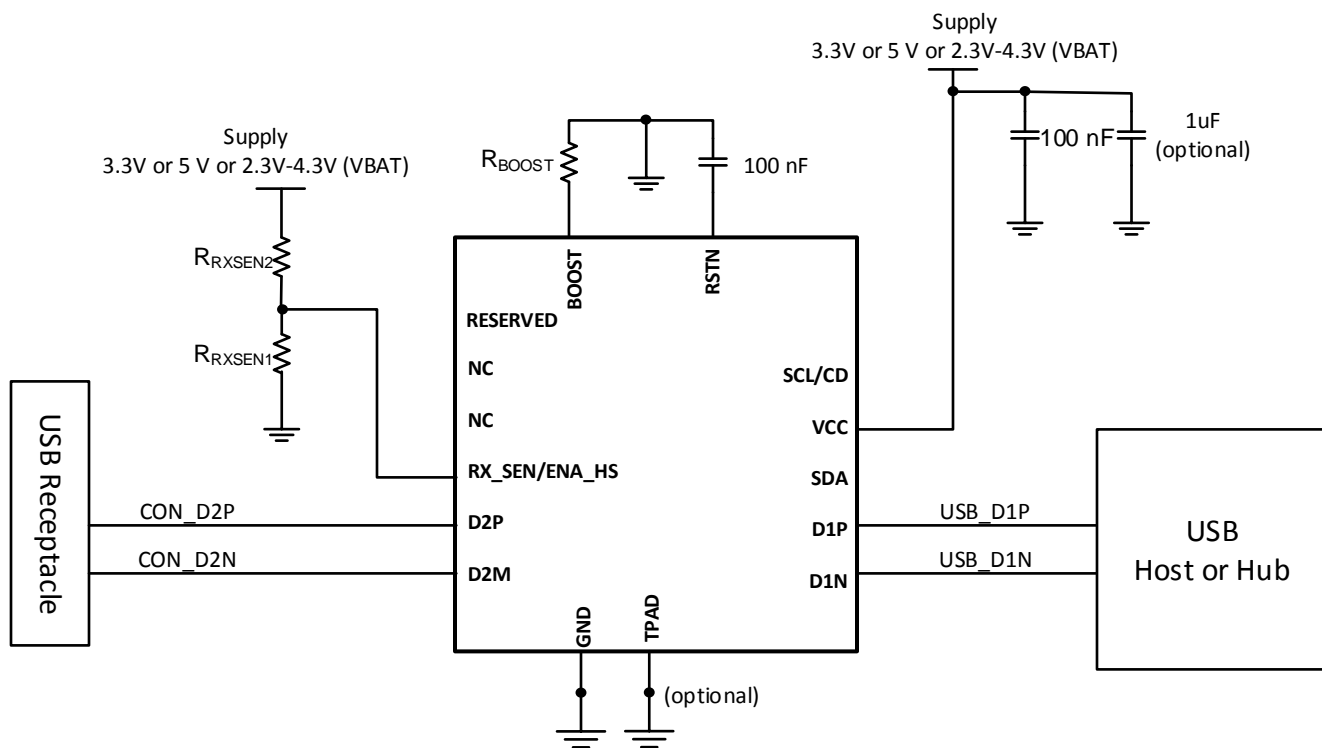
### 8.1 Application Information

The purpose of the TUSB217-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB217-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB217-Q1 to control other blocks on the customer platform, if so desired.

### 8.2 Typical Application

A typical application is shown in [图 7](#). In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



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**图 7. Reference Schematic (design example)**

## Typical Application (接下页)

### 8.2.1 Design Requirements

TUSB217-Q1 requires a valid reset signal as described in the *power supply recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in [表 8](#), [表 9](#) and [表 10](#)

**表 8. Design Parameters for 5 V Supply with High Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				5 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>		<b>BOOST Level</b>	Boost Level 1: R <sub>BOOST</sub> = 1.8 kΩ
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
Do Not Install (DNI)		3		
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	High RX Sensitivity Level: R <sub>RXSEN1</sub> = 37 kΩ R <sub>RXSEN2</sub> = 47 kΩ
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 kΩ <sup>(2)</sup>	47 kΩ	High	

- (1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 5V supply system could be applicable to 3.3V supply system as well.
- (2) This resistor is needed for a 5V supply to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

**表 9. Design Parameters for 3.3 V Supply with Low to Medium Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				3.3 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>		<b>BOOST Level</b>	Boost Level 0: R <sub>BOOST</sub> = 0-Ω
	0-Ω		0	
	1.8 kΩ ±1%		1	
	3.6 kΩ ±1%		2	
Do Not Install (DNI)		3		
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	Medium RX Sensitivity Level: R <sub>RXSEN1</sub> = DNI R <sub>RXSEN2</sub> = DNI
	22 kΩ - 33 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ - 33 kΩ (27 kΩ typical)	High	

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system could be applicable to 5V supply system as well.

**表 10. Design Parameters for 2.3V - 4.3V VBAT Supply with Low to Medium Loss System**

PARAMETER				VALUE <sup>(1)</sup>
$V_{CC}$				2.3 V to 4.3V
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost		$R_{BOOST}$	<b>BOOST Level</b>	Boost Level 0: $R_{BOOST} = 0-\Omega$
		0- $\Omega$	0	
		1.8 k $\Omega$ $\pm$ 1%	1	
		3.6 k $\Omega$ $\pm$ 1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	$R_{RXSEN1}$	$R_{RXSEN2}$	<b>RX_SEN Level</b>	Medium RX Sensitivity Level: $R_{RXSEN1} = DNI$ $R_{RXSEN2} = DNI$
	22 k $\Omega$ - 33 k $\Omega$ (27 k $\Omega$ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37 k $\Omega$ <sup>(2)</sup>	10 k $\Omega$	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 2.3V-4.3V supply system could be applicable to 5V supply system as well.

(2) This resistor is needed for a VBAT supply (2.3V - 4.3V) to divide the voltage down so the BOOST pin voltage does not exceed 3.6V

### 8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. if permissible. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level 1.

In order for the TUSB217-Q1 to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

#### 注

The TUSB217-Q1 compensates for extra attenuation in the signal path according to the configuration of the RX\_SEN pin. This pin is not 5 V tolerant and therefore when selecting the highest RX sensitivity level, the voltage level at RX\_SEN pin must be less than 3.6V.

Placement of the device is also dependent on the application goal. 表 11 summarizes our recommendations.

**表 11. Platform Placement Guideline**

PLATFORM GOAL	SUGGESTED TUSB217-Q1 PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB217s to improve device enumeration	Midway between each USB interconnect

**表 12. Table of Recommended Settings**

BOOST and RX_SEN settings <sup>(1)</sup> for channel loss		
Pre-channel cable length (Between USB PHY and TUSB217-Q1)	BOOST	RX_SEN
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB217-Q1 and inter-connect)	BOOST	RX_SEN
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host and/or device as well as cable length and loss profile.

### 8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

---

#### 注

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

---

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

#### 8.2.2.1.1 For a Host Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB217-Q1
4. Enable the host to transmit USB TEST\_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

#### 8.2.2.1.2 For a Device Side Application

1. Configure the TUSB217-Q1 to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217-Q1
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB217-Q1. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST\_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB217-Q1 with a different BOOST setting (must reset to change)

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8.2.3 Application Curves

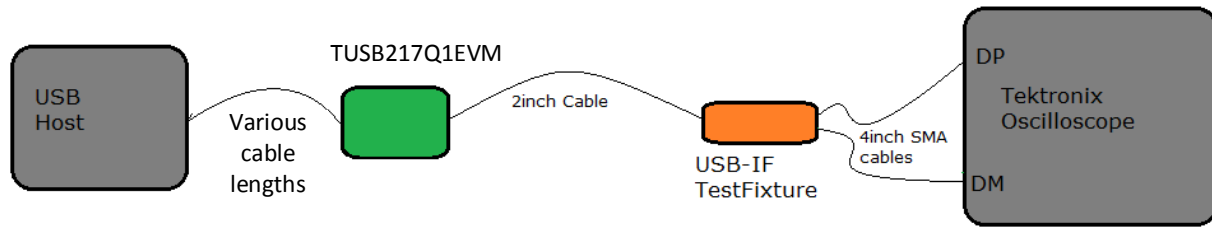


图 8. Near End Eye Measurement Set up With Pre-channel Cable

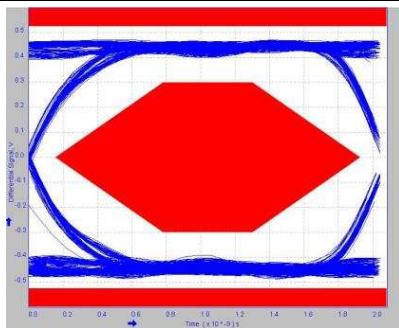


图 9. 6 inches without TUSB217-Q1

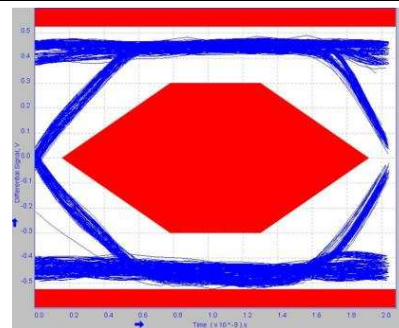


图 10. 6 inches pre-channel with TUSB217-Q1 BOOST=0 RX\_SEN=MED

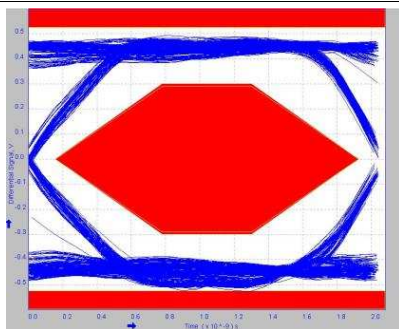


图 11. 6 inches pre-channel with TUSB217-Q1 BOOST=0 RX\_SEN=HIGH

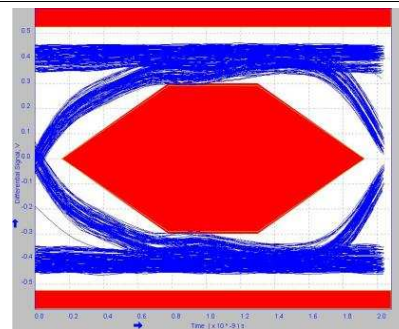


图 12. 3 meter without TUSB217-Q1



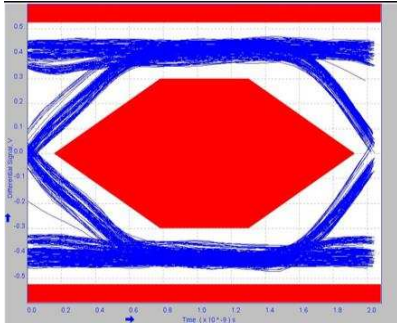


图 13. 3 meter pre-channel with TUSB217-Q1 BOOST=0  
RX\_SEN=MED

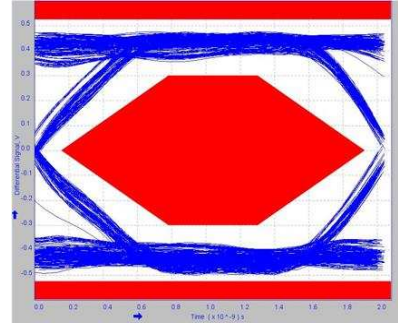


图 14. 3 meter pre-channel with TUSB217-Q1 BOOST=0  
RX\_SEN=HIGH

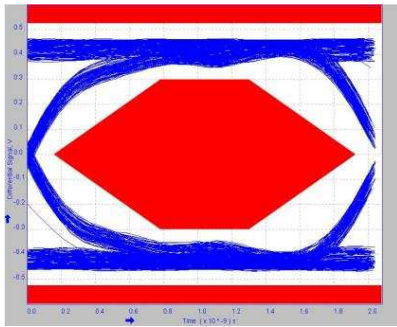


图 15. 2 meter without TUSB217-Q1

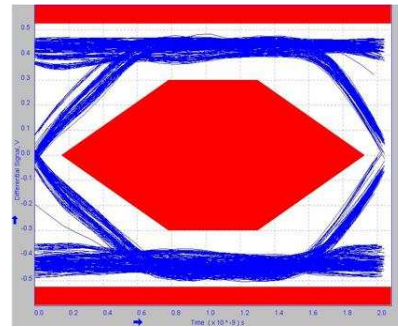


图 16. 2 meter pre-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=MED

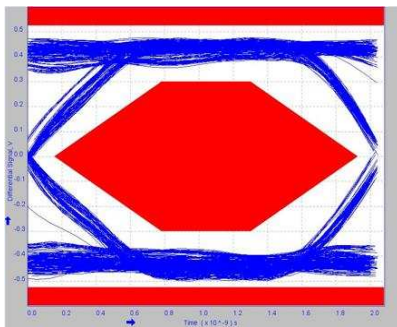


图 17. 2 meter pre-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=HIGH

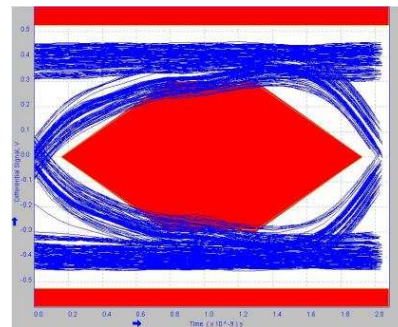
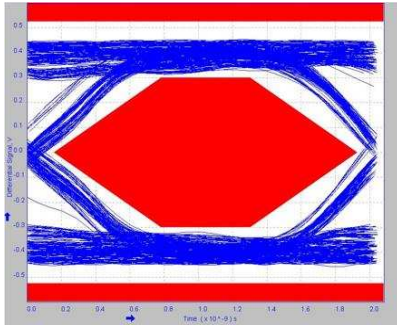


图 18. 5 meter without TUSB217-Q1

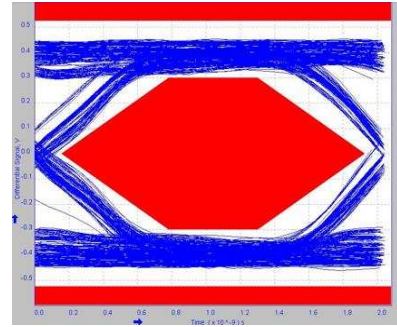
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**图 19. 5 meter pre-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=MED**



**图 20. 5 meter pre-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=HIGH**

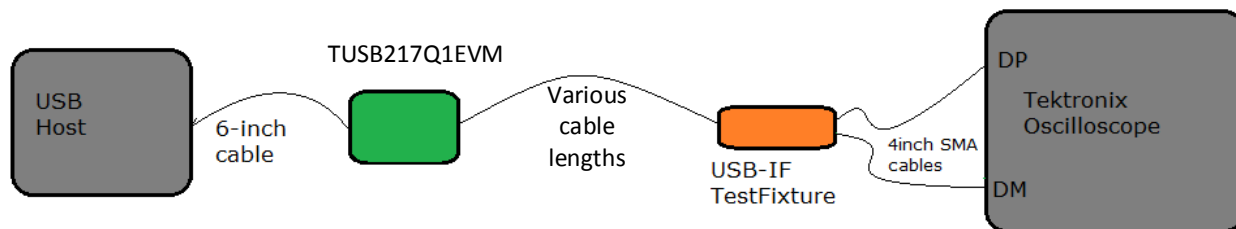


图 21. Near end eye measurement set up with post-channel cable

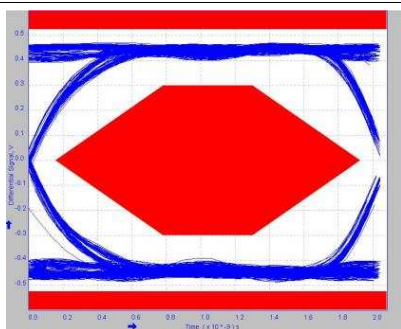


图 22. 6 inches without TUSB217-Q1

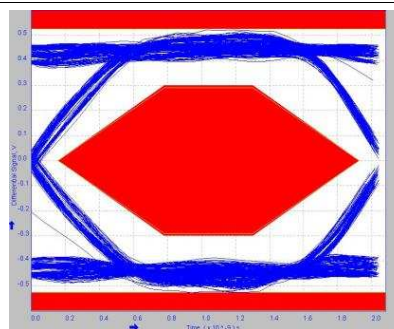


图 23. 6 inches post-channel with TUSB217-Q1 BOOST=0 RX\_SEN=MED

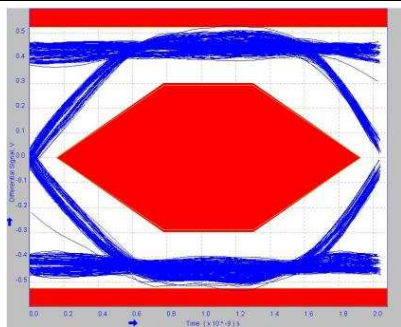


图 24. 6 inches post-channel with TUSB217-Q1 BOOST=0 RX\_SEN=HIGH

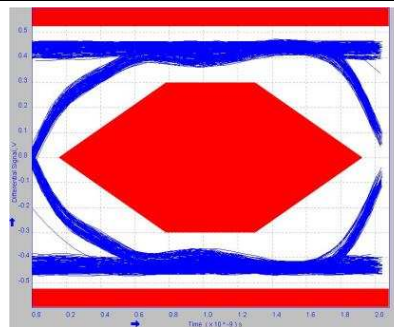


图 25. 1 meter without TUSB217-Q1

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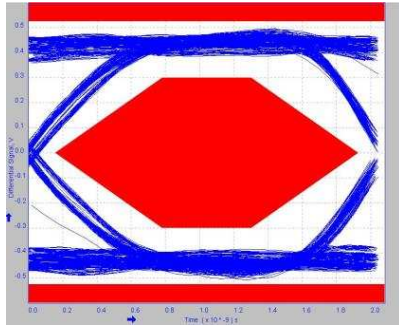


图 26. 1 meter post-channel with TUSB217-Q1 BOOST=0 RX\_SEN=MED

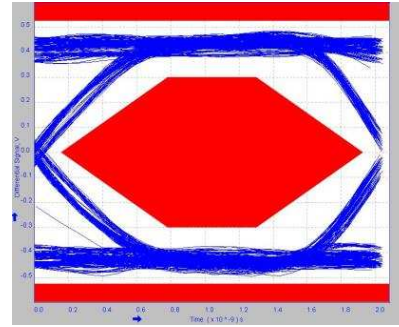


图 27. 1 meter post-channel with TUSB217-Q1 BOOST=0 RX\_SEN=HIGH

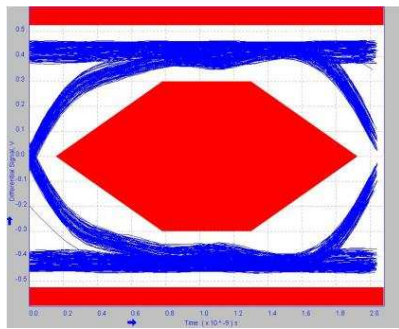


图 28. 2 meter without TUSB217-Q1

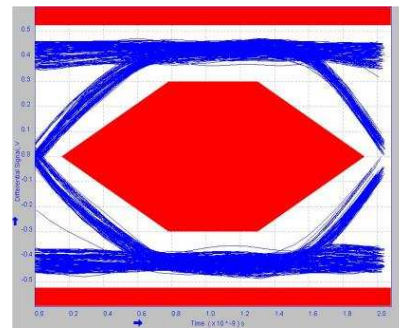


图 29. 2 meter post-channel with TUSB217-Q1 BOOST=1 RX\_SEN=MED

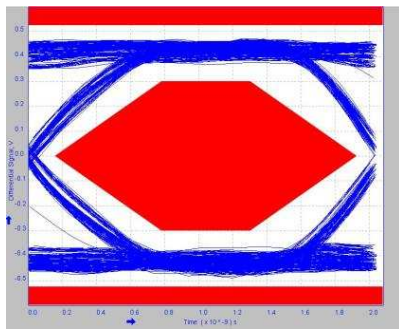


图 30. 2 meter post-channel with TUSB217-Q1 BOOST=1 RX\_SEN=HIGH

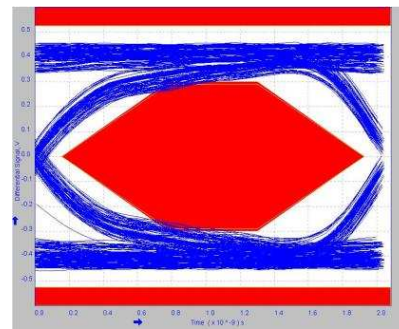


图 31. 4 meter without TUSB217-Q1

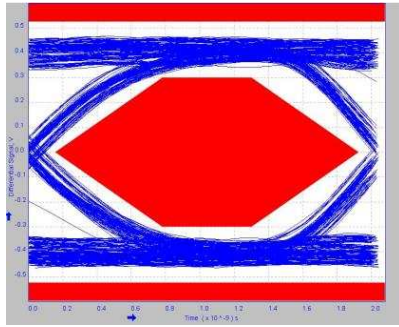


图 32. 4 meter post-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=MED

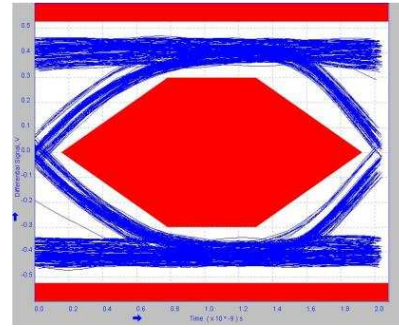


图 33. 4 meter post-channel with TUSB217-Q1 BOOST=1  
RX\_SEN=HIGH

## 9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to  $V_{CC}$ ). With a typical internal pullup resistance of 500 k $\Omega$ , the recommended minimum external capacitance is calculated as:

$$[\text{Ramp Time} \times 5] \div [500 \text{ k}\Omega] \quad (1)$$



## 10 Layout

### 10.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90  $\Omega$  differential routing underneath the device.

All dimensions are in millimetres (mm).

### 10.2 Layout Example

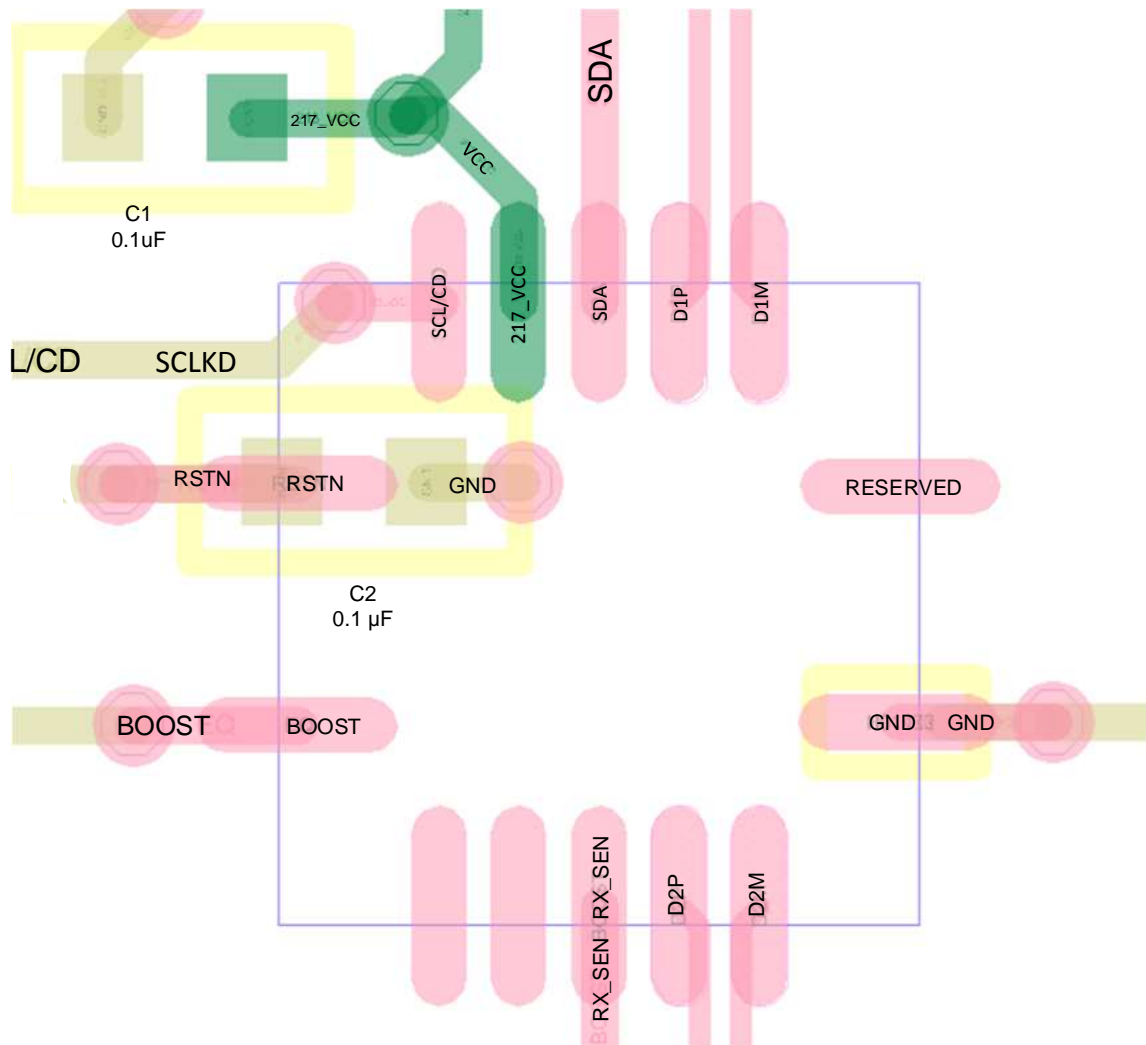


图 34. Layout Example (thermal pad grounding is optional)

## 11 器件和文档支持

### 11.1 文档支持

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.4 商标

E2E is a trademark of Texas Instruments.

### 11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



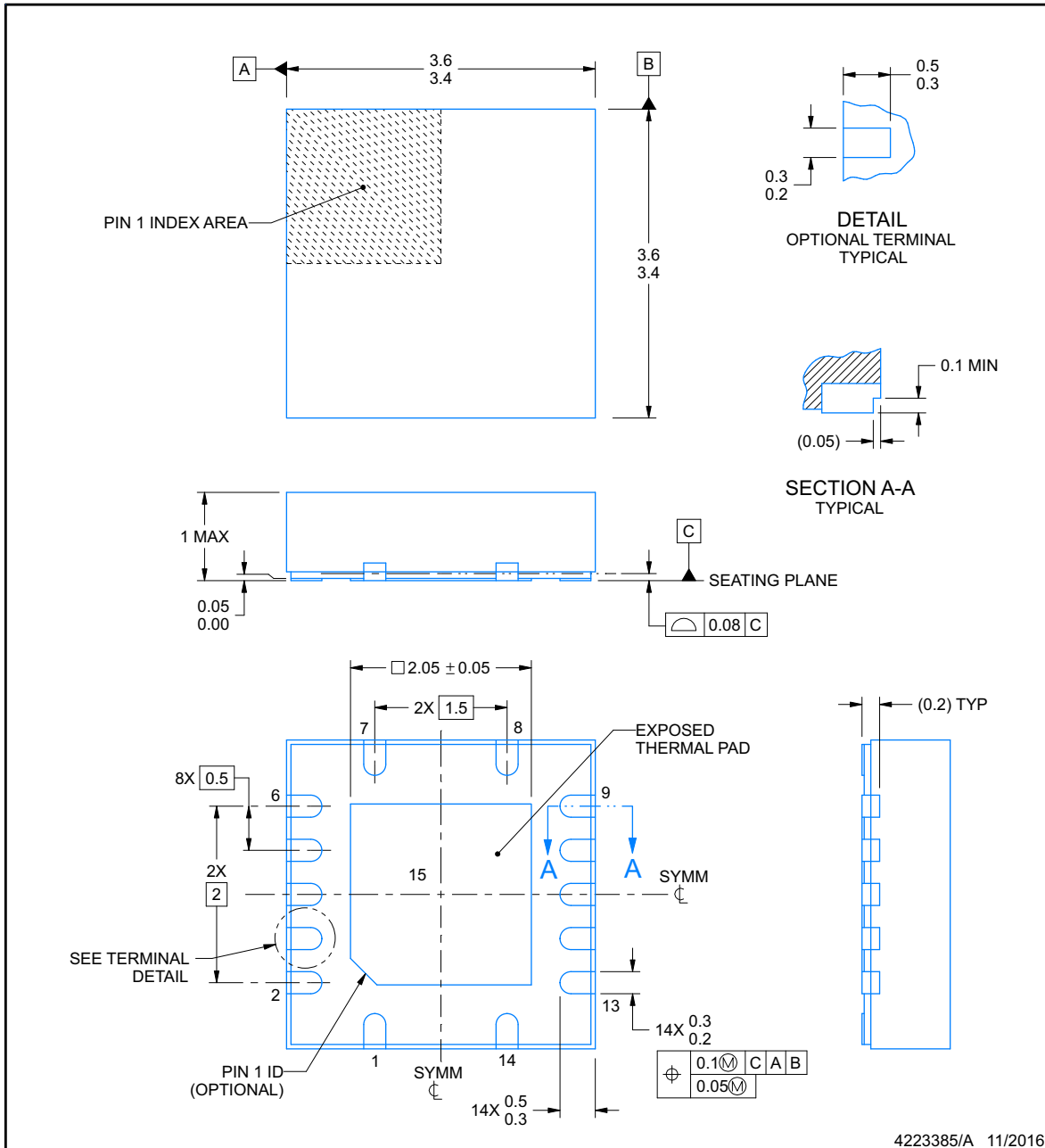


**RGY0014B**

**PACKAGE OUTLINE**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

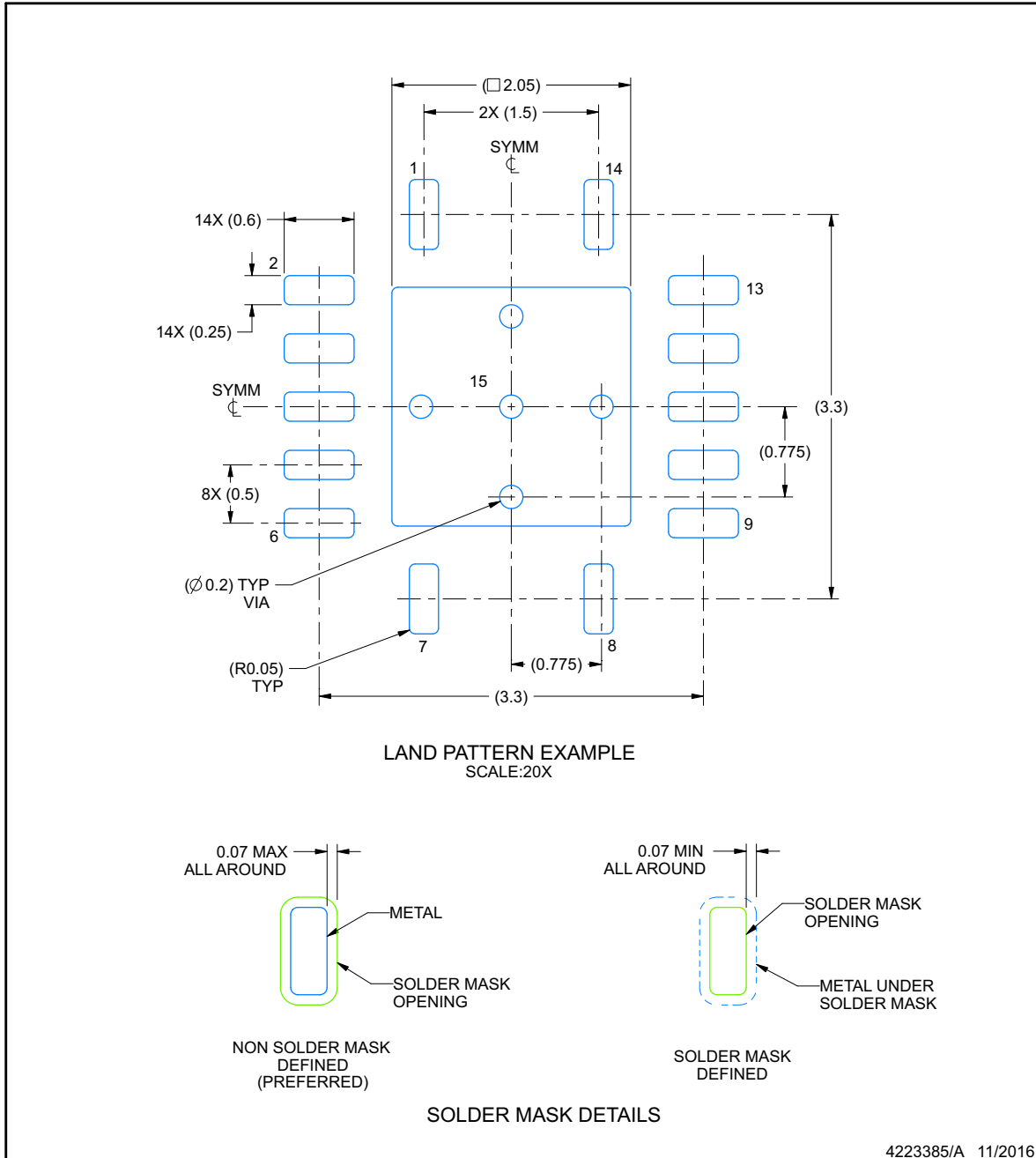
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT**

**RGY0014B**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

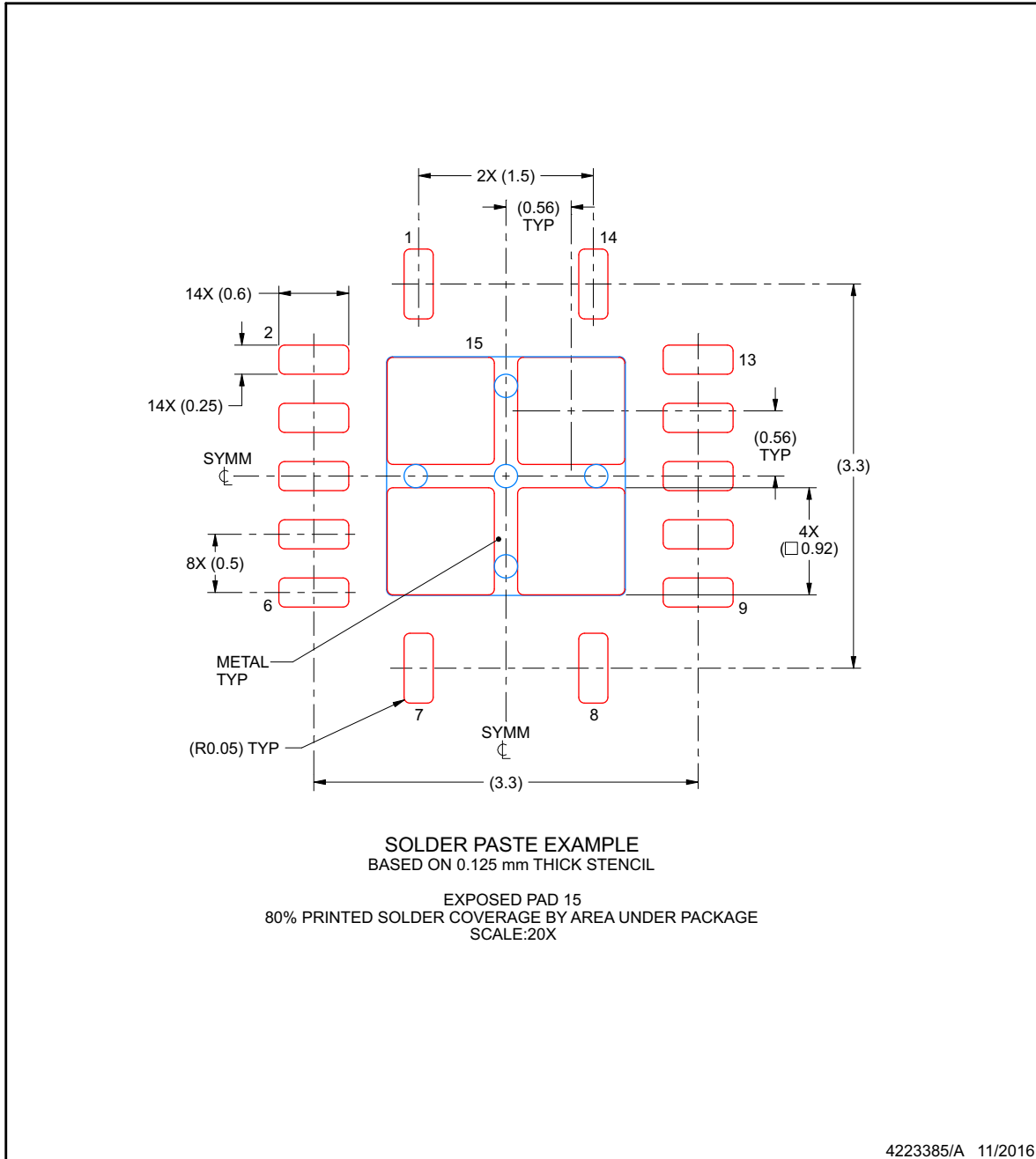
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB217RGYRQ1	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1	<a href="#">Samples</a>
TUSB217RGYTQ1	ACTIVE	VQFN	RGY	14	250	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	U217Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB217RGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB217RGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TUSB217RGYTQ1	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB217RGYRQ1	VQFN	RGY	14	3000	367.0	367.0	35.0
TUSB217RGYRQ1	VQFN	RGY	14	3000	367.0	367.0	38.0
TUSB217RGYTQ1	VQFN	RGY	14	250	210.0	185.0	35.0

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