TUSB9261 USB 3.0 至 SATA 桥接器

1 特性

- 通用串行总线 (USB)
  - 符合超高速 USB 3.0 标准 – TID 340730020
    - 集成收发器支持超高速 (SS)/高速 (HS)/快速 (FS) 信令
  - 同类产品中最佳的自适应均衡器
    - 可使接收器获得更高的抖动容差
  - USB 类别支持
    - USB 连接 SCSI 协议 (UASP)
    - USB 海量存储设备类仅批量传输 (BOT)
    - 支持 13 种错误情况（BOT 规范中定义）
    - USB 引导支持
    - USB 人机接口设备 (HID)
  - 支持使用 TI 提供的应用程序通过 USB 进行固件更新
- 串行高级技术附件 (SATA) 接口
  - 串行 ATA 规范版本 2.6
    - Gen1i、Gen1m、Gen2i 和 Gen2m
  - 支持与 ATA/ATAPI-8 规范兼容的海量存储设备
- 集成 ARM Cortex M3 内核
  - 通过 SPI 接口从 EEPROM 加载可定制的应用程序代码
  - 两个用于外设连接的附加 SPI 端口片选
  - 多达 12 个用于最终用户配置的通用输入输出 (GPIO)
    - 其中两个 GPIO 具有 PWM 功能，可用于控制 LED 闪烁速度
  - 用于调试的串行通信接口 (UART)
- 通用 特性
  - 集成有扩频时钟生成模块，使用单个低成本晶振或时钟振荡器即可正常工作
    - 支持 40MHz
  - 用于 IEEE1149.1 和 IEEE1149.6 边界扫描的 JTAG 接口
  - 采用完全符合 RoHS 标准的封装

2 应用

- 外部 HDD/SSD
- 外部 DVD
- 外部 CD
- 基于 HDD 的便携式媒体播放器

3 说明

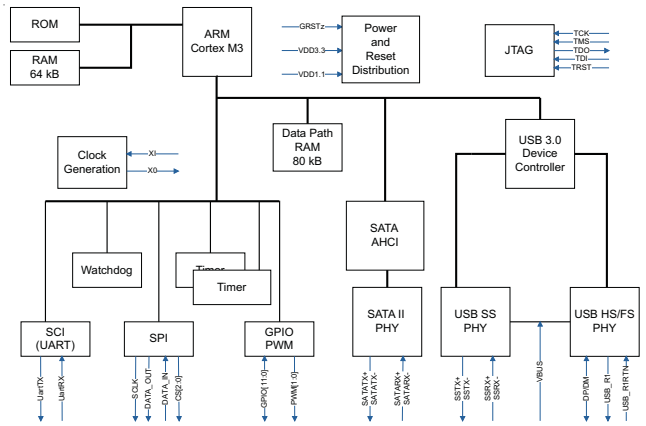
TUSB9261 是一款基于 ARM® Cortex®M3 微控制器的 USB 3.0 至串行 ATA 桥接器。该器件提供了实现兼容 USB 连接 SCSI 协议 (UASP) 的海量存储设备所需的硬件和固件，此类设备适用于将传统硬盘 (HDD)、固态硬盘 (SSD)、光盘驱动器以及其他兼容的 SATA 1.5Gbps 或 SATA 3.0Gbps 设备桥接至 USB 3.0 总线。其固件不仅支持 UASP，还可以实现海量存储设备类 BOT 和 USB HID 接口。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TUSB9261	HTQFP (64)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision H (July 2015) to Revision I **Page**

- Changed the CDM value in the *ESD Ratings* table From: 5000 To: ±1500 7

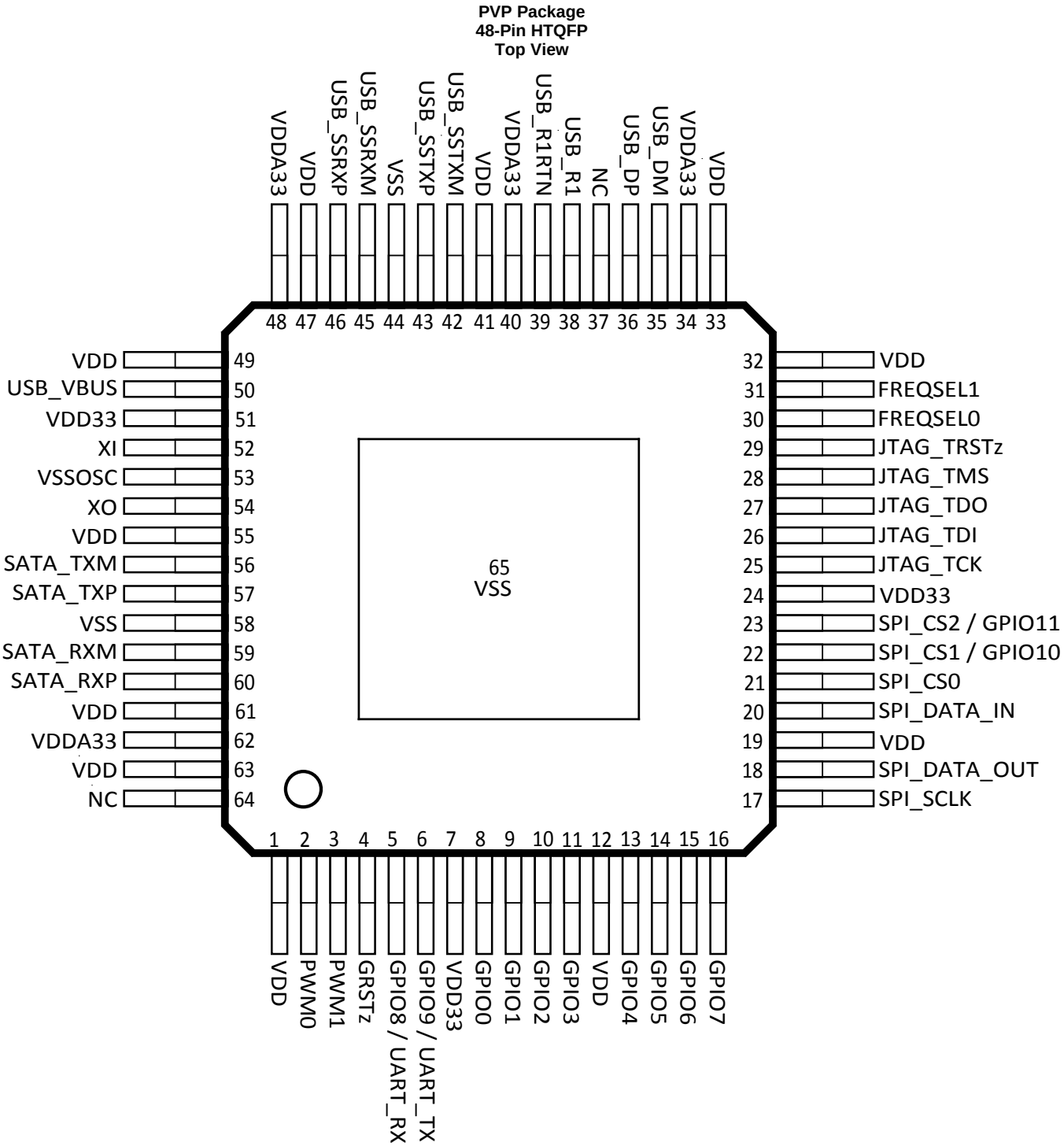
Changes from Revision G (October 2014) to Revision H **Page**

- Moved T_{stg} from *Handling Ratings* table to *Absolute Maximum Ratings* and renamed *Handling Ratings* to *ESD Ratings* ... 7
- Updated the frequency for the USB2 and USB3 to 5 Hz and 10 Hz, respectively 16

Changes from Revision F (March 2014) to Revision G **Page**

- 已将支持的频率更新至 40MHz 1
- Updated supported frequency in *Clock and Reset Signals* table 4
- Updated the frequency for the clock to 40 MHz 9
- Updated the frequency for the crystal to 40 MHz 9
- Updated oscillation frequency and ESR equivalent series resistance 9
- Updated Table 1 12

5 Pin Configuration and Functions



Signal Descriptions – I/O Definitions

I/O TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PU	Internal pullup resistor
PD	Internal pulldown resistor
PWR	Power signal

Clock and Reset Signals

PIN		I/O	DESCRIPTION		
NAME	NO.				
GRSTz	4	I PU	Global power reset. This reset brings all of the TUSB9261 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.		
XI	52	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-MΩ feedback resistor is required between X1 and XO.		
XO	54	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator, this pin may be left unconnected. When using a crystal, a 1-MΩ feedback resistor is required between X1 and XO.		
FREQSEL[1:0]	31, 30	I PU	Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows:		
			FREQSEL[1]	**FREQSEL[0]**	**INPUT CLOCK FREQUENCY**
			1	1	40 MHz

SATA Interface Signals(1)

PIN		I/O	DESCRIPTION
NAME	NO.		
SATA_TXP	57	O	Serial ATA transmitter differential pair (positive)
SATA_TXM	56	O	Serial ATA transmitter differential pair (negative)
SATA_RXP	60	I	Serial ATA receiver differential pair (positive)
SATA_RXM	59	I	Serial ATA receiver differential pair (negative)

(1) Note that the default firmware and reference design for the TUSB9261 have the SATA TXP/TXM swapped for ease of routing in the reference design. If you plan to use the TI default firmware please review the reference design in the *TUSB9261 DEMO User's Guide* (SLLU139) for proper SATA connection.

USB Interface Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
USB_SSTXP	43	O	SuperSpeed USB transmitter differential pair (positive)
USB_SSTXM	42	O	SuperSpeed USB transmitter differential pair (negative)
USB_SSRXP	46	I	SuperSpeed USB receiver differential pair (positive)
USB_SSRXM	45	I	SuperSpeed USB receiver differential pair (negative)
USB_DP	36	I/O	USB high-speed differential transceiver (positive)
USB_DM	35	I/O	USB high-speed differential transceiver (negative)
USB_VBUS	50	I	USB bus power
USB_R1	38	O	Precision resistor reference. A 10-kΩ ±1% resistor should be connected between R1 and R1RTN.
USB_R1RTN	39	I	Precision resistor reference return

Serial Peripheral Interface (SPI) Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
SPI_SCLK	17	O PU	SPI clock
SPI_DATA_OUT	18	O PU	SPI master data out
SPI_DATA_IN	20	I PU	SPI master data in
SPI_CS0	21	O PU	Primary SPI chip select for flash RAM
SPI_CS2/ GPIO11	23	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
SPI_CS1/ GPIO10	22	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.

JTAG, GPIO, and PWM Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
JTAG_TCK	25	I PD	JTAG test clock
JTAG_TDI	26	I PU	JTAG test data in
JTAG_TDO	27	O PD	JTAG test data out
JTAG_TMS	28	I PU	JTAG test mode select
JTAG_TRSTz	29	I PD	JTAG test reset
GPIO9/UART_TX	6	I/O PU	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general-purpose output.
GPIO8/UART_RX	5	I/O PU	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general-purpose output.
GPIO7	16	I/O PD	Configurable as general-purpose input/outputs
GPIO6	15	I/O PD	
GPIO5	14	I/O PD	
GPIO4	13	I/O PD	
GPIO3	11	I/O PD	
GPIO2	10	I/O PD	
GPIO1	9	I/O PD	
GPIO0	8	I/O PD	
PWM0	2	O PD(1)	Pulse-width modulation (PWM). Can be used to drive status LEDs.
PWM1	3	O PD(1)	

(1) PWM pulldown resistors are disabled by default. A firmware modification is required to turn them on. All other internal pull up/down resistors are enabled by default.

Power and Ground Signals

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	PWR	1.1-V power rail
	12		
	19		
	32		
	33		
	41		
	47		
	49		
	55		
	61		
	63		
VDD33	7	PWR	3.3-V power rail
	24		
	51		
VDDA33	34	PWR	3.3-V analog power rail
	40		
	48		
	62		
VSSOSC	53	PWR	Oscillator ground. If using a crystal, this should not be connected to a PCB ground plane. If using an oscillator, this should be connected to PCB ground. See *Clock Source Requirements* for more details.
VSS	44	PWR	Ground
	58		
VSS	65	PWR	Ground – Thermal pad
NC	37	—	No connect, leave floating
	64		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Steady-state supply voltage	–0.3	1.4	V
V_{DD33}/ V_{DDA33}	Steady-state supply voltage	–0.3	3.8	V
T_{stg}	Storage temperature	–55	150	°C

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 (1)	±2000	V
		Charged device model (CDM), per JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Digital 1.1-V supply voltage		1.045	1.1	1.155	V
V_{DD33}	Digital 3.3-V supply voltage		3	3.3	3.6	V
V_{DDA33}	Analog 3.3-V supply voltage		3	3.3	3.6	V
V_{BUS}	Voltage at VBUS PAD		0		1.155	V
T_A	Operating free-air temperature range		0		70	°C
		Industrial version	–40		85	
T_J	Operating junction temperature range		–40		100	°C

6.4 Thermal Information

THERMAL METRIC (1)		TUSB9261 PVP (HTQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.1	°C/W
$R_{J\theta C(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics for 3.3-V Digital I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
T_R	Rise time	5 pF			1.5	ns
T_F	Fall time	5 pF			1.53	ns
I_{OL}	Low-level output current	V_{DD33} = 3.3 V, T_J = 25°C		6		mA
I_{OH}	High-level output current	V_{DD33} = 3.3 V, T_J = 25°C		–6		mA
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OL} = –2 mA	2.4			V
V_O	Output voltage		0		VDD33	V
RECEIVER						
V_I	Input voltage		0		VDD33	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Input hysteresis		200			mV
t_T	Input transition time (T_R and T_F)				10	ns
I_I	Input current	V_I = 0 V to V_{DD33}			5	µA
C_I	Input capacitance	V_{DD33} = 3.3 V, T_J = 25°C		0.384		pF

6.6 SuperSpeed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL SUSPEND CURRENT (mA)(2)
VDD11	291	153
VDD33(3)	65	28

(1) Transferring data by SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.
(2) SATA Gen II SSD attached no active transfer. No SATA power management, U3 only.
(3) All 3.3-V power rails connected together.

6.7 High-Speed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL SUSPEND CURRENT (mA)(2)
VDD11	172	153
VDD33(3)	56	28

(1) Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.
(2) SATA Gen II SSD attached no active transfer. No SATA power management.
(3) All 3.3-V power rails connected together.

6.8 Oscillator Specification

XI should be tied to the 1.8-V clock source and XO should be left floating. VSSOSC should be connected to the PCB ground plane. A 40-MHz clock can be used.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XI}	XI input capacitance	T_J = 25°C		0.414		pF
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		1.05			V
T_{tosc_i}	Frequency tolerance	Operational temperature	–50		50	ppm
T_{duty}	Duty cycle		45%	50%	55%	
T_R/T_F	Rise/fall time	20% to 80%			6	ns
R_J	Reference clock	JTF (1 sigma)(1)(2)			0.8	ps
T_J	Reference clock	JTF (total p-p)(2)(3)			25	ps
T_{p-p}	Reference clock jitter	(Absolute p-p)(4)			50	ps

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as $14.1 \times R_J + D_J$
(4) Absolute phase jitter (p-p)

6.9 Crystal Specification

A parallel, 20-pF load capacitor should be used if a crystal source is used. VSSOSC should not be connected to the PCB ground plane. A 40-MHz crystal can be used.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Oscillation mode			Fundamental		
f_O	Oscillation frequency			40		MHz
ESR	Equivalent series resistance	40 MHz			50	Ω
T_{tosc_i}	Frequency tolerance	Operational temperature			±50	ppm
	Frequency stability	1 year aging			±50	ppm
C_L	Load capacitance		12	20	24	pF
C_{SHUNT}	Crystal and board stray capacitance				4.5	pF
	Drive level (max)				0.8	mW

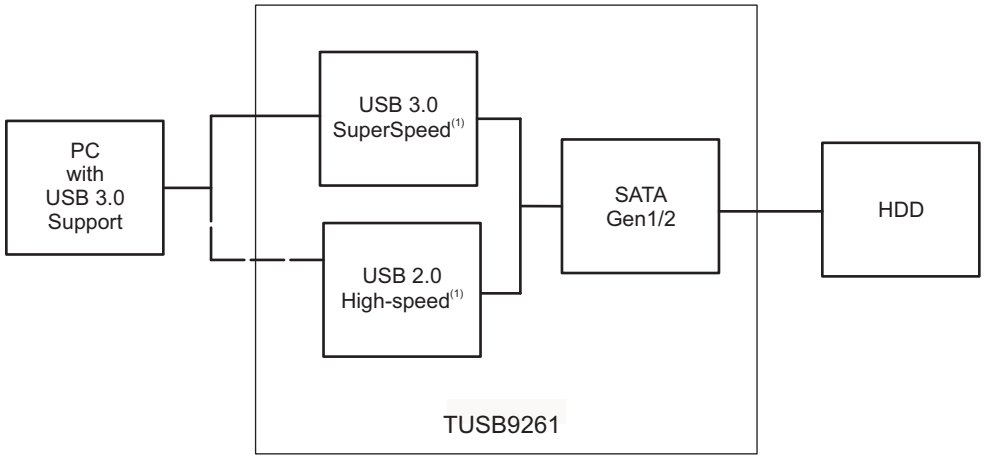
7 Detailed Description

7.1 Overview

The major functional blocks are as follows:

- Cortex M3 microcontroller subsystem including the following peripherals:
  - Time interrupt modules, including watchdog timer
  - Universal asynchronous receive/transmit (SCI)
  - SPI
  - General purpose input/output (GPIO)
  - PWM for support of PWM outputs (PWM)
- USB 3.0 core (endpoint controller) and integrated USB 3.0 PHY
- AHCI-compliant SATA controller and integrated SATA PHY
  - Supporting Gen1i, Gen1m, Gen2i, and Gen2m
- Chip level clock generation and distribution
- Support for JTAG 1149.1 and 1149.6

7.2 Functional Block Diagram



A. USB connection is made at either SuperSpeed or high speed, depending on the upstream connection support.

7.3 Feature Description

7.3.1 Operation

7.3.1.1 General Functionality

The TUSB9261 ROM contains boot code that executes after a global reset, which performs the initial configuration required to load a firmware image from an attached SPI flash memory to local RAM.

After the firmware is loaded, it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller. In addition, the configuration of the AHCI includes a port reset, which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so, negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps).

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class BOT, allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application-specific implementation, for example, a HID interface for user initiated backup.

Feature Description (continued)

After the USB device controller configuration is complete, if a SATA device was detected during the AHCI configuration, the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9261 initially tries to connect at SuperSpeed USB. If successful, it enters U0; otherwise, after the training time out, it enables the DP pullup and connects as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected, the firmware presents the BOT interface as the primary interface and the UASP interface as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

Following speed negotiation, the device should transmit a device to host (D2H) FIS with the device signature. This first D2H FIS is received by the link layer and copied to the port signature register. When firmware is notified of the device connection, it queries the device for capabilities using the IDENTIFY DEVICE command. Firmware then configures the device as appropriate for its interface and features supported, for example, an HDD that supports native command queuing (NCQ).

7.3.1.2 Firmware Support

Default firmware support is provided for the following:

- SuperSpeed USB and USB 2.0 high speed and full speed
- USB attached SCSI protocol (UASP)
- USB mass storage class (MSC) bulk-only transport (BOT)
  - Including the 13 error cases
- USB mass storage specification for bootability
- USB device class definition for HID
  - Firmware update and custom functionality (for example, one-touch backup)
- Serial ATA advanced host controller interface (AHCI)
- GPIO
  - LED control and custom functions (for example, one-touch backup control)
- PWM
  - LED dimming control
- SPI
  - Firmware storage and storing custom device descriptors
- Serial communications interface (SCI)
  - Debug output only

Feature Description (continued)

7.3.1.3 GPIO/PWM LED Designations

The default firmware provided by TI drives the GPIO and PWM outputs as listed in Table 1.

Table 1. GPIO/PWM LED Designations

GPIO	DESCRIPTION		DEFAULT SETUP
GPIO0	Undefined. Can use HID commands to change to output low or high. [internal 100-µA PD]		Input
GPIO1	USB 3.0 Link State if U1/U2 enabled, otherwise [input with 100-µA PD]		Output
GPIO5	USB 3.0 Link State if U1/U2 enabled, otherwise [input with 100-µA PD]		Output
GPIO1/ GPIO5	USB3 power state (U0 to U3)	U0: Off/Off	Output
		U1: On/Off	
		U2: Off/On	
		U3: On/On	
		Other: Off/Off	
GPIO2	HS/FS suspend		Output
GPIO3	[INPUT with 100-µA PD] momentary push button		Input
GPIO4	Bus- or self-powered indicator. (GPIO level should be HIGH when self-powered). [internal 100-µA PD]		Input
GPIO6	Undefined. Can use HID commands to change to output low or high. [internal 100-µA PD]		Input
GPIO7	SS connection		Output
GPIO10	Undefined. Can use HID commands to change to output low or high. Compile option to configure as SATA drive power enable output. [internal 100-µA PU]		Input
GPIO11	Power fault indicator. [internal 100-µA PU]		Input
PWM0	Disk activity (LED blink rate is faster when connected at USB SuperSpeed), USB connection (LED on), and USB suspend (fading LED).		Output
PWM1	SW heartbeat		Output

The LEDs on the TUSB9261 product development kit (PDK) board are connected as in Table 1. See the TUSB9261 PDK Guide for more information on GPIO LED connection and usage. This EVM is available for purchase. Contact TI for ordering information.

7.3.1.4 Power-Up and Reset Sequence

The core power (VDD) must be present and at its minimum high level prior to, or at the same time that, the I/O power (VDD33).

In addition, meet the following constraints:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 2 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz.

7.3.2 Clock Connections

7.3.2.1 Clock Source Requirements

The TUSB9261 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow these guidelines.

Because XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. TI also recommends to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (C_{load}) of the crystal (varies with the crystal vendor) is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors, CL1 and CL2, in Figure 1. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB9261 must be minimized. TI also recommends that the trace length from the capacitor pad to the power or ground plane be minimized.

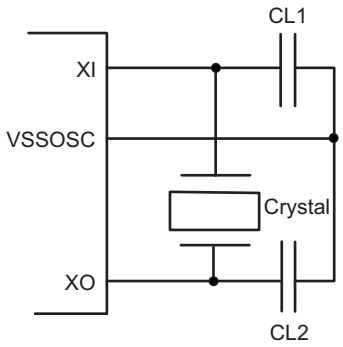


Figure 1. Typical Crystal Connections

7.3.2.2 Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock degrades both the transmit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with the PLL lock detection mechanism, forcing the lock detector to issue an Unlock signal. A good-quality, low-jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function (JTF)). As the PLL typically has a number of additional jitter components, the reference clock jitter must be considerably below the overall jitter budget.

7.4 Device Functional Modes

7.4.1 VBUS Power

Power can be supplied by a USB cable on the terminal VBUS. When using power from VBUS, both the TUSB9261 and the SATA device are allowed to draw only up to 500 mA from VBUS when operating.

7.4.2 External Power

Power can be supplied from an external power source. When using an external power source, both the TUSB9261 and the SATA interface can draw all their current from the external supply.

Device Functional Modes (continued)

7.4.3 External Voltage Regulator

Because the TUSB9261 requires two voltage supplies (1.1 V and 3.3 V), TI recommends a multi-channel voltage regulator. The TPS650061 or TPS65024x are good choices. The TPS650061 uses a DC-DC converter and two LDO regulators in a single package. The DC-DC converter can supply 1-A nominal current while the two LDOs can supply 300-mA nominal current. Because the 1.1-V supply can consume upwards of 340 mA of current, the DC-DC converter is ideal for supplying the 1.1-V current while the two LDOs can be used to supply 3.3-V current. Likewise the TPS65024x uses three DC-DC converters and three LDOs. Both devices also have a built-in supervisor circuit that can be connected to $\overline{\text{GRST}}$ on the TUSB9261.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device serves as a bridge between a downstream USB 3.0 host port and a SATA device such as a hard disk drive. A crystal or oscillator supplies the required clock source. A SPI flash device contains the firmware that is loaded into the TUSB9261 after the deassertion of RESET. Push buttons or any other desired logic can be connected to the TUSB9261 GPIO pins. The TUSB9261 can also output a pulse-width modulated signal that can be used to drive an activity LED.

8.2 Typical Application

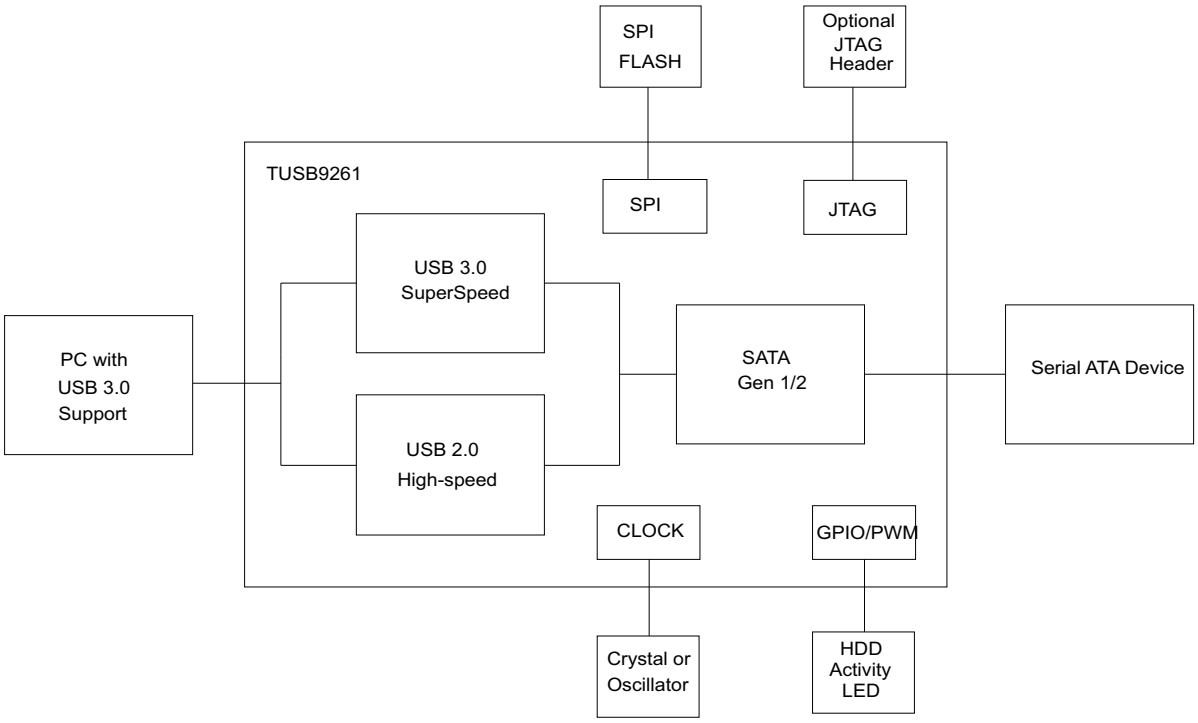


Figure 2. Typical Application Schematic

8.2.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD supply	1.1 V
VDD33 supply	3.3 V
Upstream port USB support	SS, HS, FS
Main supply	VBUS
USB_VBUS resistor values	90.9 kΩ, 10 kΩ
Crystal frequency	40 MHz
SATA device	SSD

8.2.2 Detailed Design Procedure

8.2.2.1 PWM Terminals

The TUSB9261 has two pulse-width modulated output terminals.

Table 3 shows the default firmware configuration of PWMs.

Table 3. Default Firmware Configuration of PWMs

PWM	USAGE
0	Primary Indicator LED: ON when there is a USB connection. OFF when there is no connection. Blinks during disk activity (Frequency: 5 Hz for USB2 or 10 Hz for USB3). Fades when USB is in Suspend or U3 state.
1	Power indicator LED

PWM duty cycle will be 0% when the LED should be fully ON.

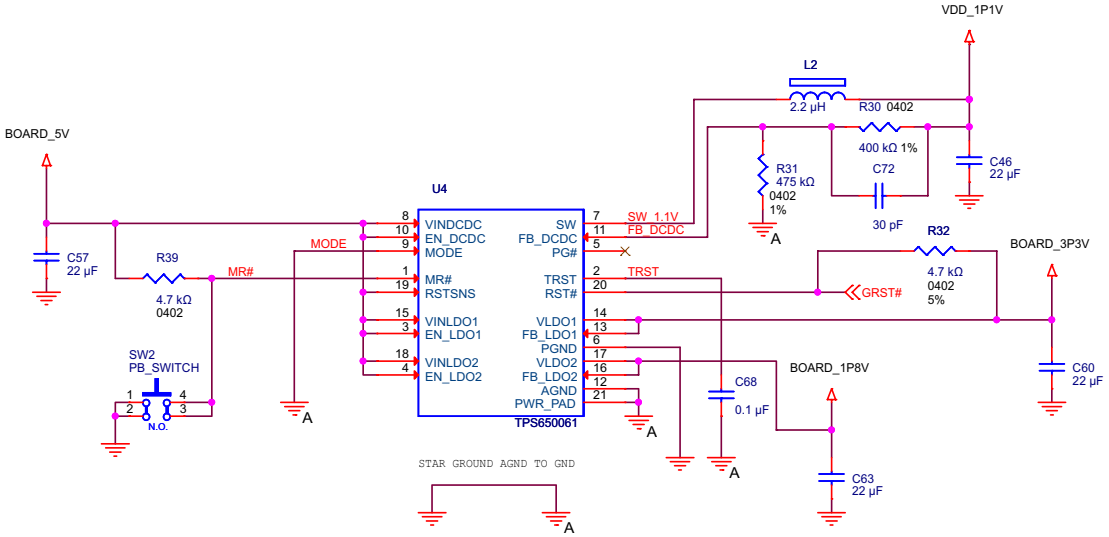
8.2.2.2 JTAG Interface

The TUSB9261 supports JTAG for board-level test and debug support. Typically, these terminals are left unconnected or routed to a header to plug in an external JTAG controller. Table 4 shows the JTAG terminal names and internal resistor connection. The JTAG interface should be left unconnected if JTAG support is not required.

Table 4. Internal JTAG Resistor Termination

NAME	PULL UP OR PULL DOWN	DESCRIPTION
JTAG_TCK	Pull down	JTAG test clock
JTAG_TDI	Pull up	JTAG test data in
JTAG_TDO	Pull down	JTAG test data out
JTAG_TMS	Pull up	JTAG test mode select
JTAG_RSTZ	Pull down	JTAG reset

8.2.2.3 Voltage Regulator Schematic



8.2.2.4 SPI

A SPI system consists of one master device and one or more slave devices. The TUSB9261 is a SPI master providing the SPI clock, data-in, data-out, and up to three chip-select terminals.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with an active-low chip select terminal (SPI_CS[2:0]#). Data is transmitted with a 3-terminal interface consisting of terminals for serial data input (SPI_DATA_IN), serial data output (SPI_DATA_OUT) and serial clock (SPI_SCLK).

All SPI terminals have integrated pullup resistors. No external components are required to connect the SPI interface to an external SPI flash device. See Figure 3 for an example implementation of the SPI interface using one SPI slave device.

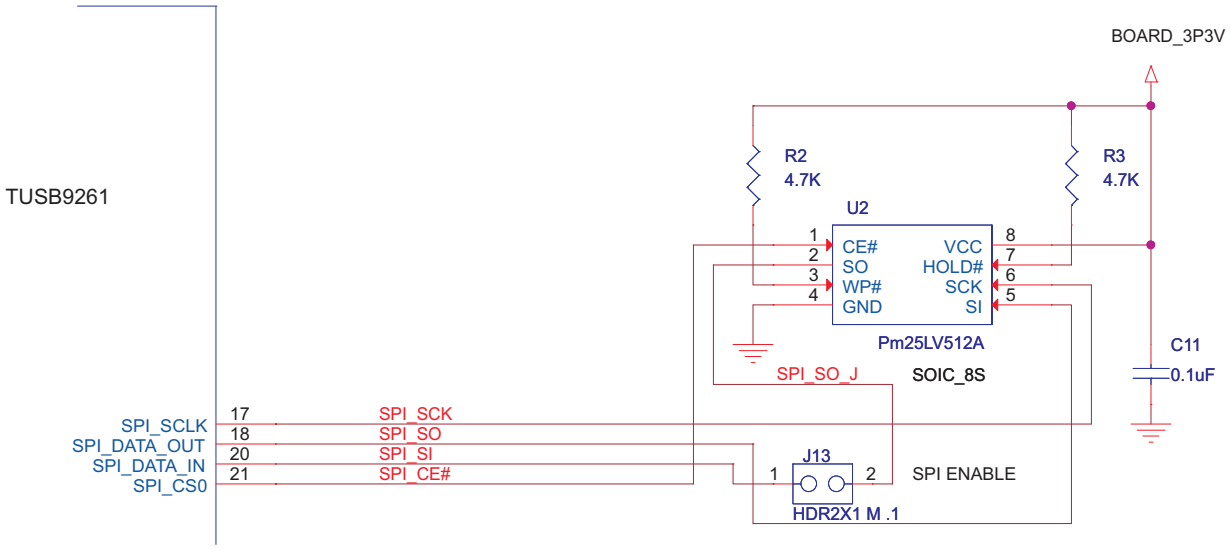


Figure 3. SPI Connection

The SPI_CLK is running at a fixed frequency of 18.75 MHz and its clocking mode is configured with a POLARITY of 0 and a PHASE of 1, this means that the SPI sends the data output one half-cycle before the first rising edges of SPI_CLK and on subsequent falling edges. Meanwhile, the input data is latched on the rising edge of SPI_CLK (see Figure 4 and Table 5 for a detailed timing description).

The flash memory is erased by the bootloader prior to programming and must use a word size of 8 bits with an address length of 24 bits and its program instruction must allow 256 bytes to be written in one operation. TI recommends a minimum flash size of 512 kb (64 k × 8). Table 5 shows SPI flash devices that have been tested with the TUSB9261.

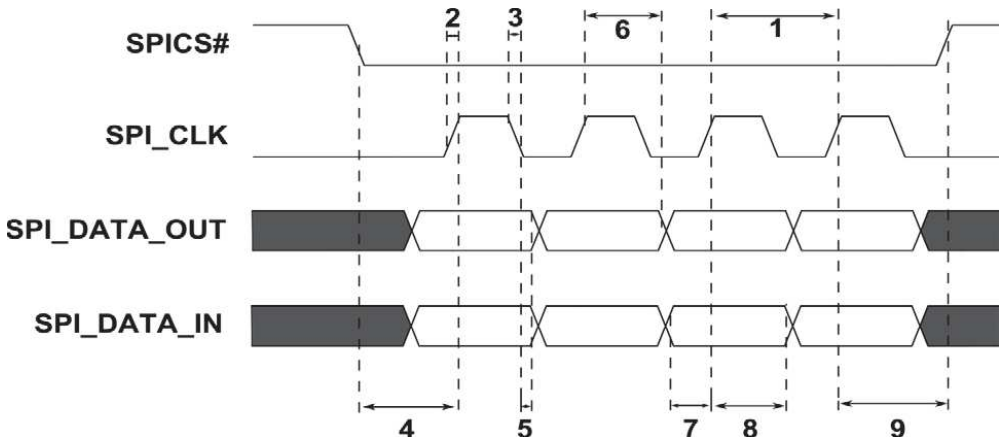


Figure 4. SPI Characterization

Table 5. SPI Characterization Time

NO.	TIME REFERENCE	THEORETICAL VALUE
1	Cycle time SPICLK	53.3 ns
2	Positive SPI_CLK slope	2 ns
3	Negative SPI_CLK slope	3 ns
4	SPISCS – SPICLK edge(PHASE = 1)	MIN: 53.3 ns TYP: 80 ns MAX: 93.3 ns
5	Output delay time, SPICLK TX edge to SPISIMO valid	260 ps
6	Output hold time, SPICLK RX edge to SPISIMO valid	26.7 ns
7	Setup time	22 ns
8	Hold time	500 ps
9	"SPICLK -SPISCS Phase = 1, Master"	13.3 ns

9 Power Supply Recommendations

9.1 Digital Supplies 1.1-V and 3.3-V

The TUSB9261 requires a 1.1-V and 3.3-V digital power source.

The 1.1-V terminals are named VDD11. These terminals supply power to the digital core. The 1.1-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named VDD33 and supply power to most of the input and output cells. Both VDD11 and VDD33 supplies must have 0.1-μF bypass capacitors to VSS (ground) to ensure proper operation. One capacitor per power terminal is sufficient and should be placed as close to the terminal as possible to minimize trace length. TI also recommends smaller value capacitors like 0.01-μF on the digital supply terminals.

When placing and connecting all bypass capacitors, follow high-speed board design rules.

9.2 Analog Supplies 1.1-V and 3.3-V

TI recommends a Pi filter on all analog power terminals to minimize circuit noise. These filters can be combined on a per-rail basis for a total of two (VDDA11 / VDDA11_USB2) + (VDDA33).

Analog power terminals must have a 1-μF and a 10-μF bypass capacitor connected to VSSA (ground) to ensure proper operation. Place the capacitor as close as possible to the associated terminal to minimize trace length. TI also recommends smaller value capacitors such as 0.1-μF and 0.01-μF on the analog supply terminals.

10 Layout

10.1 Layout Guidelines

10.1.1 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a USB type B connector. The differential pair traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between high-speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling capacitors are required. If a common-mode choke is required, then place the choke as close as possible to the USB connector signal pins. Likewise, ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

To minimize crosstalk on the USB2/3 differential signal pairs, TI recommends that the spacing between the two interfaces be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs and the DP/DM differential pair. If this 5W rule cannot be implemented, then the space between the TX/RX differential pairs and DP/DM differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.1.2 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each differential pair's traces should be routed with 90-Ω, ±15% differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter differential pair requires 0.1-uF coupling capacitors for proper operation. The package/case size of these capacitors should be no bigger than 0402. C-packs are not allowed. The capacitors should be placed symmetrically as close as possible to the USB connector signal pins. If a common mode choke is required, then place the choke as close as possible to the USB connector signal pins (closer than the transmitter capacitors). Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter capacitors).

Layout Guidelines (continued)

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with receive differential pair. To minimize crosstalk on the SS USB differential signal pairs, TI recommends that the spacing between the TX and RX signal pairs be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.1.3 SATA Differential Routing

The SATA traces (SATA_TXP and SATA_TXM) should be routed with 100-Ω, ±15% differential impedance. Maximum trace length mismatch between SATA signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. Each SATA trace requires a coupling capacitor be placed inline. The package/case size of these capacitors should be no bigger than 0402. C-packs are not allowed. The capacitors should be placed symmetrically as close as possible to the SATA connector signal pins.

It is permissible to swap the plus and minus on the SATA differential pair. This may be necessary to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with the receive differential pair.

To minimize crosstalk on the SATA differential signal pairs, TI recommends that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the SATA TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs. If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

10.2 Layout Examples

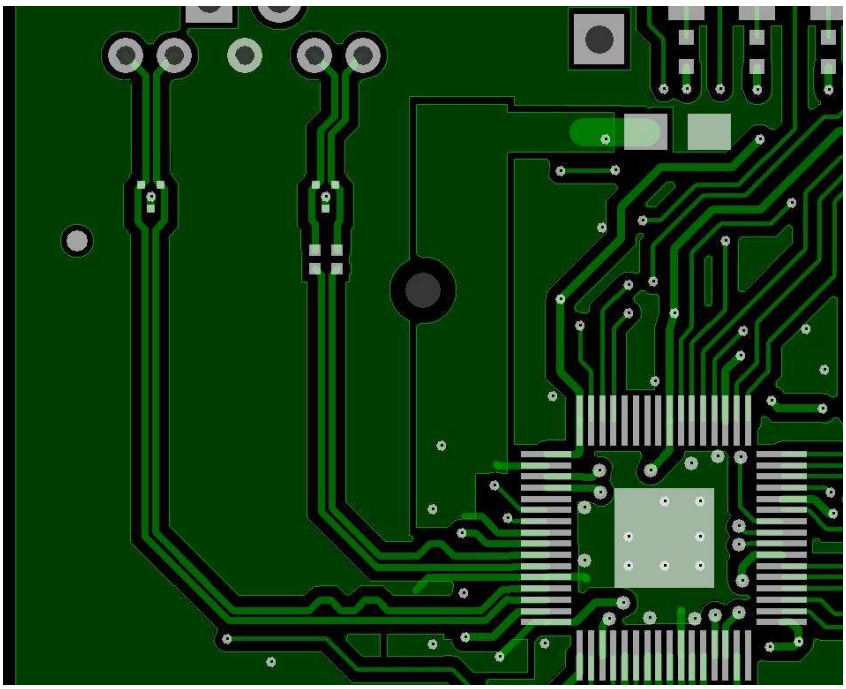


Figure 5. SuperSpeed Differential Routing

Layout Examples (continued)

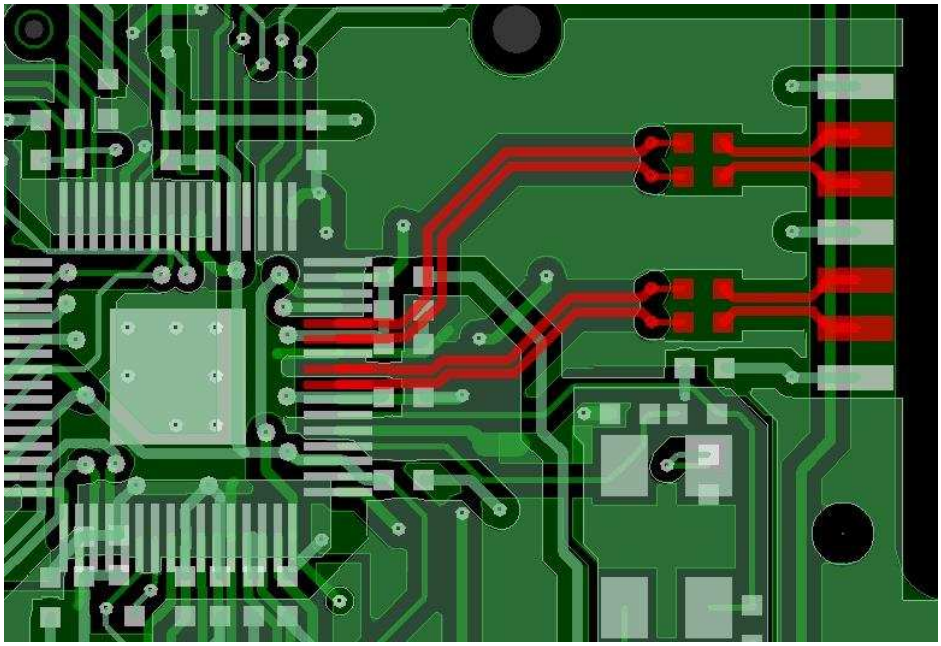


Figure 6. SATA Differential Routing

11 器件和文档支持

11.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.2 商标

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ARM, Cortex are registered trademarks of ARM Ltd.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB9261IPVP	ACTIVE	HTQFP	PVP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB9261I	Samples
TUSB9261PVP	ACTIVE	HTQFP	PVP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB9261	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

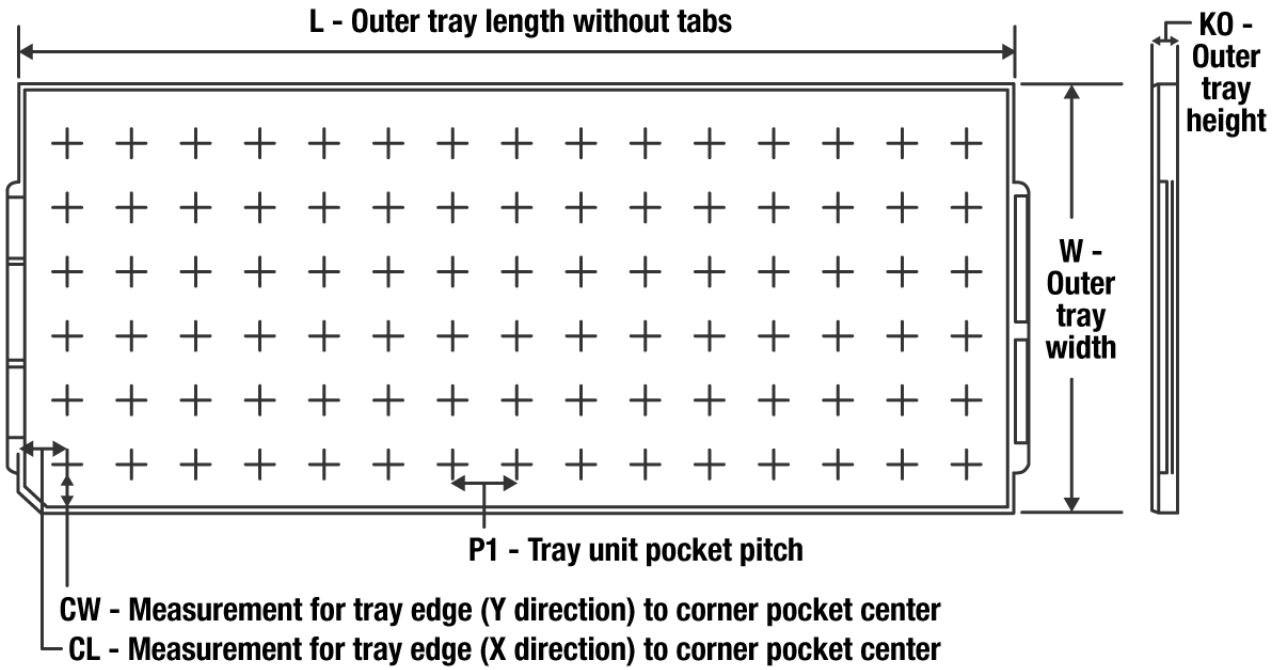
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

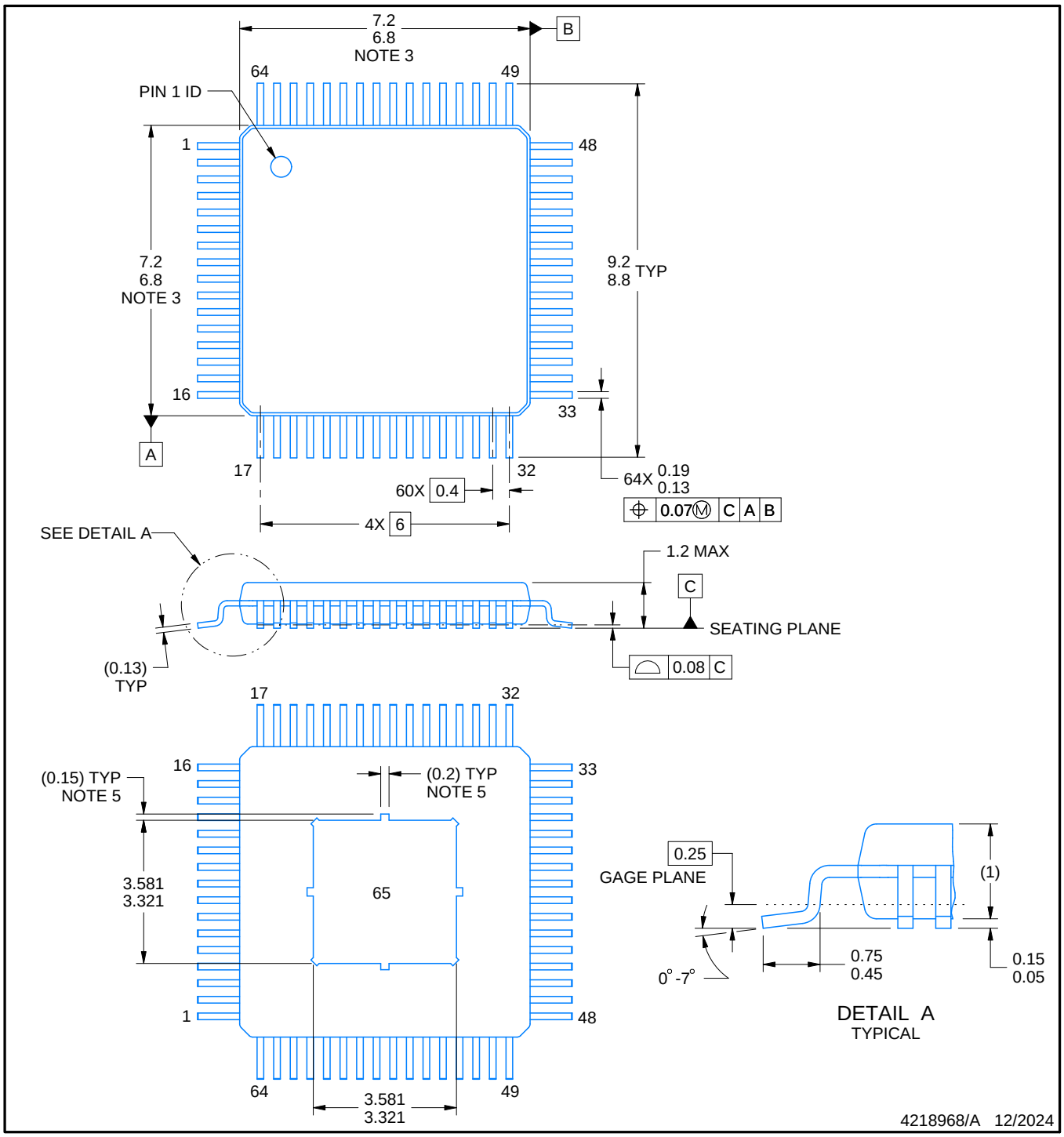
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TUSB9261IPVP	PVP	HTQFP	64	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TUSB9261PVP	PVP	HTQFP	64	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PVP0064A

PowerPAD™ HTQFP - 1.2 mm max height

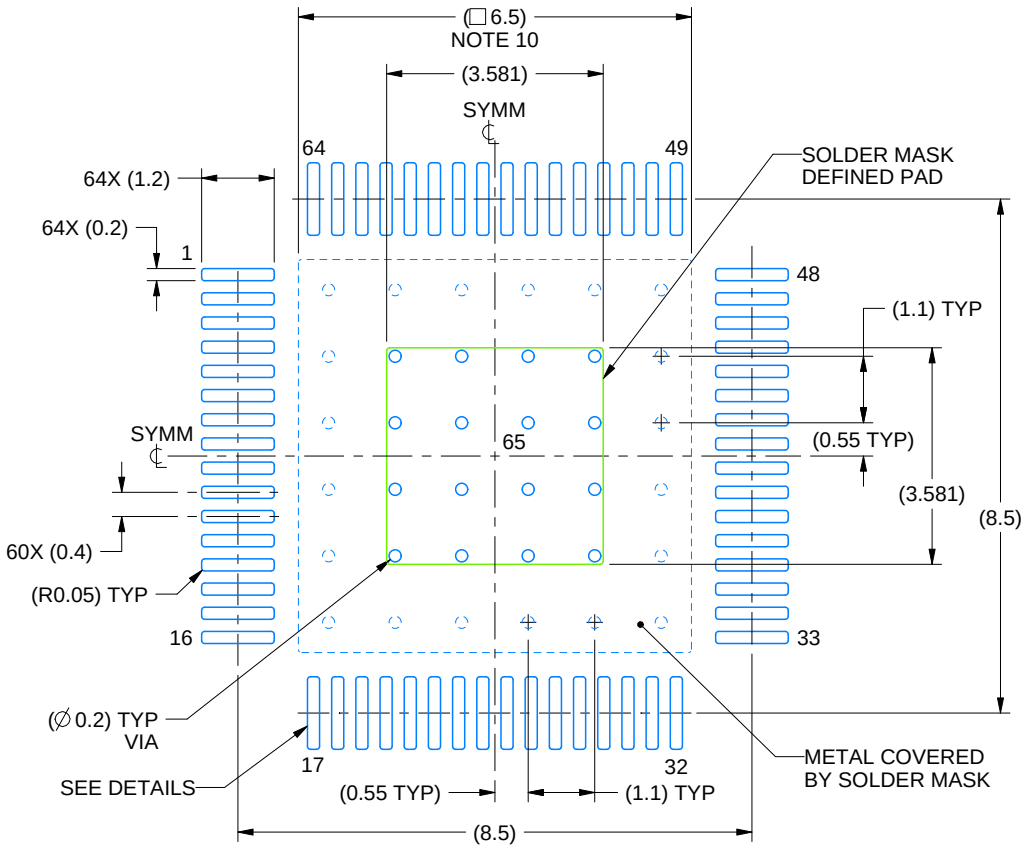
PLASTIC QUAD FLATPACK



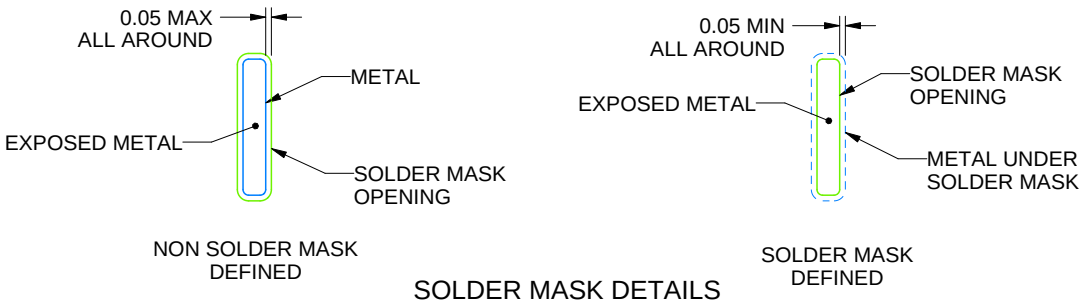
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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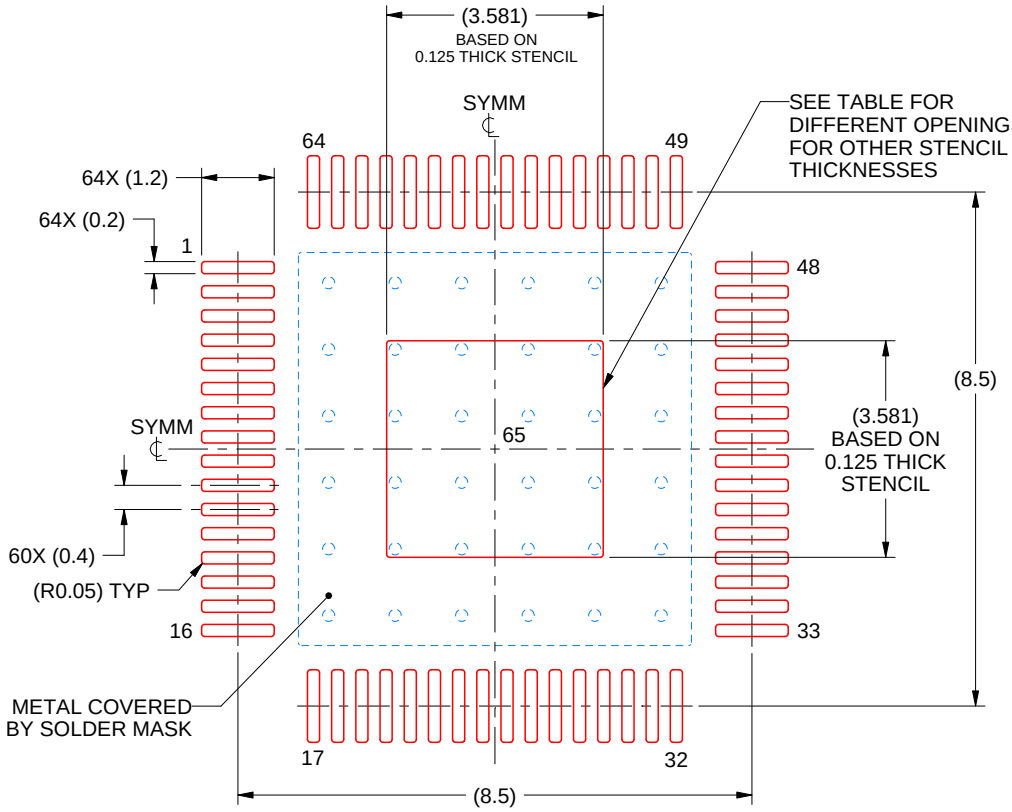
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.004 X 4.004
0.125	3.581 X 3.581 (SHOWN)
0.150	3.269 X 3.269
0.175	3.026 X 3.026

4218968/A 12/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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