Application Report
DLPA042–October 2013

DLP® LightCrafter™ FPGA Overview

DLP MEMS

ABSTRACT

DLP® LightCrafter™ evaluation module (EVM) is offered as a convenient and flexible tool for familiarization and development with the TI DLP3000/DLPC300 chipset. An FPGA is incorporated into the design of DLP LightCrafter. This document gives an overview of the functions of the FPGA.

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1 Introduction

The DLP® LightCrafter™ evaluation module (EVM) is offered as a convenient and flexible tool for familiarization and development with the TI DLP3000/DLPC300 chipset.

The DLP LightCrafter EVM consists of three components:

- Light Engine
- Driver Board
- System Board

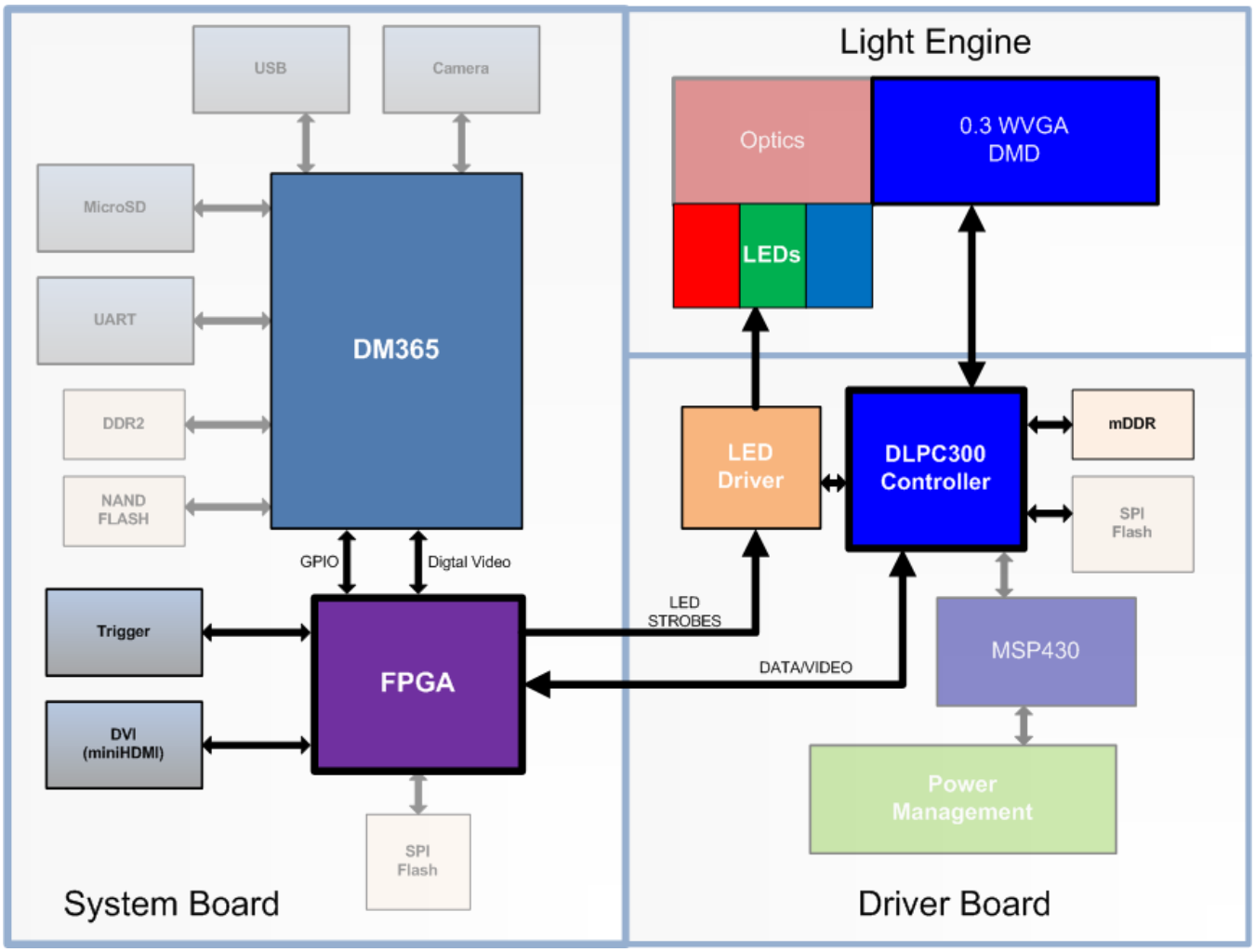

Figure 1. DLP® LightCrafter™ Block Diagram

The Light Engine interfaces to the DLP3000 DMD, and provides the LED illumination and optical elements necessary for the projection of the patterns and images produced by the other components of DLP LightCrafter. The Light Engine is not discussed further in this document.

The Driver Board contains the DLPC300 controller chip, which provides the required direct interface and core capabilities to the DLP3000 Digital Micromirror Device (DMD). The System Board provides higher-level functionality via a TI DM365 DaVinci Digital Video Processor running Linux OS. The System Board also contains an FPGA (Altera Cyclone IV EP4CE6), which interfaces to both the DM365 and the DLPC300, as well as providing other system functions.

The FPGA provides several important functions to enable the features and performance of DLP LightCrafter:

- MUX between DM365 video and external DVI video input

- Manages Frame Buffer operation in internal and stored pattern modes
- Camera Trigger control
- LED Exposure control

1.1 FPGA Overview

An overview block diagram of the FPGA is shown in Figure 2. This figure shows the signals which are input and output from the FPGA, and the major functional blocks implemented by the FPGA.

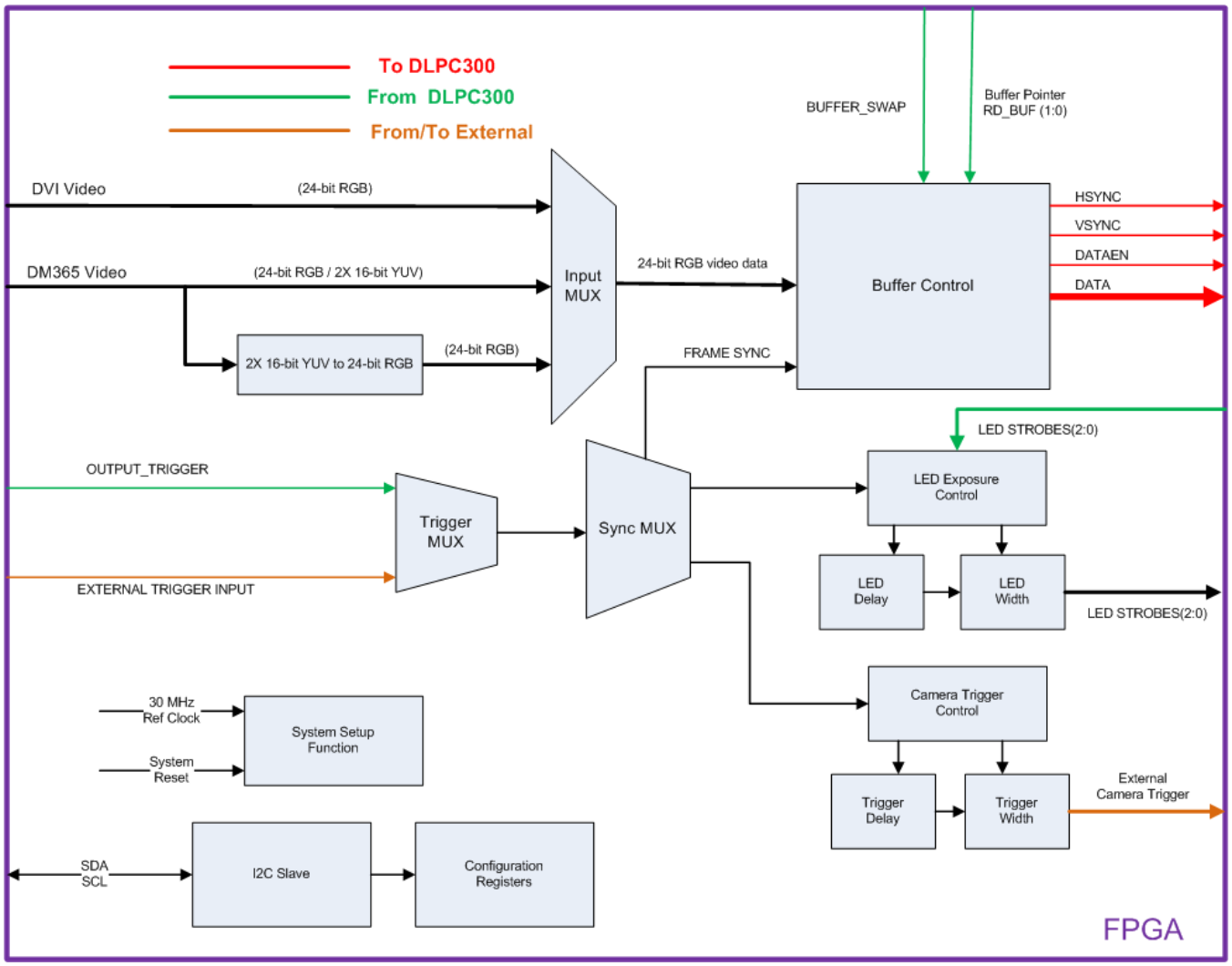

Figure 2. FPGA Overview Block Diagram

The FPGA expands the functionality of the TI DLP3000/DLPC300 chipset to enable the features of DLP LightCrafter. The additional capabilities include:

- An external trigger input, which allows an external device to trigger stored patterns; configurable for polarity (positive/negative), delay, and duration (pulse width).
- An external trigger output, which provides the ability to synchronize an external camera with the display of patterns; configurable for polarity (positive/negative), delay, and duration (pulse width).
- A timing generator, which implements the internal auto trigger for continuously repeated pattern display.
- Control for the illumination LEDs; generates LED strobe signals with configurable delay and duration to set exposure; synchronized with the trigger.

- A video data source input selector (MUX); sends the video data to the DLPC300 parallel input. Inputs are:
  - Video from the TFP401A DVI receiver
  - DM365 24-bit RGB (not bit identical with stored patterns)
  - DM365 YUV4:2:2 video converted to RGB888 (bit identical with stored patterns).
- Timing and signal management for a "circular" frame buffer

An important feature of DLP LightCrafter is the ability to display stored patterns at high frame rates. The FPGA provides the timing and signal management to implement a four buffer rotation scheme, which enables a stored pattern capability of 4 × 24 = 96 binary patterns. The operation of the "circular" frame buffer is discussed in greater detail in the subsequent sections.

2 FPGA Functional Description

This section describes in more detail the functionality of the blocks shown in Figure 2. All of the functions, modes, and operations of the FPGA are configured via commands on its I2C bus, which set onboard registers.

The video data from both the DM365 and the DVI receiver come into the FPGA on separate 24-bit parallel buses. The video interface from the FPGA to the DLPC300 is a parallel 24-bit (RGB888) digital interface.

Control signals from the DLPC300 are received by the FPGA – RD_BUF(1:0), BUFFER_SWAP, OUTPUT_TRIGGER, LED STROBES. The FPGA also drives signals to the DLPC300 – BUFFER_INVERT, HSYNC, VSYNC, DATAEN.

This following sections describe the functionality of the blocks shown in Figure 2.

2.1 Input MUX

The Input MUX selects the video data source for the DLPC300 parallel video data input.

1. DVI 24-bit video (from miniHDMI input)
2. DM365 video stream

The DVI 24-bit video is simply passed through to the DLPC300.

The DM365's standard 24-bit video output is YUV4:2:2, which is not bit identical to the pattern data stored in the pattern memory buffer. The DM365 is used in a 16-bit video mode with 54 MHz pixel rate, in which all 24 bits of the pattern are contained within two successive 16-bit words. The FPGA assembles the two 16-bit words into 24-bit RGB888 data, which is bit identical to the stored pattern data.

2.2 Trigger MUX

The Trigger MUX selects between:

1. Internal software generated pulse
2. Internally generated repeated (Auto) trigger with configurable frequency
3. External trigger, with selectable polarity (invert) and selectable delay

The internal (Auto) trigger can be set from 1 Hz–4000 Hz.

The FPGA conditions an external trigger supplied to DLP LightCrafter. In the Stored Pattern Sequence mode, either "Auto" trigger (internally generated), or "External Trigger" is selected. DLP LightCrafter Trigger output timing with respect to the External Trigger signal is shown in Figure 3.

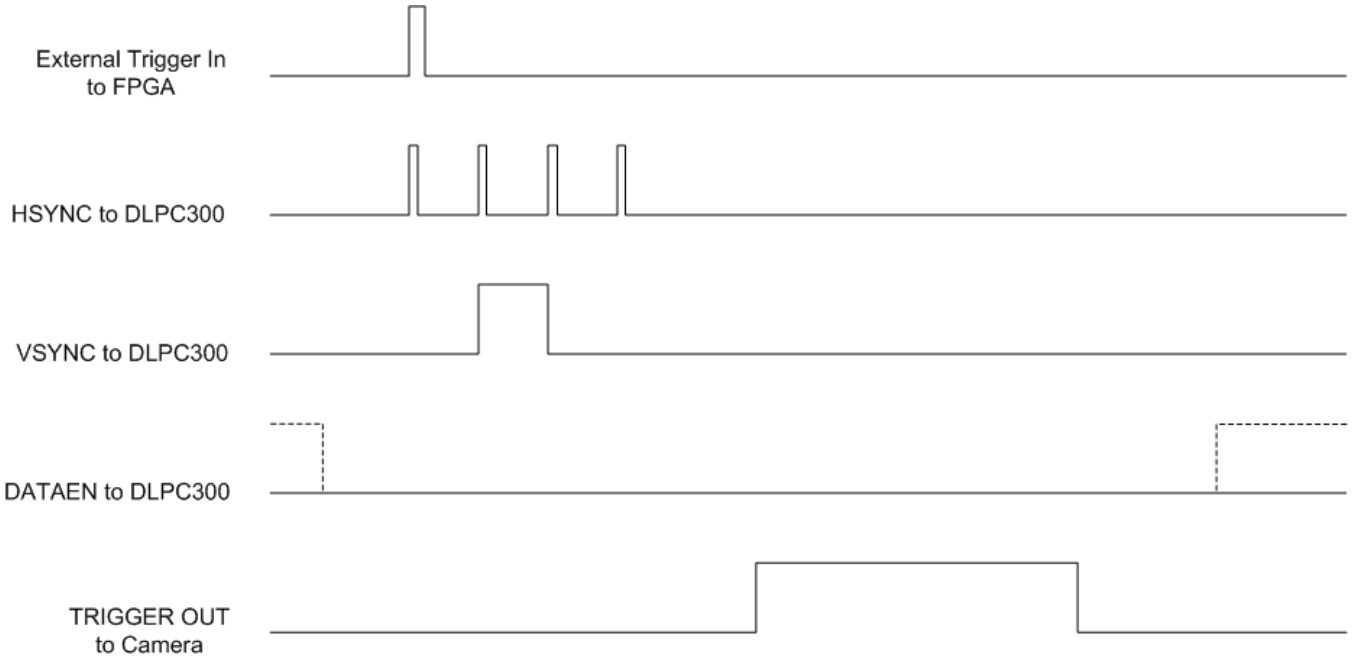

Figure 3. External Trigger Timing (Stored Pattern Sequence Mode with External Trigger)

Important Note

The FPGA does not have hysteresis on its inputs. Therefore, in order to avoid false triggers, it is advised to buffer the trigger input with a Schmitt trigger. Refer to the Altera Cyclone IV EP4CE6 documentation for I/O rise and fall time specifications.

2.3 Sync MUX

The Sync MUX selects among the various sync sources and provides these sync sources to the Camera Trigger Controller (CTC) and LED Enable Controller (LED) blocks. In addition, the selected trigger can be used to generate a FRAME SYNC pulse (VSYNC), which initiates a process to cause the stored buffers to advance to the next buffer.

2.4 Buffer Control

DLP LightCrafter can display up to 96 binary patterns in a continuously repeated set of patterns at binary (1-bit) patterns at up to 4000 frames (patterns) per second. This is accomplished by a 4 section (24 patterns per section) “circular” buffer residing in the mDDR memory device, which is controlled by the DLPC300.

The Buffer Control generates and sequences the proper signals to the DLPC300 to advance the frame buffer. These signals include:

- HSYNC -- horizontal (or "line") synchronization
- VSYNC -- vertical (or "frame") synchronization
- DATAEN -- signal which brackets the valid data
- DATA -- the 24-bit video data (RGB888)

The BUFFER_SWAP signal from the DLPC300 causes the FPGA to initiate a buffer rotation operation. The BUFFER_SWAP signal is triggered by a bit in the stored sequence associated with the last pattern in each buffer.

The RD_BUF (1:0) signals indicate which buffer (0-3) is currently active.

RD_BUF[1:0] = 00b

RD_BUF[1:0] = 01b
RD_BUF[1:0] = 10b
RD_BUF[1:0] = 11b

The value of the RD_BUF(1:0) is crucial for the system to know whether the DLPC300 actually did jump to the next buffer.

The OUTPUT_TRIGGER signal (goes to the Trigger MUX) indicates that the next pattern has been displayed. The output trigger is derived from this signal. The output trigger is used, for example, to synchronize a camera with each frame of a pattern sequence.

The PATTERN_INVERT signal to the DLPC300 is used by the FPGA to cause each pattern in the sequence of patterns to be displayed first as the pattern, then as the inverse of the pattern, and so on, throughout the pattern sequence.

2.5 Camera Trigger Controller (CTC)

The CTC conditions the external and internal trigger signal to an external trigger signal, which is used to synchronize a camera. The CTC provides the ability to adjust the polarity, delay and pulse width of the camera trigger signal.

2.6 LED Exposure Control

The LED Exposure Control supports LED selection, and the adjustment of the delay and width (exposure) of the LEDs. The output from the LED Exposure control block is the strobe signals to the LED driver circuit. The FPGA allows for the LED strobes from the DLPC300 to pass through unmodified in the video modes or modified when in the pattern modes. In the video modes the LED timing is controlled by the DLP display sequence stored in the DLPC300. In the pattern modes the LED timing is controlled by the FPGA. This enables the direct control of exposure time (LED on time) and strobe delay.

The DLPC300 pattern sequences are always encoded only in the green channel. In order to enable the use of any (all) of the LEDs, the FPGA translates the strobe from the DLPC300 to any selected LED channel.

3 Video Modes and Structured Light Patterns

DLP LightCrafter supports two main video modes for displaying video and structured light patterns:

1. External streaming of video data to the DLPC300 24-bit RGB parallel interface, selected by the input MUX (see Section 2.1)
   - DM365 video data
   - DVI video data
2. Stored pattern display of up to 96 pre-loaded patterns from the DLPC300's display buffer (see Section 3.2)

In streaming pattern mode, the input is real-time video data at up to 60 Hz frame rate from the 24-bit RGB interface. The DLPC300 converts the incoming data into the necessary format for display on the DLP3000 DMD. This requires decomposition of the 24-bit RGB frame image into a set of 24 bit-planes, which are then stored into the frame buffer (FB). Simultaneously, the DLPC300 sends the set of 24 bit planes from the previously loaded frame buffer to the DLP3000 DMD for display. The frame buffer rotates at the occurrence of each active VSYNC, which marks the end of a completed video frame. For a 1-bit (bit depth) streaming pattern at 60 Hz video frame rate there are 24 binary patterns per frame, which gives a binary pattern rate of 60 × 24 = 1440 patterns per second.

The frame buffer, with simultaneous write and read of the buffers is visualized in Figure 4.

3.1 Streaming Pattern Mode

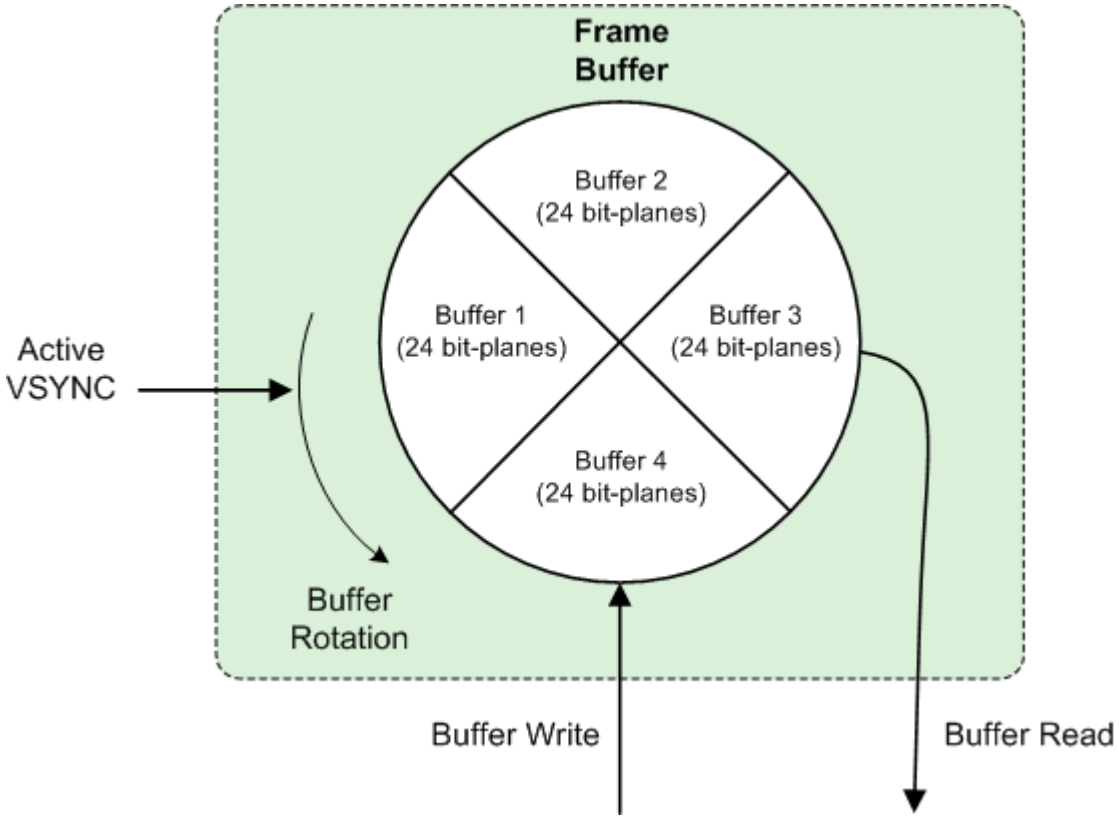

Figure 4. Frame Buffer During Real-Time Streaming Video Mode

Figure 5 shows the Hsync and Vsync relative to the buffer pointer, RD_BUF(1:0). The timing shown is for video streaming mode. These 2 signals compose a 2-bit binary value which indicates the currently active frame buffer. The key observation is that the buffer pointer transitions several horizontal lines after the Vsync rising edge.

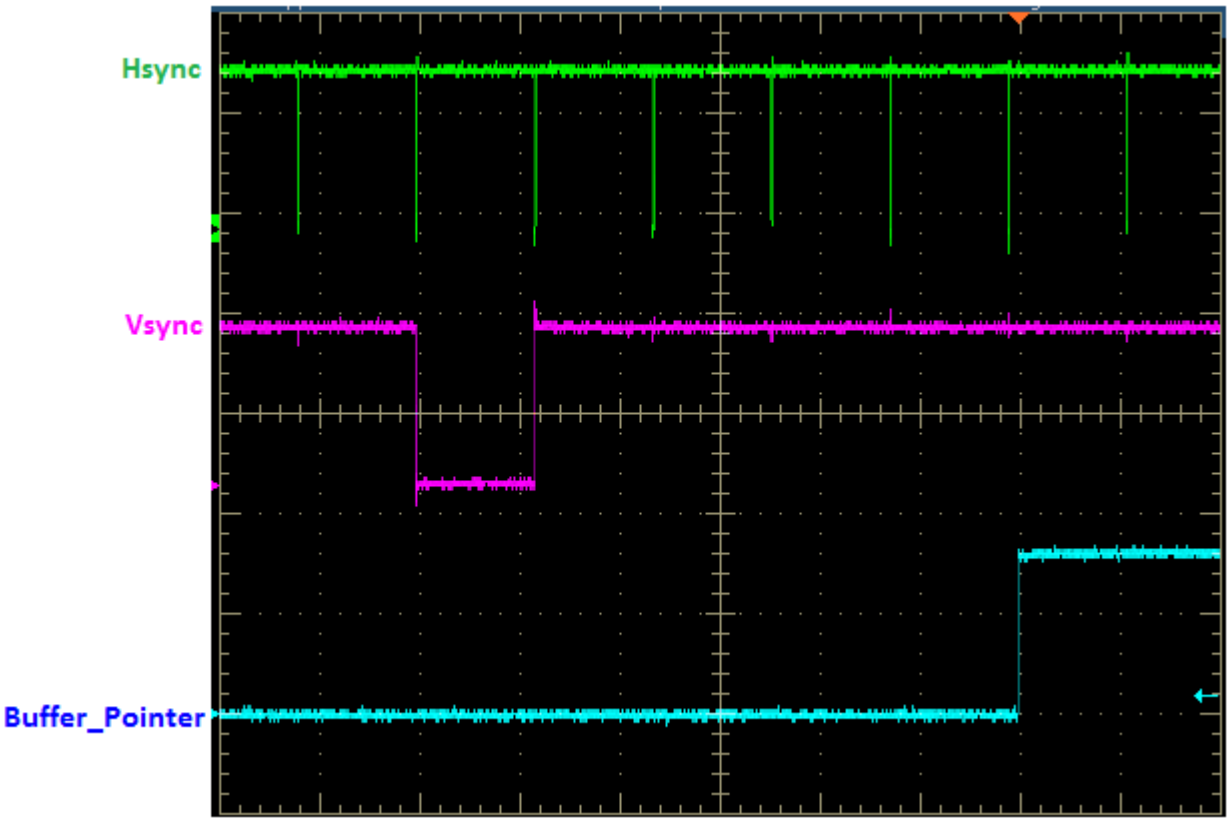

Figure 5. Waveforms Showing Hsync, Vsync and Buffer Pointer RD_BUF(0) in Streaming Mode

3.2 Stored Pattern Mode

The Internal Stored Pattern Mode enables pattern sequences of up to 96 1-bit (binary) patterns displaying at up to 4000 patterns per second. The mechanism for doing this is conceptually shown in Figure 6. The pattern buffer can be visualized as a rotating wheel (called a “circular buffer”) with four buffers of up to 24 bit-planes each. While the DLPC300 fills one buffer, the DLPC300 can simultaneously read a previously filled buffer and load it into the DLP3000 DMD array for display. A sequencer bit is stored with the last pattern saved in each buffer. When the last pattern in each buffer is displayed, this bit triggers the DLPC300 to send a BUFFER_SWAP signal to the FPGA. The FPGA then executes actions which cause the DLPC300 to rotate to the next buffer, and continue displaying the stored patterns. In this way, DLP LightCrafter displays a continuously repeated sequence of all the patterns in the buffers.

The process of buffer rotation is further explained in Section 3.3 below.

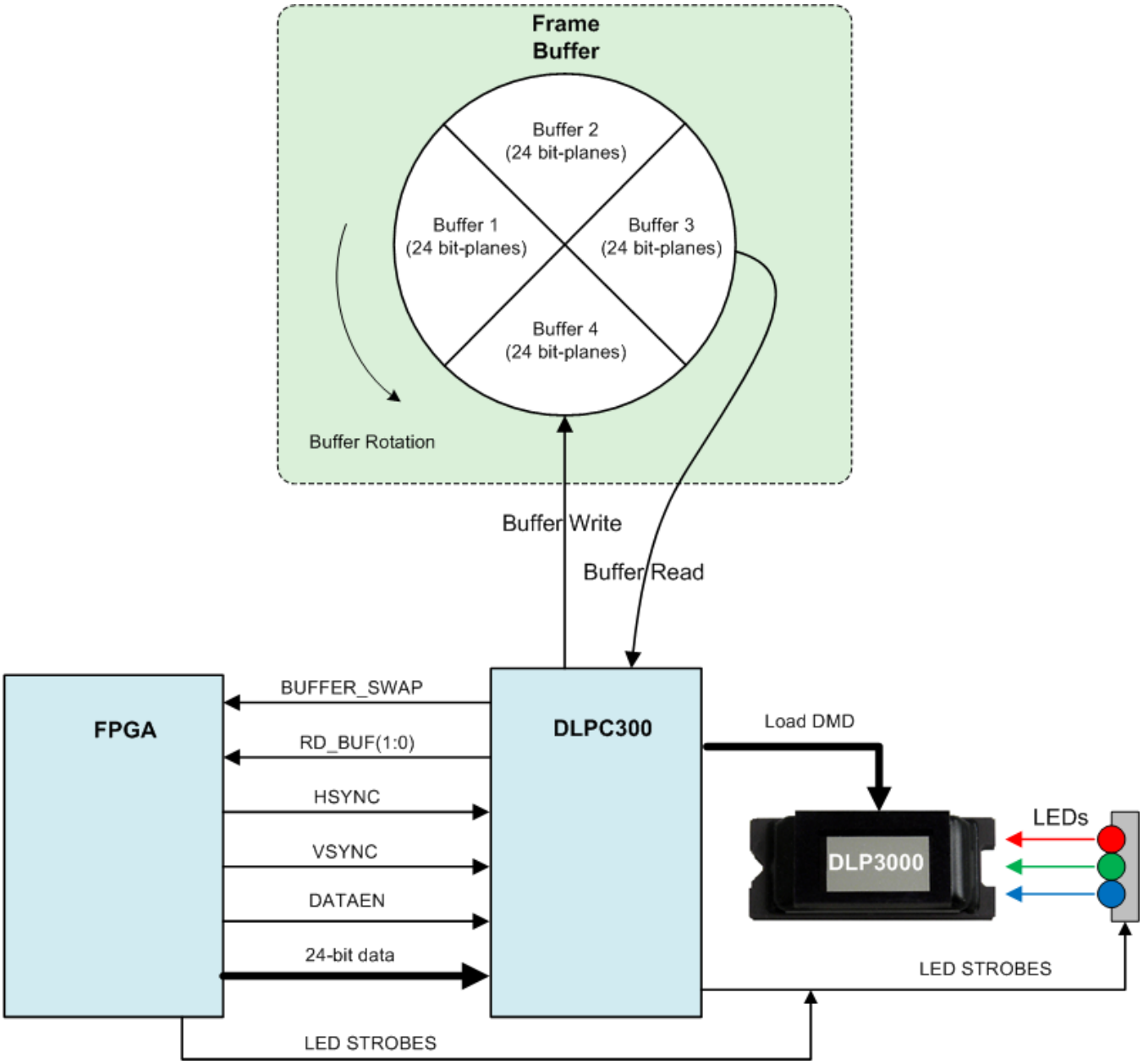

Figure 6. DLP LightCrafter Circular Buffer for Stored Pattern Display

3.3 Rotating the Circular Buffer

The VSYNC and HSYNC signals from the FPGA are used by the DLPC300 to advance the memory buffer and fill its four buffers. The RD_BUF(1:0) signals from the DLPC300 indicate to the FPGA the current buffer in use. The timing of the signals is shown in Figure 7.

The DLPC300 does the buffer loading and reading directly to and from the frame buffer memory. The FPGA controls the operation of the “circular” frame buffer. The FPGA causes the DLPC300 to do a buffer swap by sending a particular set of control signals and data to the DLPC300. The FPGA creates a “dummy” frame consisting of only two blank horizontal lines followed by a VSYNC. No stored pattern data passes through the FPGA during the internal stored pattern display.

The HSYNC signal brackets the horizontal lines of image data (800 total pixels/608 active pixels) from the 24-bit RGB Interface, and the VSYNC signal indicates the end of a frame. The HSYNC signals are 800 pixels apart, with the DATAEN signal enabling (bracketing) only the 608 active pixels. The DATAEN signal must be low when the VSYNC signal occurs. (See the DLPC300 data sheet for further explanation of the DATAEN signal.)

The DLPC300 loads data from a previously filled buffer into the DMD while simultaneously writing data into the next buffer in the rotation. The currently displayed image is delayed by a frame with respect to the currently loading frame. Once the 24-bit planes are loaded into a buffer, the circular buffer rotates to receive the next pattern.

The buffer must be filled with two blank horizontal lines to rotate (advance) to the next buffer when the next VSYNC occurs. The two blank lines must be sent at the beginning of the frame, even if non-blank lines are sent afterwards. After all 4 buffers are filled, the rotation between the buffers is accomplished by sending only two blank lines followed by a VSYNC to advance to the next buffer. The buffer rotation timing is shown in Figure 7.

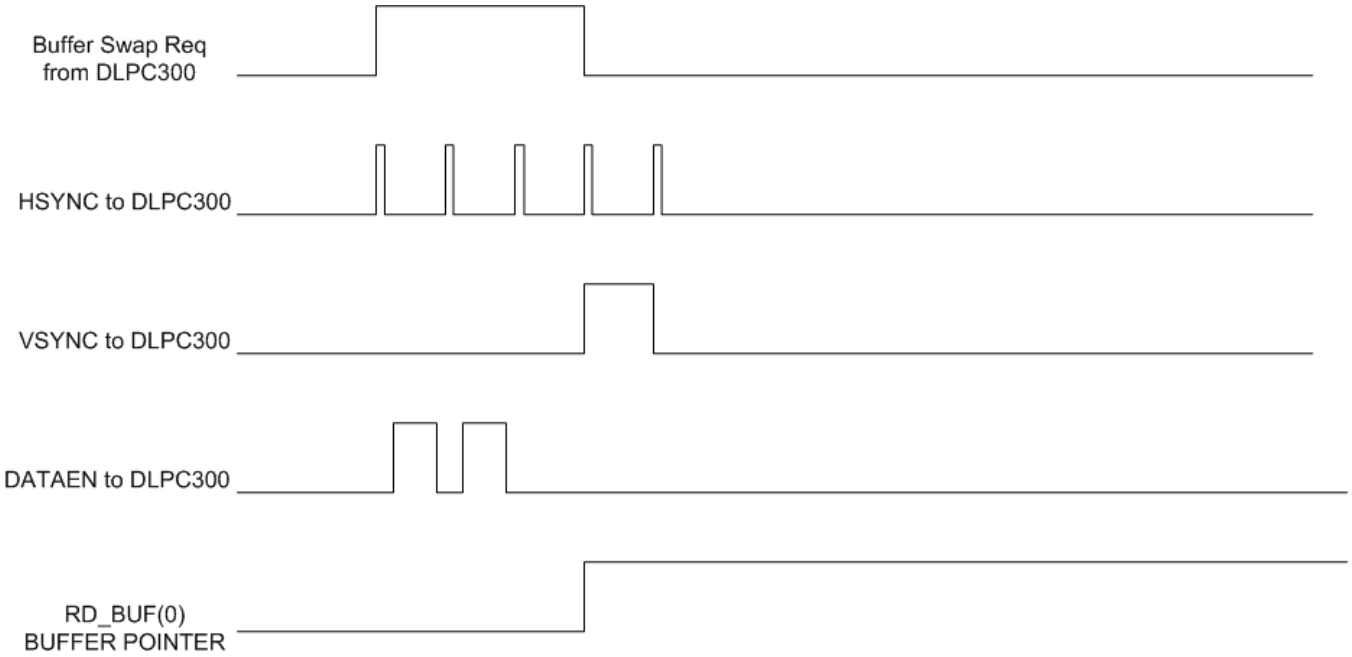

Figure 7. Buffer Swap Timing for Stored Pattern Mode

4 Conclusion

This document has been an overview of the features and functions of the FPGA used in the design of DLP LightCrafter. This document is not a full requirements document for the development of a FPGA for systems other than DLP LIghtCrafter. This effort would involve specific application and system requirements for the intended system. The method of implementation for DLP LightCrafter has been presented in overview, and should give a good starting point for the development of another implementation of a system employing the TI DLP3000/DLPC300 chipset.

For more information, see the DLP & MEMS website (http://ti.com/dlp).

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