Interfacing the ADS1202 Modulator With a Pulse Transformer in Galvanically Isolated Systems

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ABSTRACT

The ADS1202 is a precision, 80dB dynamic range, delta-sigma (ΔΣ) modulator operating from a single +5V supply. The differential inputs are ideal for direct connections to transducers or low-level signals. With the appropriate digital filter and modulator rate, this device can be used to achieve 15-bit analog-to-digital (A/D) conversion with no missing codes. This application note describes how to interface the ADS1202 with an appropriate pulse transformer and minimal external components for isolated applications.

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1 Introduction

In many industrial or high voltage applications, the transducer requires galvanic isolation from the control circuit. The measured signal must pass through an isolation barrier before it can be elaborated by a digital signal processor (DSP) or other control circuit. Digital signals are relatively easy to isolate, compared to analog signals. Consequently, new designs can place the A/D converter on the signal transducer side, and then pass the digitized value of the analog signal through the isolator.

There are many different types of galvanic isolators that can be used. Commonly used isolators include optocouplers, pulse transformers, Giant Magneto Resistive (GMR), and capacitive isolators. The type of isolator used depends on factors related to the specific application. For simplicity, high voltage isolation, immunity to disturbance, and high reliability, pulse transformers are the preferred choice for many industrial applications, including motor control. The following discussion describes one of the many possible ways to interface the ADS1202 with a pulse transformer and isolate the incoming signal from $\Delta\Sigma$ modulator to the control board.

2 Interfacing the ADS1202 With a Pulse Transformer

As with ordinary A/D converters, the analog signal connected to the input of the ADS1202 delta-sigma modulator is digitized by applying a conversion clock signal. The result of the conversion (or modulation) is the data output signal from the delta-sigma modulator.

The receiver, DSP, or other control circuit must sample the output data signal from the modulator at precise moments in time. To do this, a clock signal at the receiver is needed in order to synchronize with the clock signal at the transmitter. In fact, the delta-sigma modulator, the receiver, and the filter circuits must all be synchronized in order to receive proper data.

An ideal solution is a delta-sigma modulator with a flexible interface, such as the ADS1202, which can provide various output formats. The specific output format is selected with mode control pins M0 and M1.

2.2 Operating Modes and Output Signals of the ADS1202

In most applications where a direct connection is realized between the delta-sigma modulator and DSP or µC, two standard output signals (MDAT and MCLK) are available. The MDAT and MCLK output signals provide the easiest means of connecting the data and clock signals to the host.

The ADS1202 has four user-selectable operating modes. The first three modes use an internal conversion clock source, and are well suited to transformer-coupled design applications. Mode 0, 1 and 2 operations are discussed here. Mode 3 requires an external clock to be fed to the ADS1202, making it impractical for transformer-coupled applications. Mode 3 operations will not be discussed in this application note.

- **Mode 0**

In Mode 0, input control signals M0 and M1 are both LOW. The control signals enable an internal RC oscillator that provides a conversion clock source (IntCLK) to the code generator block. The source for the output signal (MDAT) is the signal arriving directly from the delta-sigma modulator. MCLK is an output in Mode 1, and has a frequency of IntCLK/2. In this mode, the DSP or µC reads MDAT data on every rising edge of the MCLK output clock.

- **Mode 1**

In Mode 1, the input control signal M0 is HIGH and M1 is LOW. As in Mode 0, the internal RC oscillator provides a conversion clock source (IntCLK) to the code generator block, and the source for the output signal (MDAT) is the signal arriving directly from the delta-sigma modulator. MCLK is again an output signal, but has a frequency of IntCLK/4. In this mode, the DSP or µC reads MDAT data on every edge (rising and falling) of the MCLK output clock.

- **Mode 2**

In Mode 2, the input control signal M0 is LOW and M1 is HIGH. Once again, the internal RC oscillator provides a conversion clock source (IntCLK) to the code generator block. The output code from the delta-sigma modulator is also passed through the code block generator where it is combined with the conversion clock. A twinned-binary coding is implemented, and MDAT is presented as a split-phase or Manchester encoded signal. Since the clock and data are combined into one signal, the ADS1202 output must be decoded before the DSP or µC can process the information.

2.3 ADS1202 MDAT and MCLK Output Signals

Figures 1 and 2 present the output signals from ADS1202 operating in Mode 0. The MCLK signal has constant frequency between 8MHz and 12MHz and a fixed 50% duty cycle.
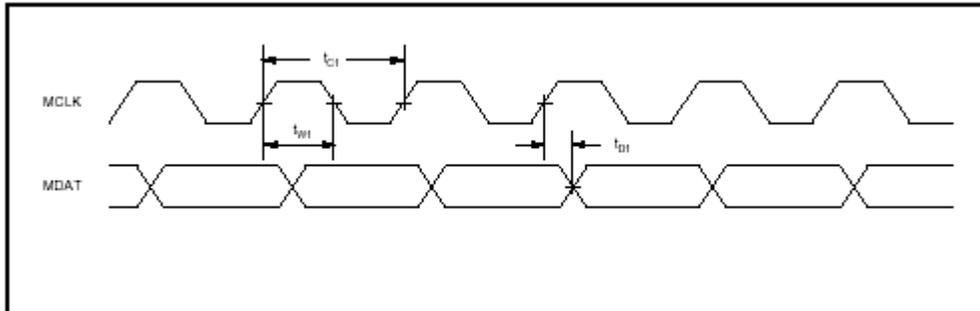

Figure 1.   Output Signals From ADS1202 Operating in Mode 0

The MDAT signal is a digitized representation of the analog input. Unlike the MCLK signal, it does not have a fixed frequency or duty cycle. The duty cycle is a variable function of the input analog signal (see Figure 2).
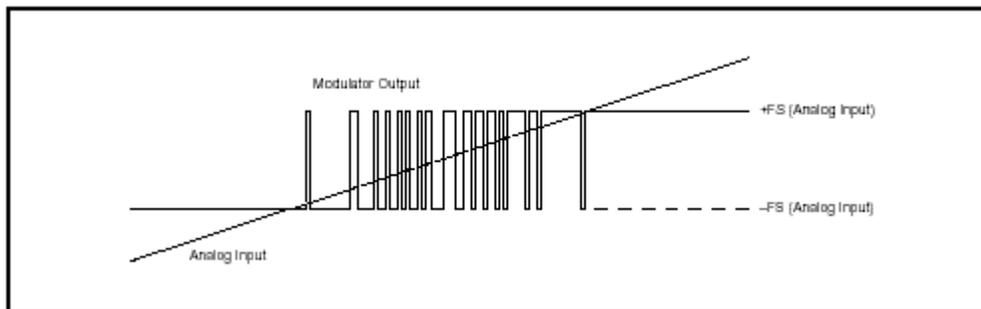

Figure 2.   Analog Input Versus Modulator Output of the ADS1202

2.4 Transformer Connections

With the output signal from the ADS1202, as shown in Figure 2, the transfer of the signal can be done only using edge detection. The variable frequency and duty cycle of the MDAT signal will cause the pulse transformer to saturate. To avoid saturating the transformer magnetics, the circuits shown in Figure 3 and 4 can be used.

The output stage of the ADS1202 is capable of driving a high current pulse (up to 20 mA), and can easily drive capacitor and primary transformer winding shown in Figure 3. The resulting positive and negative pulses are transferred to the secondary winding, which is connected directly across the input and output of a Schmitt-trigger inverting buffer (Figure 3), or differential input of line receiver (Figure 4).
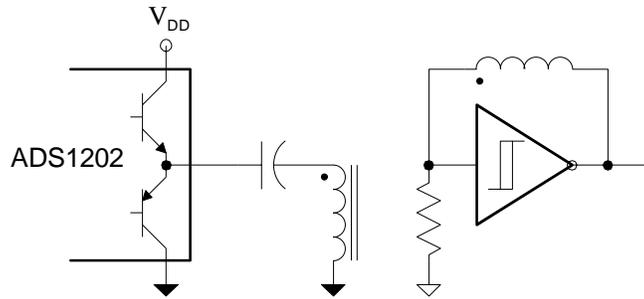
Figure 3. Output Signal Transfer Through Pulse Transformer and Schmitt-Trigger Inverter
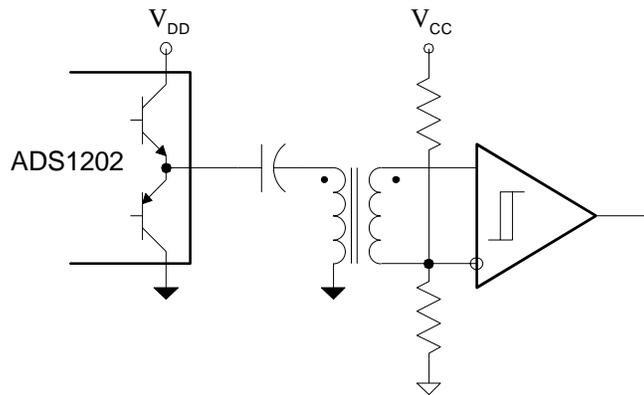

Figure 4. Output Signal Transfer Through Pulse Transformer and Differential Line Receiver

Using the general equivalent transformer circuit from Figure 27 (see **Appendix**), and transferring parallel and serial impedances to the primary side, the resulting equivalent circuit is presented in Figure 5.
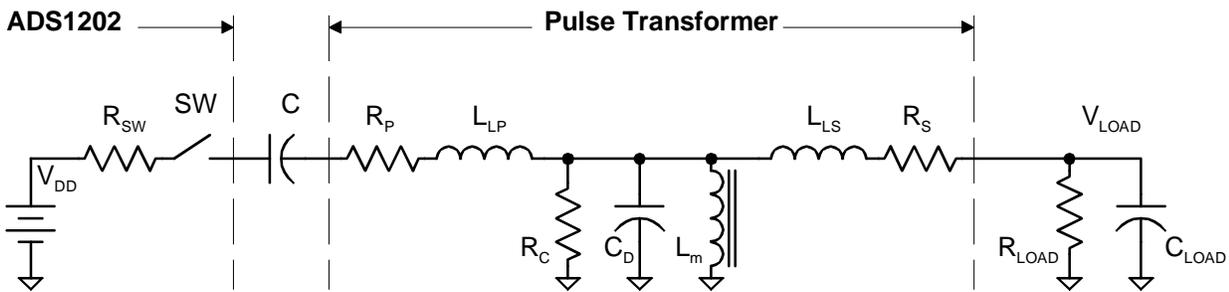
Figure 5. Equivalent Circuit of Figures 3 and 4

The power supply of the ADS1202 is presented as V_{DD}. Equivalent resistance of the output switch (SW) is represented as R_{SW}. Capacitor C, on the output of the ADS1202, is blocking the DC component of the MDAT signal, creating controlled AC pulses on the transformer primary winding. The load resistor is presented as R_{LOAD} and input capacitance of the Schmitt trigger inverting buffer, or differential line receiver, as C_{LOAD}.

Using the equivalent circuit from Figure 5, it is possible to analyze four different parts of the transferred signal: positive pulse rising edge, positive pulse peak response, negative pulse rising edge and negative pulse peak response. Each of these parameters is discussed in more detail in the following sections.

2.5   Positive Pulse Rising Edge Response

At t_0, the switch SW closes. At that moment, the capacitor C has an initial charge of 0V. Since the value of C is much larger than the equivalent distributed and load capacitance, it can be ignored for rising transient analysis. Winding resistances are also negligible compared to the source and load resistances and will not be taken into consideration. The magnetizing inductance effectively represents infinite impedance to the instantaneously changing input voltage and will also be disregarded. The resulting equivalent circuit is presented in Figure 6.
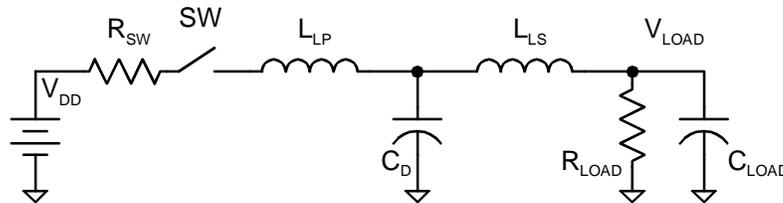

Figure 6.   Rising Edge Equivalent Circuit

The waveform resulting from the circuit presented in Figure 6 is shown in Figure 7. The extent of the overshoot and waveform rise time both depend on the relative value of the resistive, capacitive, and inductive components in the circuit.
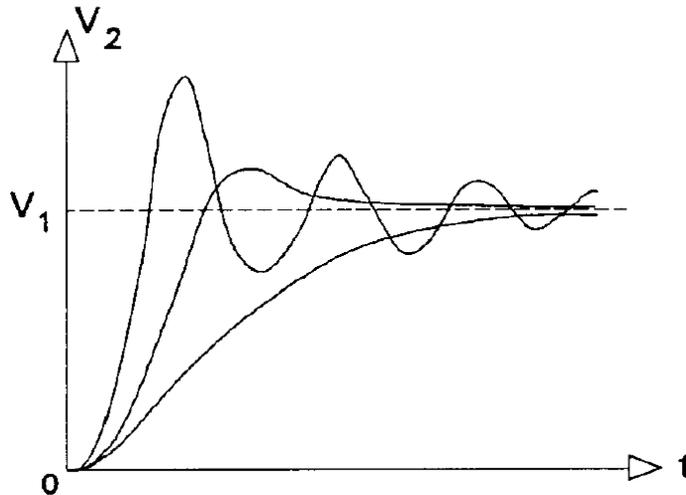
Figure 7.   Rising Edge Waveform

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2.6 Positive Pulse Peak

When the rising edge transient dies away, you enter the second stage of the applied ideal pulse peak. The load peak voltage is $V_{LOAD}=K*V_{DD}$. Figure 8 represents the equivalent circuit that determines the peak load voltage.
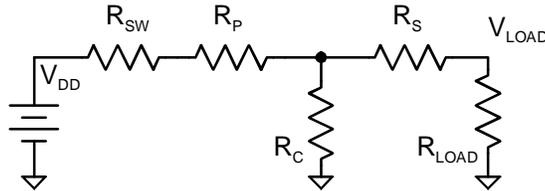

Figure 8.   The Load Peak Voltage Circuit

The peak output voltage can be now calculated using equations 1 and 2:

$$V_{LOAD} = k \times V_{DD}$$

Equation 1

$$k = \frac{R_{LOAD}}{R_{LOAD} + R_S} \times \frac{\dfrac{R_C \times (R_S + R_{LOAD})}{R_C + R_S + R_{LOAD}}}{R_{SW} + R_P + \dfrac{R_C \times (R_S + R_{LOAD})}{R_C + R_S + R_{LOAD}}}$$

Equation 2

When the peak load voltage is determined, it is possible to evaluate the components that determine the positive peak response. Capacitor C determines the shape of the output signal. By manipulating the value of C, it is possible to obtain the desired shape of the output signal. The equivalent circuit from Figure 9 helps determine optimum values of external components and obtains the desired waveform from the applied pulse-transformer.
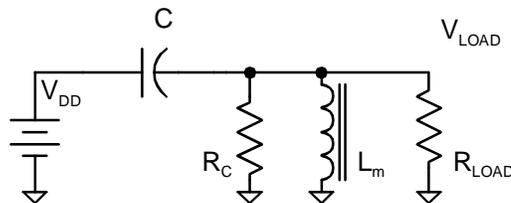
Figure 9.   Positive Peak Equivalent Circuit

2.7 Negative Pulse Rising Edge Response

Using a similar analogy as presented in the positive pulse analysis, it is possible to determine the characteristics of the negative rising edge of the output signal. Capacitor C was previously fully charged at the power supply voltage V_{DD}. With the new equivalent circuit of Figure 10, capacitor C is now represented as a voltage source on the primary side of the transformer.
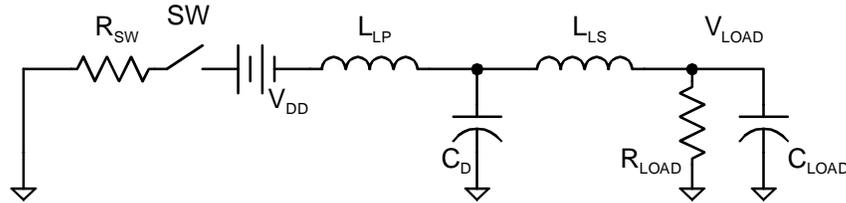

Figure 10. Negative Rising Edge Equivalent Circuit

2.8 Negative Pulse Peak Response

The negative peak equivalent circuit is shown in Figure 11. The initial voltage on capacitor C must be added in the equation describing negative peak voltage.
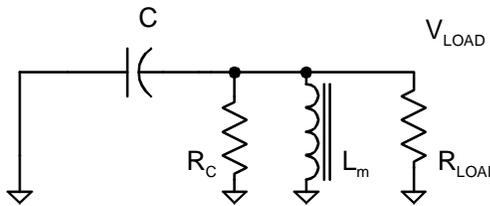

Figure 11. Negative Peak Equivalent Circuit

3   Practical Test Results

To verify the information previously explained, a surface-mounted pulse transformer, SC979-03, from Scientific Conversion Inc. was chosen for the test. This transformer has the following characteristics:

Primary to secondary winding ratio (1:n)	1 : 1
Primary inductance (L_{LP})	0.160μH
Leakage inductance (L_m)	300μH
Interwinding capacitance (C_{WW})	2pF
U-t product	35μVs
Primary resistance (R_P)	0.1Ω
Bandwidth	32kHz – 160MHz
Primary to secondary voltage isolation	1kV_{DC}
Voltage rise time	1.8ns

The circuit from Figure 12 is realized. The ADS1202 is operating in Mode 1, where MCLK signal is 5MHz. Primary capacitor C has a value of 0.1μF.
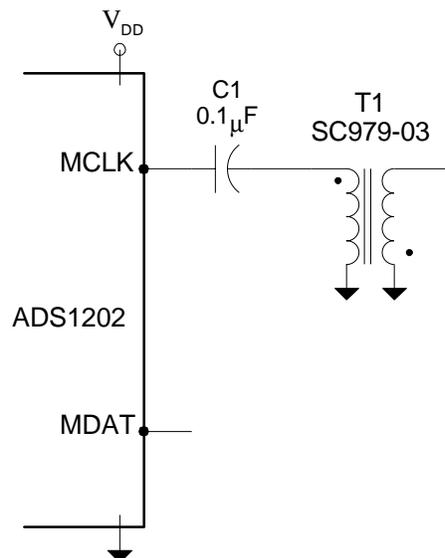
Figure 12.   Open Circuit Pulse Transformer Test

Figures 13-16, 18 and 20 present different waveforms where channel 1 is the output signal from ADS1202, channel 2 is transformer primary voltage, and channel 3 is the output signal or transformer secondary voltage.

Figure 13 shows waveforms for the configuration from Figure 12. Figure 14 and Figure 15 present more details on the falling and rising edge of the input and output signal for the same configuration.
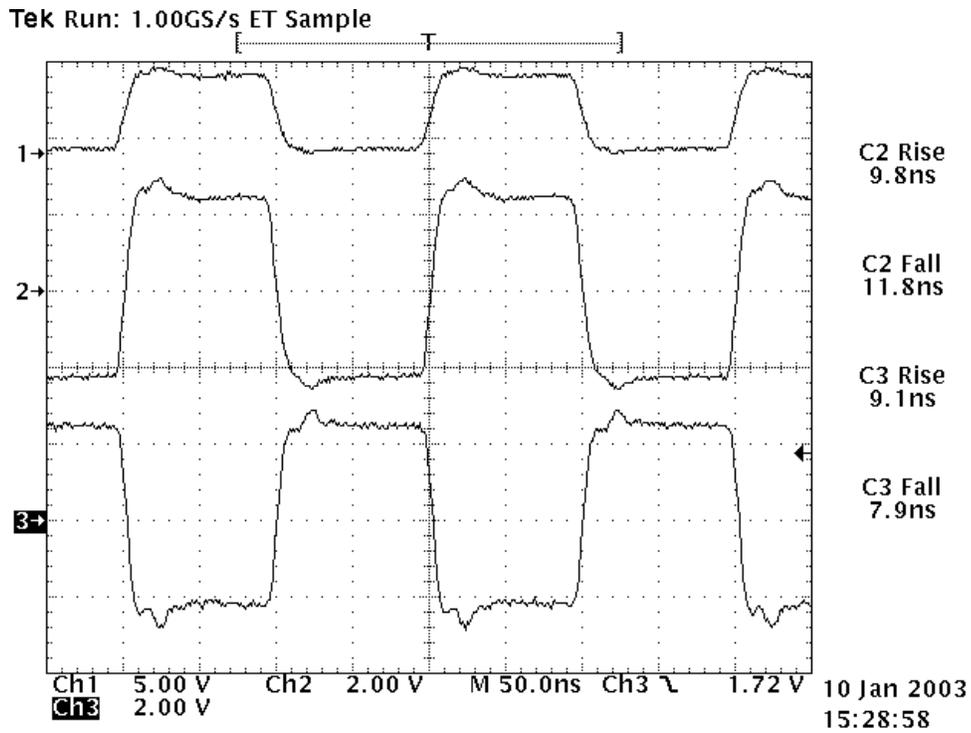

Figure 13. Open Circuit Pulse Transformer Test Waveforms

Tek Run: 5.00GS/s ET Sample

C2 Rise
9.62ns

C2 Fall
11.32ns

C3 Rise
8.76ns

C3 Fall
7.68ns

Ch1 5.00 V   Ch2 2.00 V   M 10.0ns Ch3 ⌐ 1.72 V   10 Jan 2003
Ch3 2.00 V   15:34:29

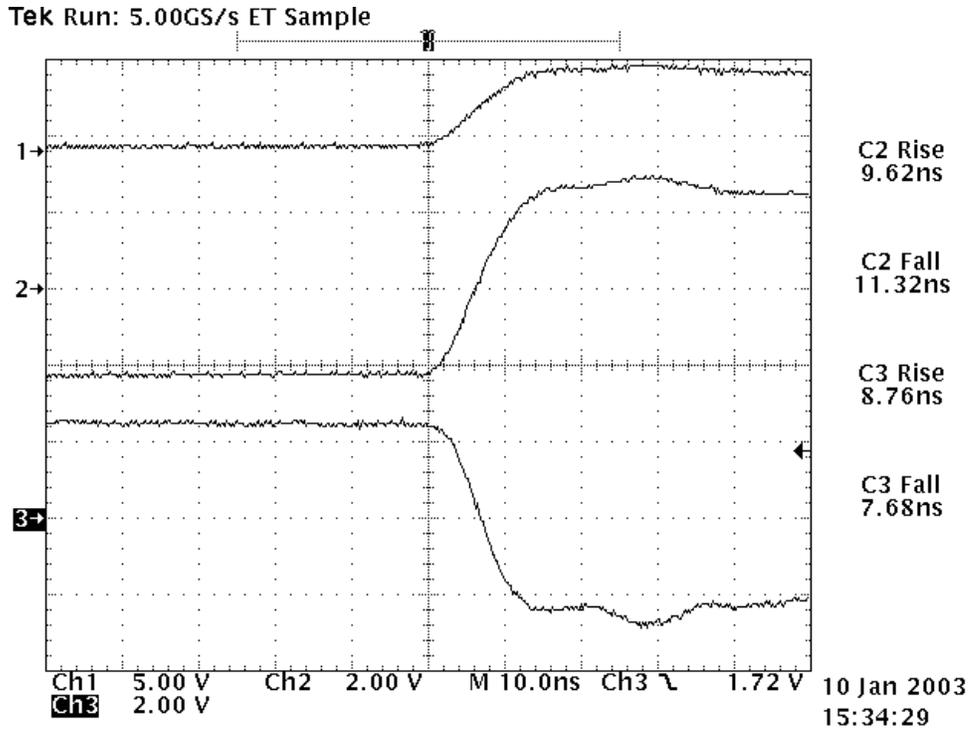**Figure 14.   Falling Edge of the Output Signal for Open Circuit Test**

Tek Run: 5.00GS/s ET Sample

C2 Rise
9.82ns

C2 Fall
10.74ns

C3 Rise
8.68ns

C3 Fall
7.14ns

Ch1 5.00 V   Ch2 2.00 V   M 10.0ns Ch3 ∫ 1.72 V   10 Jan 2003
Ch3 2.00 V   15:35:17
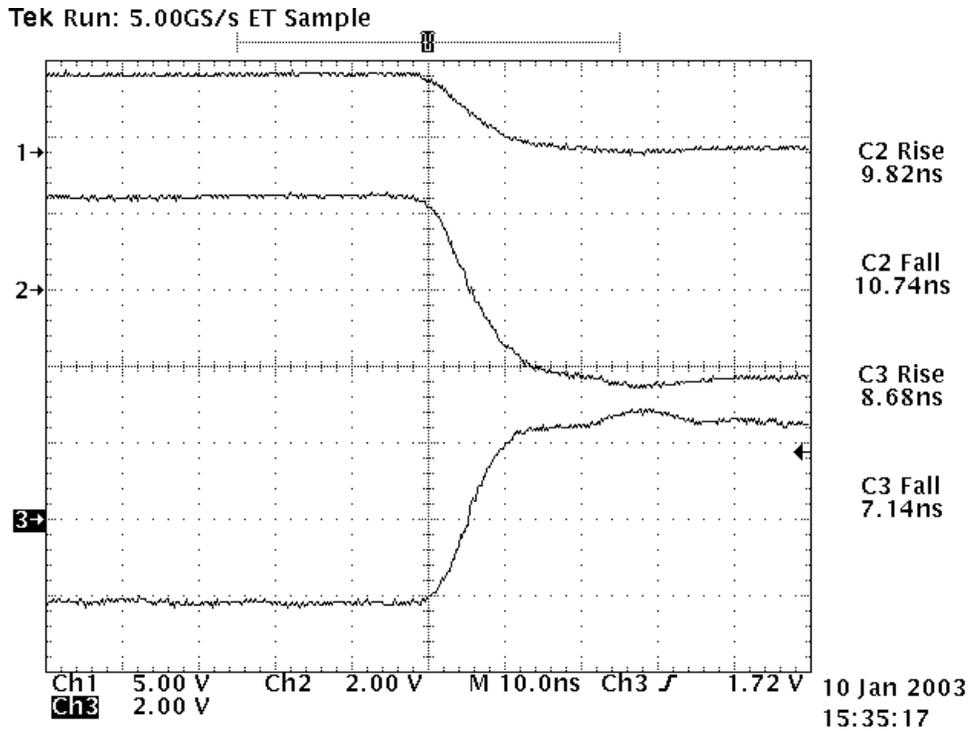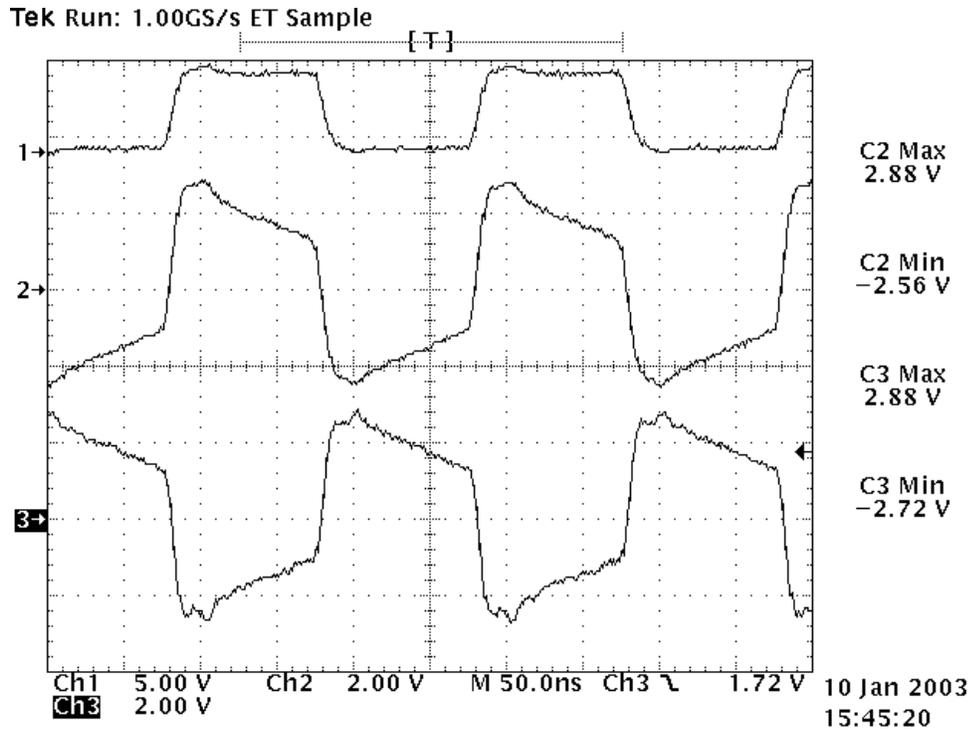
Figure 15.   Rising Edge of the Output Signal for Open Circuit Test

To obtain the required waveform, the input capacitor is reduced and the new value of 100pF is tested. Figure 16 presents the same waveforms from Figure 13. The only difference is that capacitor C1 from Figure 12 is now 1000 times smaller.

Figure 16.   Open Circuit Pulse Transformer Test Waveforms With Small Blocking Capacitor

The output signal is still not optimal. To accelerate the charging of capacitor C1, resistor R1 is added in parallel with primary winding of the transformer. The new test circuit is now presented in Figure 17.
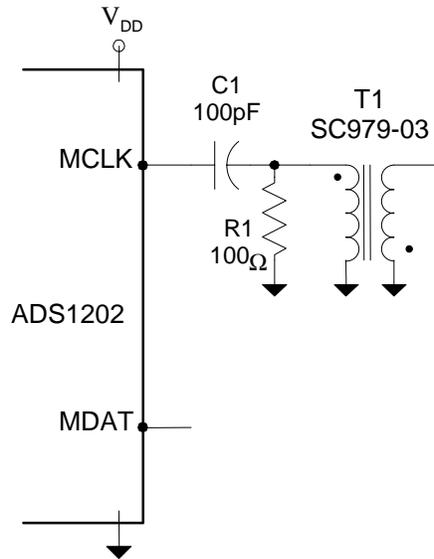
Figure 17.   Open Circuit Test of Pulse Transformer With Added Components for Shape Forming

The resulting waveform, compared to Figure 13 and Figure 16, is shown in Figure 18.
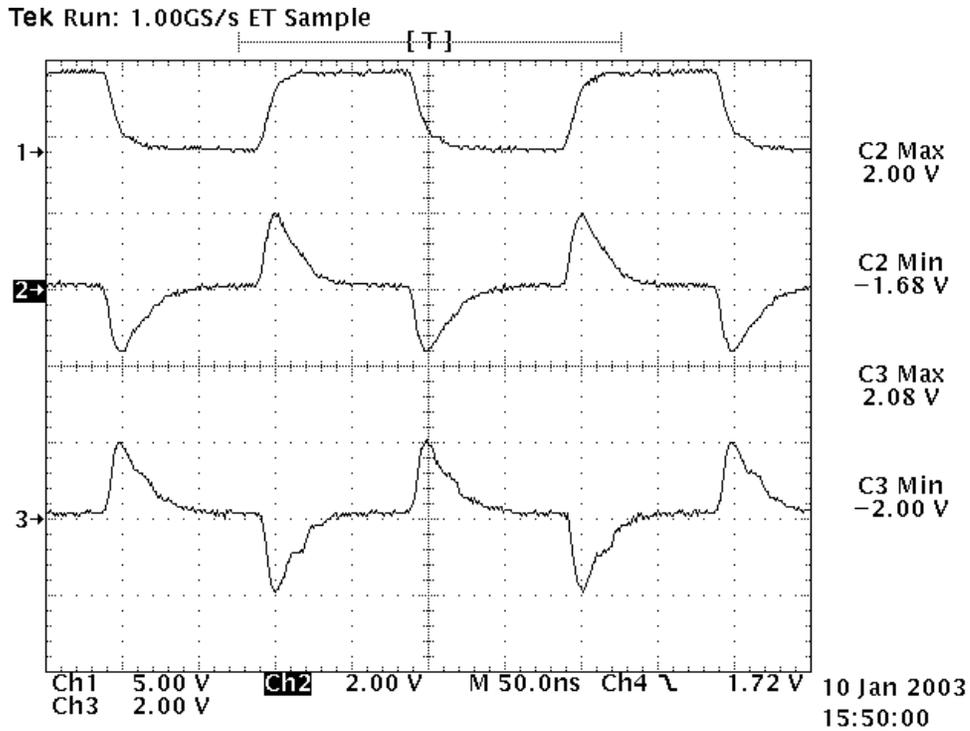
Figure 18.   Desired Open Circuit Waveforms of the Pulse Transformer

To simulate an output load from a Schmitt trigger circuit SN74LVC2G14, or differential line receiver, the 10K-ohm resistor in parallel with a 20pF capacitor is added in parallel with the secondary winding of the transformer. The final test circuit is shown in Figure 19.

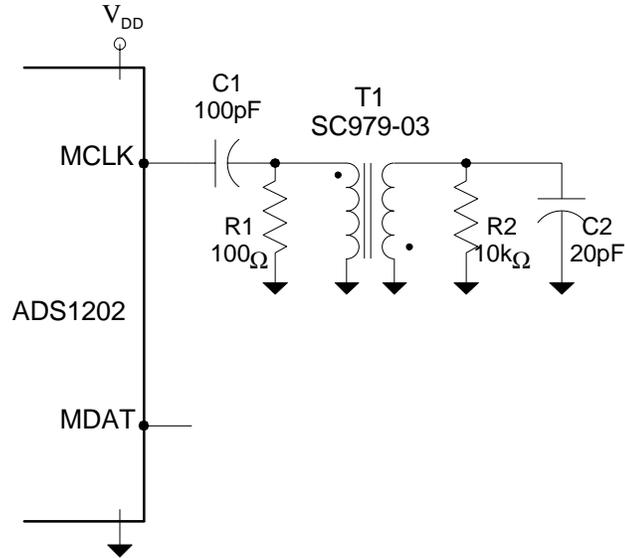**Figure 19.   Final Test Circuit for Pulse Transformer**

The final results for the circuit from Figure 19 are shown in Figures 20 through 22.

Figure 20.   Final Waveform on the Pulse Transformer
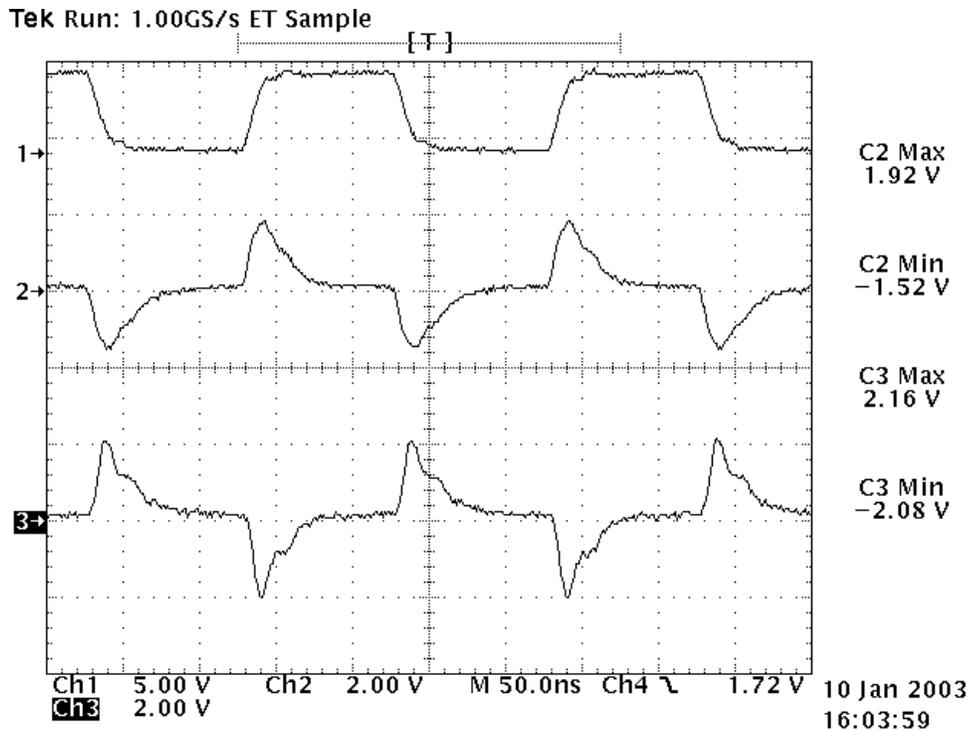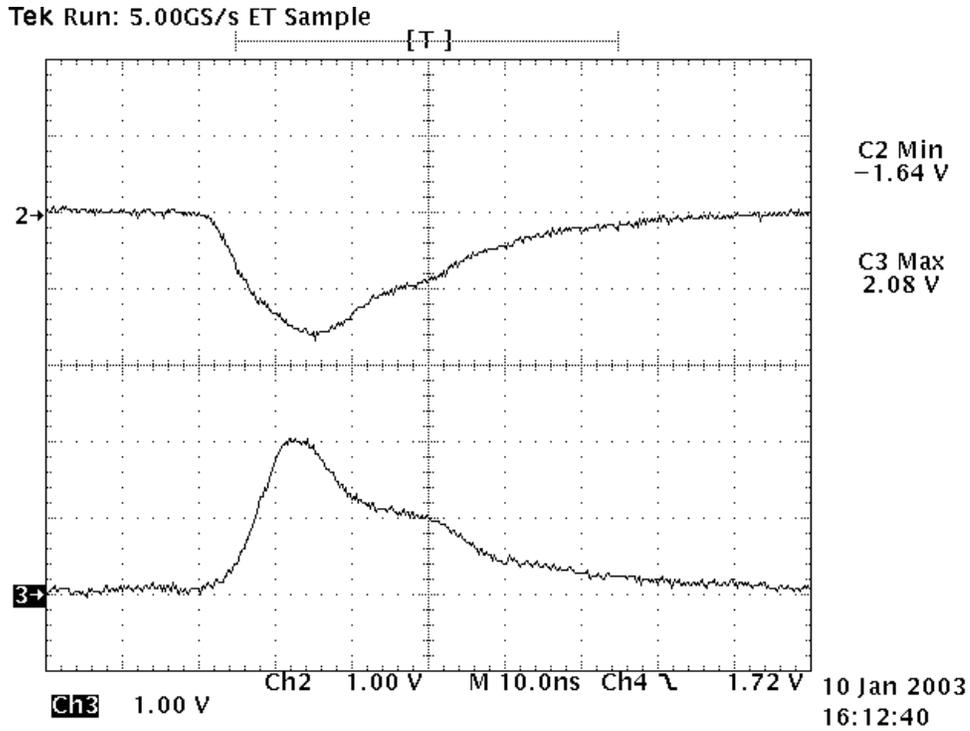
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Figure 21. Falling Edge of Transformer Primary Signal and Rising Edge of the Secondary Signal
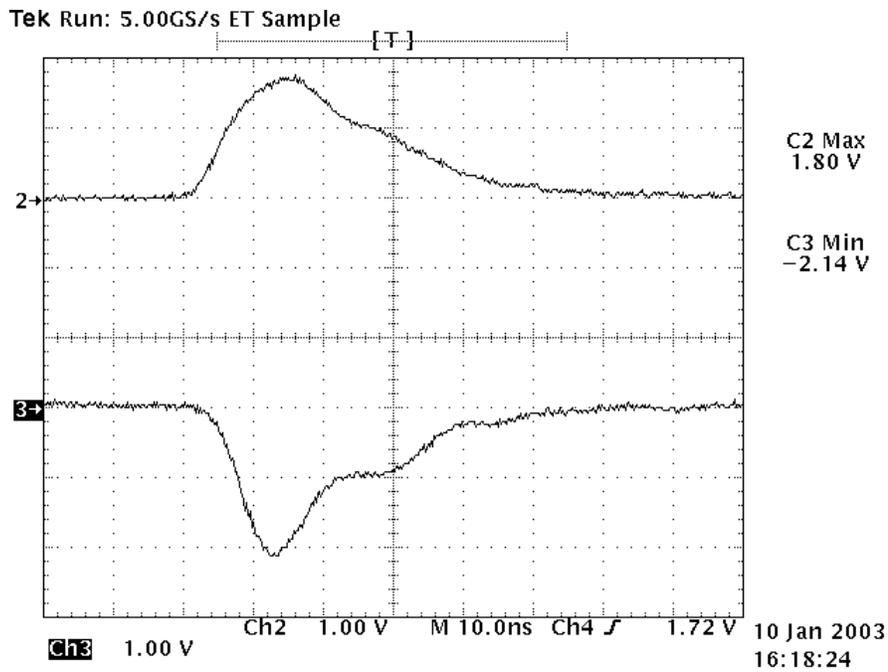
Figure 22. Rising Edge of Transformer Primary Signal and Falling Edge of the Secondary Signal
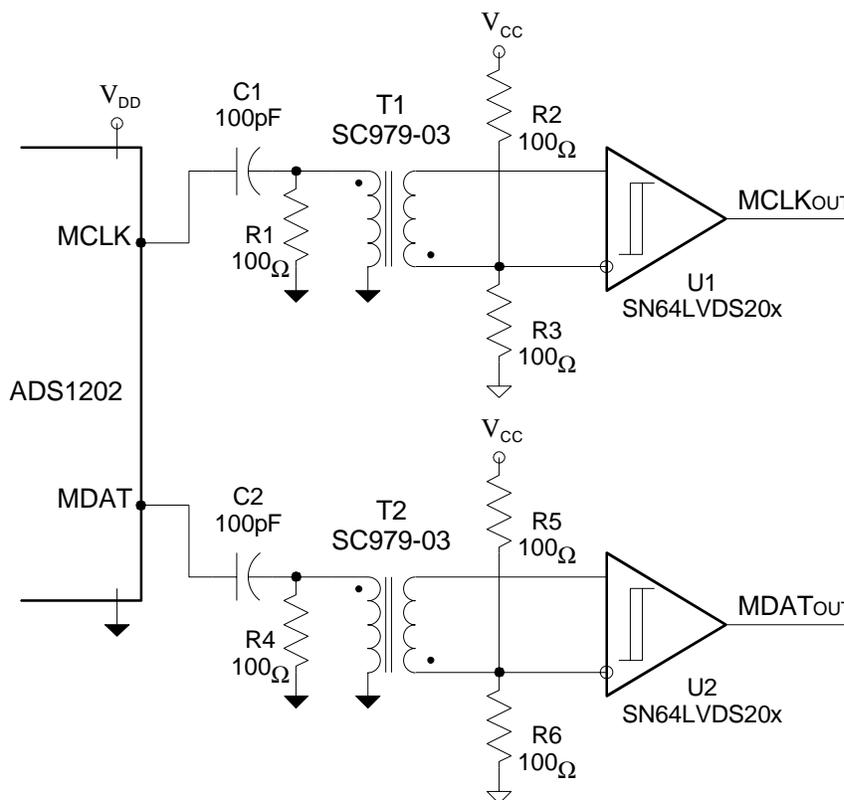
Figure 23. Proposed Pulse Shaping Circuit With Pulse Transformer for ADS1202 Outputs

The final differential line receiver circuit of Figure 23 uses a 100pF capacitor in series with the transformer primary. The transformer is a Scientific Conversion component (part no. SC979-03). The differential line receiver is a LVDT device (SN65LVDT34D) with a 50Ω resistor between the inputs.

Figures 24 through 26 present different waveforms where channel 1 is the output signal from ADS1202, channel 2 is the transformer primary voltage, channel 3 is the transformer output signal or transformer secondary voltage, and channel 4 is the output of the differential line receiver.

Tek Run: 1.00GS/s   Sample
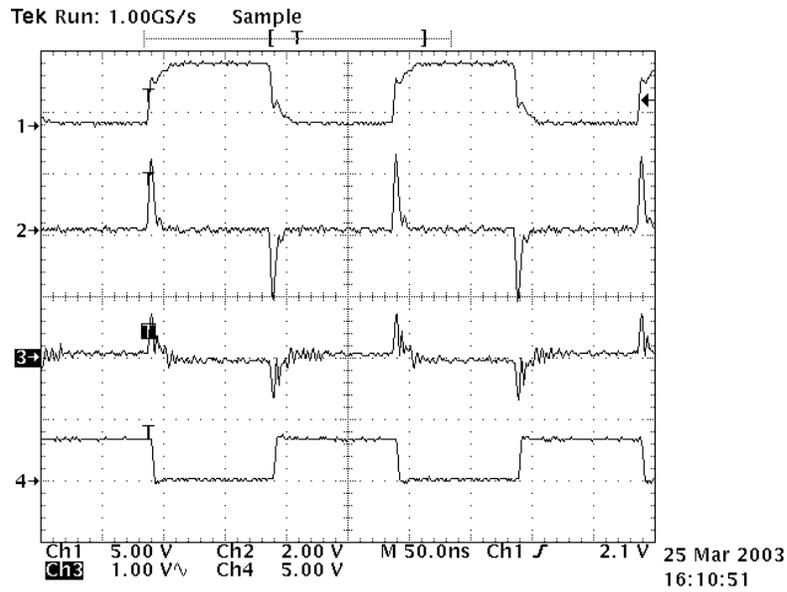
Figure 24.   Waveforms of the Circuit From Figure 23

Tek Run: 4.00GS/s ET Sample   PrTrig
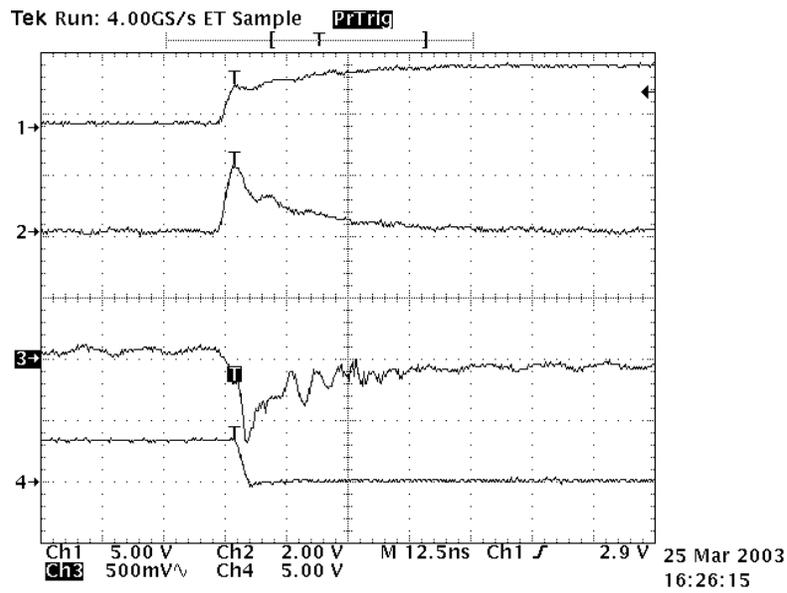
Figure 25.   Rising Output Edge of the Circuit From Figure 23
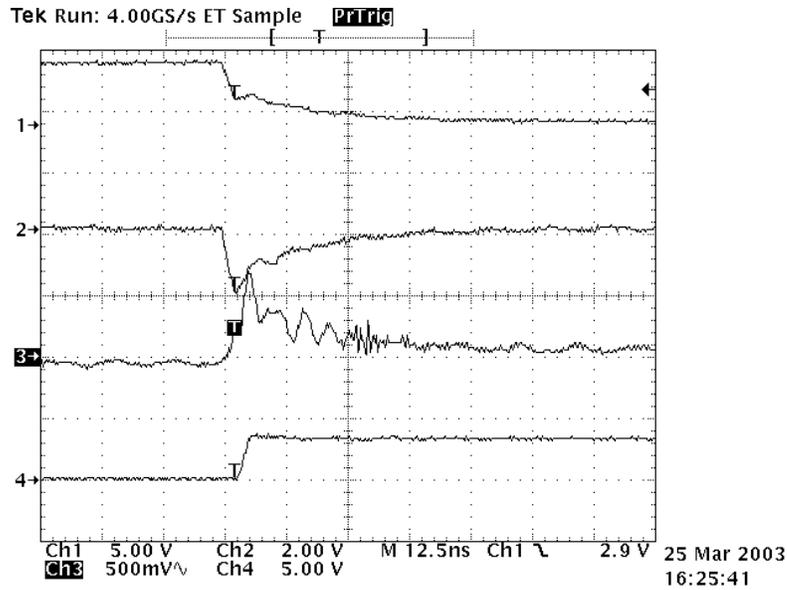
Figure 26.   Falling Output Edge of the Circuit From Figure 23

Conclusion

The transformer chosen for demonstrating the circuit described in this application note is not recommended for high-voltage industrial applications, but by using the methods described here, the ADS1202 can easily be adapted for use in galvanically isolated systems. The isolated digital signal from the dual LVDT receiver can interface directly to 3.3V processors for additional filtering/decoding.

APPENDIX

4 Transformer Equivalent Circuit

4.2 Finite Permeability

The core magnetization current that flows through the primary winding to maintain the core flux is called finite permeability. The i_m is the core magnetization current, and is in phase with the primary coil current. This additional current is represented in our equivalent circuit by placing an inductance L_m in parallel with the primary coil shown in Figure 1.

4.3 Core Losses

The hysteresis and eddy loss terms can be combined to produce a useful approximation for core loss. To use model core loss as resistance, R_C in parallel with the primary winding as shown in Figure 1 is added. To reduce core losses we can use either a material with a high receptivity or a core construction type that impedes the flow of eddy currents.

4.4 Winding Resistance

The wire that is used to wind the transformer coils has a non-zero resistance, which will cause ohmic losses in each of the windings. Including this effect in the equivalent circuit requires series resistance to be added to each coil, as shown in Figure 1.

4.5 Leakage Flux

The general case of not all flux is completely linking both coils. To include the effect of the leakage flux in the equivalent circuit, add an inductance in series with the ideal primary coil as shown in Figure 1. The same reasoning applies equally to the secondary coil. Winding techniques and core geometry will affect the magnitude of leakage inductance.

4.6 Distributed Capacitance

The most significant source of parasitic capacitance is the capacitance that appears across a winding due to coupling between the coil wire and the transformer core. A secondary capacitance effect is caused by the capacitance between a coil turn and adjacent turns, although this effect is usually small as the turn-turn capacitance sum in series rather than in parallel. To model this distributed winding capacitance we add a lumped capacitance across each ideal coil in the transformer equivalent circuit as shown in Figure 1.

4.7 Inter-Winding Capacitance

The proximity of primary and secondary windings in a transformer gives rise to a capacitance between the windings. Usually this capacitance is very small in comparison with the transformer inductance. If the transformer is exposed to high common mode voltage change, dV/dt, as is common in motor control applications, this capacitance cannot be ignored.

4.8 Combined Equivalent Circuit

Combining all the non-ideal factors described in this section, you can obtain the general equivalent transformer circuit shown in Figure 27.
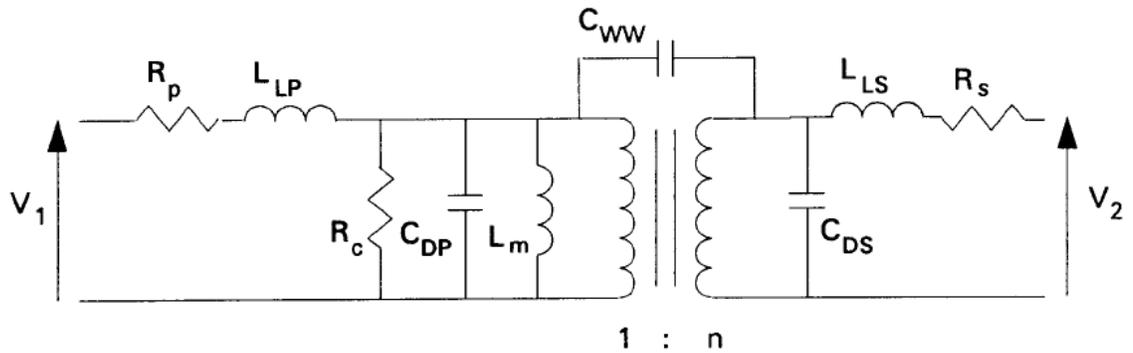
Figure 27.   General Transformer Equivalent Circuit

Using the equivalent circuit from Figure 27, it is then possible to calculate all parameters of the output pulse waveform from the transformer.

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