Application Report
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Reading Data from the ADS7862

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ABSTRACT

This application note presents a method for interfacing multiple ADS7862 12-bit SAR analog-to-digital converters (ADCs) to the parallel data bus of a host processor. Care must be taken when multiple devices share the data bus in order to maintain the integrity of channel sampling information.

Contents

1 Introduction

The ADS7862 is a 2+2 channel, 12-bit parallel version of the ADS7861. The device features two independent ADCs, each with a two-channel mux. Besides the parallel interface, a major difference between the devices is the output data format. The ADS7861 provides conversion channel information in a serial output data stream; the ADS7862, however, does not contain this information.

2 ADS7862 Design Problem

Assume three ADS7862 data converters share a common data bus. Each device can be independently ***chip-selected*** by means of a simple address decoding scheme. The start of conversion to all devices could be simultaneous or independent, but is controlled by an external source. We will also assume the BUSY signal from each ADC maps to an external interrupt pin of the host controller. The block diagram of Figure 1 represents the basic interface and assumptions.

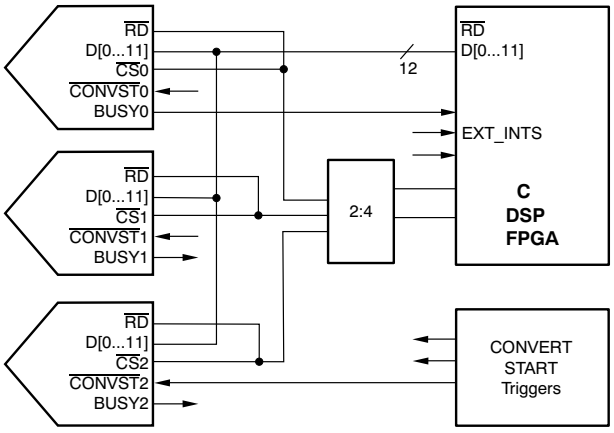

Figure 1. Hardware Interface Block Diagram

3 Parallel Interface of the ADS7862

Taking a closer look at Figure 1, one might notice that the $\overline{RD}$ pin on each device is connected to the device chip select ($\overline{CS}$) pin. The reason for this connection is to maintain data channel selection integrity.

Typically, a host processor such as a DSP will have an active-low read strobe ($\overline{RD}$) that is used for strobing the read pin of external devices; thus, one might ask, “Why can’t we use that for the ADS7862?” The reason for not using this option is because the ADS7862 does not internally validate the $\overline{RD}$ strobe with the device $\overline{CS}$ pin. If the configuration shown in Figure 1 tied a common $\overline{RD}$ strobe to all three devices, each part in the chain would increment its read pointer regardless of whether it was chip-selected or not.

The only way to ensure channel data integrity is to strobe $\overline{RD}$ only while the device is chip- selected. The first read cycle will be from Channel 0 and the second from Channel 1. The channel pair (pair A or B) is determined by the state of the A0 pin. Since there is no set-up or hold time minimums for the relationship of $\overline{RD}$ and $\overline{CS}$, the pins can be tied together as shown in Figure 1, provided the signal is pulsed low for a minimum of 30ns.

The ADS7862 datasheet (SBAS101) shows several timing diagrams related to the individual control of the $\overline{RD}$ and $\overline{CS}$ pins, Figure 2 shows two alternative methods of reading data from the ADS7862 when sharing a parallel data bus with additional peripherals. Option 1 depicts a standard $\overline{RD}$ strobe logically ***OR’d*** with the device chip-select. Option 2 proposes a decoded address scheme that ties $\overline{CS}$ and $\overline{RD}$ together and feeds the signal to both pins simultaneously.

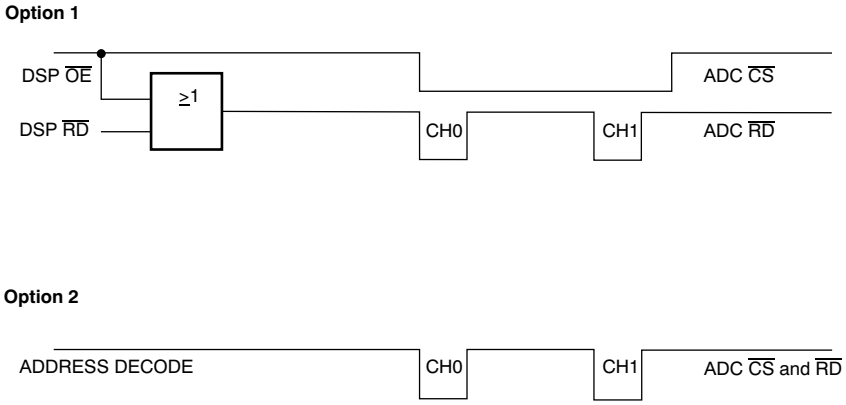

Figure 2. Alternate Control Options

4 Conclusion

Our simple design example above assumes multiple ADS7862 devices sharing a common data bus. In reality, this information pertains to any additional parallel device which might share common strobes such as an output or read enable. When sharing a common data bus and control signals with other peripherals, the ADS7862 should have its $\overline{RD}$ pin connected to or gated by the device $\overline{CS}$ pin.

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