Application Report

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Determining Minimum Acquisition Times for SAR ADCs When a Step Function is Applied to the Input

Miro Oljaca and Keith Sanborn — *Data Acquisition Products*

ABSTRACT

This application report analyzes a simple method for calculating minimum acquisition times for successive-approximation register analog-to-digital converters (SAR ADCs). The input structure of the ADC is examined along with the driving circuit. The voltage on the sampling capacitor is then determined for the case when a step function is applied to the input of the driving circuit. Three different test cases are subsequently evaluated using both precise and approximated equations.

Contents

List of Figures

1 Introduction

When it comes to designing the proper input driving circuit for analog-to-digital converters (ADCs), emphasis is generally placed on the calculation of the RC filter in front of the analog input and the selection of an operational amplifier (see Reference 1). The selection of the external RC components depends on the internal structure, sampling sequence, and charge injection of the successive approximation register (SAR) ADC (see Reference 2 through Reference 4). Knowledge of the internal ADC input structure, especially the value of the sampling capacitor, will assist users in optimizing the external RC components in order to obtain the maximum specified device performance (see Reference 5).

The calculation of the external RC filter is usually carried out with the assumption that the analog input sampling switch resistance is negligible (see Reference 5). In the following analysis, the analog input sampling switch resistance will be included.

2 SAR ADC Analog Input Equivalent Circuit

A typical analog input driving circuit for the ADC includes an operational amplifier (op amp) as well as an input RC filter composed of R_{IN} and C_{IN} as shown in Figure 1. The signal is then fed through the sampling switch SW with an equivalent on-resistance R_{SW} to the sampling capacitor C_{SH}. The input switch is composed of a CMOS transmission gate or similar structure. The equivalent on-resistance of the transistors is not linear and depends on the input signal level (see Reference 6). For this analysis, the average on-resistance of the switch measured in the linear region of operation will be used.

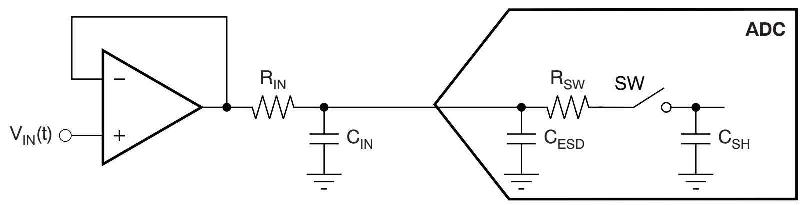

Figure 1. Typical SAR ADC Input Driving Circuit

Furthermore, the op amp is assumed to have ideal characteristics. As a result, it can be modeled as an ideal voltage source. By modeling the op amp in this way, the circuit from Figure 1 can be simplified as Figure 2 shows.

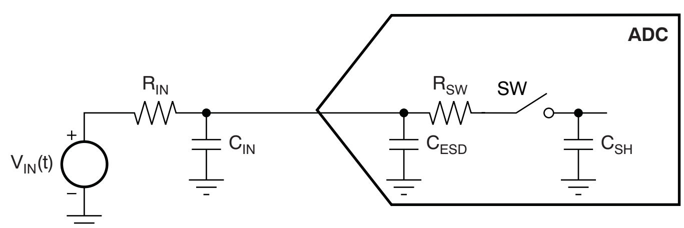

Figure 2. Simplified SAR ADC Input Driving Circuit

The ESD protection circuit at the input of the ADC has an equivalent capacitance C_{ESD}. This capacitance is the parallel combination of the protection circuit from the input pin to the power-supply rail and ground. The equivalent capacitance of C_{ESD} is in the range of 4 pF to 10 pF. On the other hand, the input filter capacitance C_{IN} is in the range of 1 nF to 10 nF. If $C_{IN} >> C_{ESD}$, then C_{ESD} can be ignored.

Besides treating the op amp in Figure 1 as ideal, this analysis investigates the case of the input signal to the converter changing state after the sampling switch SW has closed. This situation may occur if the input signal suddenly changes during the acquisition period for a SAR ADC with a single input channel. SAR ADCs with an integrated multiplexer may also experience this situation when changing input channels. Under these conditions, the input signal can be represented as a unit step function with voltage V_{IN}. Furthermore, the circuit in Figure 2 can be represented as a second-order, low-pass filter. The circuit for this case with updated variables is shown in Figure 3.

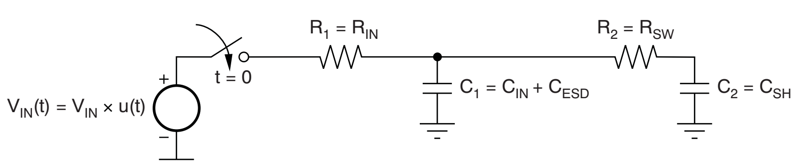

Figure 3. SAR ADC Input Driving Circuit Represented as a Second-Order, Low-Pass Filter

The worst case occurs when the input signal switches from zero or negative full-scale (NFS) to the input voltage V_{IN} or positive full-scale (PFS). In order to analyze the circuit in Figure 3 under worst-case conditions, the initial voltages on capacitors C_1 and C_2 are set to zero or NFS. Figure 4 shows the Laplace transform of the circuit in Figure 3 with the initial conditions, reference currents, and voltages that are used in the analysis.

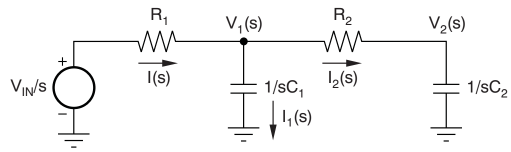

Figure 4. Second-Order Filter with Voltages and Currents Defined

The primary goal of this analysis is to determine the minimum acquisition time (t_{ACQ}) for the voltage on capacitor C_2 to settle within 1/2 LSB of the input signal for an *N*-bit SAR ADC as a function of R_1, C_1, R_2, and C_2. In order for this analysis to be performed, an expression for the voltage V_2 across capacitor C_2 as a function of time must be calculated. The next section in this application report focuses on this calculation.

3 Mathematical Analysis of the Equivalent Circuit

The Laplace transform of voltage V_2 in Figure 4 is:

$$V_2(s) = A(s) \times V_{IN} \tag{1}$$

where:

$$A(s) = \omega_n^2 \times \frac{1}{s} \times \frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

The calculations for Equation 1 and Equation 2 are shown in Appendix A. The inverse Laplace transform of Equation 2 is:

$$A(t) = \omega_n^2 \times \left[\frac{1}{\omega_n^2} + \frac{1-\zeta^2}{\omega_n^2(\zeta^2-1)} \times e^{-\zeta\omega_n t} \times \cos(\omega_n\sqrt{1-\zeta^2}\,t) + \frac{-\zeta}{\omega_n^2\sqrt{1-\zeta^2}} \times e^{-\zeta\omega_n t} \times \sin(\omega_n\sqrt{1-\zeta^2}\,t)\right] \tag{3}$$

After simplifying and applying Euler's formula, Equation 3 can be re-written as follows (see Appendix B for further details):

$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2-1}} \times \left[\left(\zeta + \sqrt{\zeta^2-1}\right) \times e^{-\omega_n(\zeta - \sqrt{\zeta^2-1})t} - \left(\zeta - \sqrt{\zeta^2-1}\right) \times e^{-\omega_n(\zeta + \sqrt{\zeta^2-1})t}\right] \tag{4}$$

Equation 4, in turn, can be expressed as:

$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2-1}} \times \left[(\zeta + \sqrt{\zeta^2-1}) \times e^{-\frac{t}{\tau_1}} - (\zeta - \sqrt{\zeta^2-1}) \times e^{-\frac{t}{\tau_2}}\right] \tag{5}$$

where time constants τ_1 and τ_2 are defined as Equation 6 and Equation 7, respectively:

$$\tau_1 = \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2-1})} \tag{6}$$

$$\tau_2 = \frac{1}{\omega_n(\zeta + \sqrt{\zeta^2-1})} \tag{7}$$

In order to observe the effects of these two time constants, Equation 5 can be rewritten as:

$$A(t) = 1 - \left[k1(t) - k2(t)\right] \quad (8)$$

where:

$$k1(t) = \frac{\zeta + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \quad (9)$$

and

$$k2(t) = \frac{\zeta - \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_2}} \quad (10)$$

The plots of Equation 8, Equation 9, and Equation 10 as a function of time are shown in Figure 5.

The following values were used in Figure 5: R_1 = 100 Ω, R_2 = 800 Ω, C_1 = 1000 pF, and C_2 = 40 pF.

These component values set **a** = 100 ns, **b** = 4 ns, and **c** = 32 ns. These values, in turn, establish ω_n = 17.678 Mrad/s and ζ = 1.202. Furthermore, the time constants are calculated to be τ_1 = 105.721 ns and τ_2 = 30.267 ns.

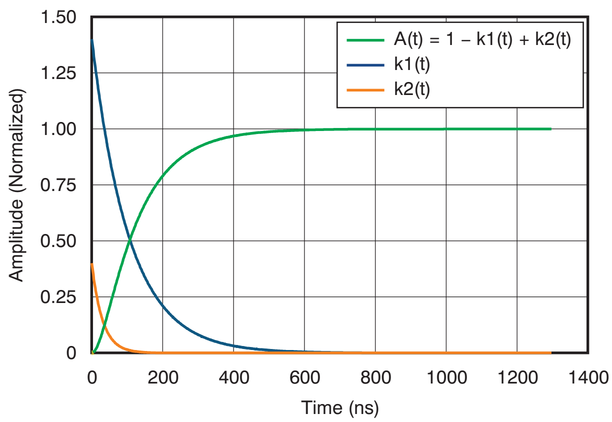

Figure 5. Plots of Equations (8), (9), and (10) versus Time

As shown in Figure 5, k2(t) is going to decay faster than k1(t) when $\tau_2 << \tau_1$. In fact, Equation 6 and Equation 7 show that τ_1 will always be greater than τ_2. Under these conditions, Equation 8 can be approximated as a function with only time constant τ_1, or:

$$A(t) \approx 1 - \frac{\zeta + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \quad (11)$$

4 Minimum Acquisition Time

In order for the voltage on capacitor C_2 in Figure 3 to settle within 1/2 LSB of the input signal for an *N*-bit SAR ADC:

$$A(t) \geq 1 - \frac{1}{2^{N+1}} \quad (12)$$

If k1(t) >> k2(t) at the minimum acquisition time, then A(t) in Equation 12 may be approximated by Equation 11. When this approximation is done, the minimum acquisition time t_{ACQ} for an *N*-bit ADC is (see Appendix C for calculations):

$$t_{ACQ} \geq \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \left[N \times \ln(2) + \ln\left(\frac{\zeta + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \quad (13)$$

5 Test Cases

In order to evaluate if the approximation derived in Equation 11 is valid, the following test cases were analyzed for a 16-bit ADC (*N* = 16):

(a) $R_1C_1 = R_2C_2 \times 100$

(b) $R_1C_1 = R_2C_2$

(c) $R_1C_1 = R_2C_2 / 100$

The results of these cases are displayed in Table 1.

Table 1. Results of Three Test Cases

Parameter	Case (a)	Case (b)	Case (c)	Units
R_1	100	100	10	Ω
C_1	1000	1000	1000	pF
R_2	20	2000	2000	Ω
C_2	50	50	50	pF
$f_1 = \frac{1}{2\pi R_1 C_1}$	1.59	1.59	159	MHz
$f_2 = \frac{1}{2\pi R_2 C_2}$	159	1.59	1.59	MHz
f_2/f_1	100	1	0.01	
a[(1)]	100	100	1	ns
b[(1)]	5	5	0.5	ns
c[(1)]	1	100	100	ns
ω_n[(1)]	100	10	100	Mrad/s
ζ[(1)]	5.300	1.025	5.075	
τ_1	105.048	125.000	100.505	ns
τ_2	0.952	80.000	0.995	ns
t_{ACQ}	1.239	1.601	1.185	µs

(1) Refer to Appendix A for equations.

By using the acquisition times from Table 1, the final voltage on the sampling capacitor of the ADC from Figure 1 was calculated for each test case by using Equation 11 and Equation 8. The difference in the final voltage calculated with Equation 11 and Equation 8 for each test case is negligible. This investigation clearly shows that using the simplified Equation 11 to calculate the final voltage on the sampling capacitor does not introduce any significant error compared to using the exact formula (Equation 8). This result is further supported by the plots in Figure 6 through Figure 8.

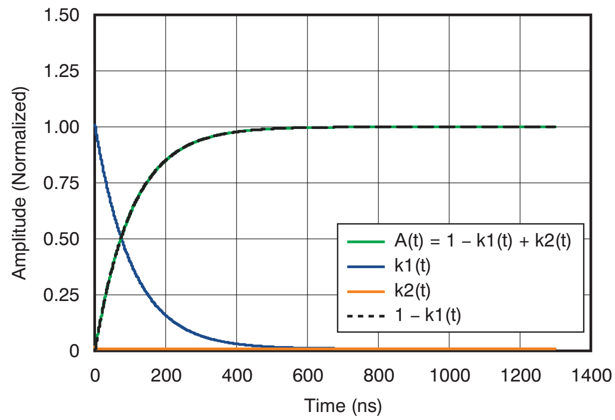

Figure 6. Case (a)

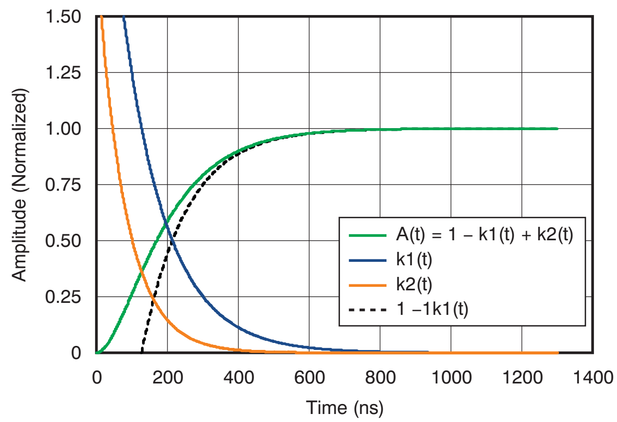

Figure 7. Case (b)

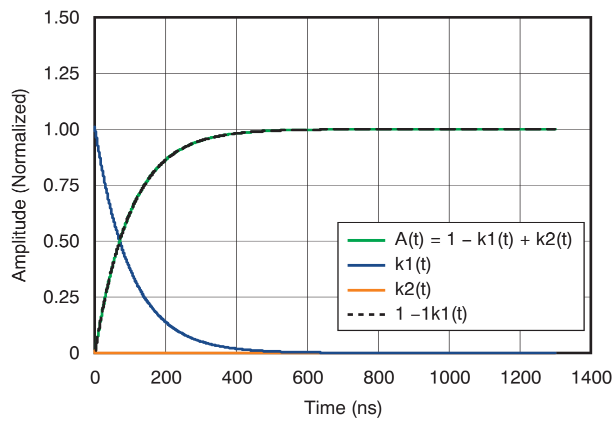

Figure 8. Case (c)

6 Conclusion

This application report provides a simple analytical method for calculating minimum acquisition times for SAR ADCs. The input structure of the ADC is analyzed together with the driving circuit. The voltage on the sampling capacitor is then determined for the case when a step function occurs on the input of the driving circuit. Three different test cases were calculated using exact equations as well as simplified ones. The difference in the final acquired voltage calculated with these two equations was negligible.

7 References

The following documents are available for download through the indicated web sites.

1. Oljaca, M. and B. Baker. (2008). Start with the right op amp when driving SAR ADCs. EDN. October 16, 2008. Pp. 43-58.

   Download at: http://www.edn.com/article/CA6602451.html
2. Downs, R. and M. Oljaca. (2005). Designing SAR ADC drive circuitry, Part I: A detailed look at SAR ADC operation. Analog Zone.

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   Download at: http://www.edn.com/article/CA6447231.html
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   Download at: http://www.analogzone.com/acqt1101.pdf

Appendix A

The voltage and currents in the circuit of Figure 4 can be described with the following equations:

$$V_1(s) = \frac{I_1(s)}{sC_1} \tag{14}$$

$$V_2(s) = \frac{I_2(s)}{sC_2} \tag{15}$$

$$V_1(s) - V_2(s) = R_2 I_2(s) \tag{16}$$

$$\frac{V_{IN}}{s} - V_1(s) = R_1 I(s) \tag{17}$$

$$I(s) = I_1(s) + I_2(s) \tag{18}$$

Equation 14, Equation 15, and Equation 17 can be rewritten as:

$$I_1(s) = sC_1 V_1(s) \tag{19}$$

$$I_2(s) = sC_2 V_2(s) \tag{20}$$

$$I(s) = \frac{V_{IN}}{sR_1} - \frac{V_1(s)}{R_1} \tag{21}$$

Substituting Equation 19 through Equation 21 into Equation 18 yields:

$$V_{IN} = (s^2 R_1 C_1 + s) V_1(s) + s^2 R_1 C_2 V_2(s) \tag{22}$$

Using Equation 20 in Equation 16 produces:

$$V_1(s) = (sR_2C_2 + 1) V_2(s) \tag{23}$$

Substituting Equation 23 into Equation 22 produces:

$$V_{IN} = \left[(s^2 R_1 C_1 + s)(sR_2C_2 + 1) + s^2 R_1 C_2\right] \times V_2(s) \tag{24}$$

By using these constants:

$a = R_1C_1$

$b = R_1C_2$

$c = R_2C_2$

Equation 24 can be simplified to:

$$V_{IN} = s\left[(sa + 1)(sc + 1) + sb\right] \times V_2(s) \tag{25}$$

The voltage $V_2(s)$ can be described as a function of the input step signal V_{IN} by rearranging Equation 25 to yield:

$$V_2(s) = \frac{1}{ac} \times \frac{1}{s} \times \frac{1}{s^2 + s\frac{a + b + c}{ac} + \frac{1}{ac}} \times V_{IN} \tag{26}$$

The coefficients in Equation 26 can be represented as:

$$\frac{a + b + c}{ac} = 2\zeta\omega_n \tag{27}$$

and

$$\frac{1}{ac} = \omega_n^2 \tag{28}$$

Substituting Equation 27 and Equation 28 into Equation 26 produces:

$$V_2(s) = A(s) \times V_{IN} \tag{29}$$

where:

$$A(s) = \omega_n^2 \times \frac{1}{s} \times \frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{30}$$

Appendix B

The equation:

$$A(t) = \omega_n^2 \times \left[\frac{1}{\omega_n^2} + \frac{1 - \zeta^2}{\omega_n^2(\zeta^2 - 1)} \times e^{-\zeta\omega_n t} \times \cos(\omega_n \sqrt{1 - \zeta^2}\, t) + \frac{-\zeta}{\omega_n^2 \sqrt{1 - \zeta^2}} \times e^{-\zeta\omega_n t} \times \sin(\omega_n \sqrt{1 - \zeta^2}\, t) \right] \quad (31)$$

Can be reduced to:

$$A(t) = 1 - e^{-\zeta\omega_n t} \times \left[\cos(\omega_n \sqrt{1 - \zeta^2}\, t) + \frac{\zeta}{\sqrt{1 - \zeta^2}} \times \sin(\omega_n \sqrt{1 - \zeta^2}\, t) \right] \quad (32)$$

The arguments of the cosine and sine terms in Equation 32 can be defined as:

$$x = \omega_n \sqrt{1 - \zeta^2}\, t \quad (33)$$

Since:

$$\sqrt{1 - \zeta^2} = i\sqrt{\zeta^2 - 1} \quad (34)$$

Equation 33 can be re-arranged to be:

$$x = iy \quad (35)$$

where:

$$y = \omega_n \sqrt{\zeta^2 - 1}\, t \quad (36)$$

Euler's formula can be used to represent the cosine and sine terms in Equation 32 as:

$$\cos(iy) = \frac{e^{-y} + e^{y}}{2} \quad (37)$$

and

$$\sin(iy) = \frac{e^{-y} - e^{y}}{2i} \quad (38)$$

Substituting Equation 35 and Equation 36 into Equation 37 and Equation 38 yields:

$$\cos(\omega_n \sqrt{1-\zeta^2}\,t) = \frac{e^{-\omega_n\sqrt{\zeta^2-1}t} + e^{\omega_n\sqrt{\zeta^2-1}t}}{2} \tag{39}$$

and

$$\sin(\omega_n \sqrt{1-\zeta^2}\,t) = \frac{e^{-\omega_n\sqrt{\zeta^2-1}t} - e^{\omega_n\sqrt{\zeta^2-1}t}}{2i} \tag{40}$$

Using Equation 39 and Equation 40 in Equation 32 produces:

$$A(t) = 1 - e^{-\zeta\omega_n t} \times \left(\frac{e^{-\omega_n\sqrt{\zeta^2-1}t} + e^{\omega_n\sqrt{\zeta^2-1}t}}{2} + \frac{\zeta}{\sqrt{1-\zeta^2}} \times \frac{e^{-\omega_n\sqrt{\zeta^2-1}t} - e^{\omega_n\sqrt{\zeta^2-1}t}}{2i} \right) \tag{41}$$

Substituting Equation 34 for the square-root portion in the denominator of right-hand term in Equation 41 yields:

$$A(t) = 1 - e^{-\zeta\omega_n t} \times \left(\frac{e^{-\omega_n\sqrt{\zeta^2-1}t} + e^{\omega_n\sqrt{\zeta^2-1}t}}{2} + \frac{\zeta}{i\sqrt{\zeta^2-1}} \times \frac{e^{-\omega_n\sqrt{\zeta^2-1}t} - e^{\omega_n\sqrt{\zeta^2-1}t}}{2i} \right) \tag{42}$$

By re-arranging the terms, Equation 42 can be simplified to:

$$A(t) = 1 - \frac{1}{2\sqrt{\zeta^2-1}} \times \left[\left(\zeta + \sqrt{\zeta^2-1}\right) \times e^{-\omega_n(\zeta - \sqrt{\zeta^2-1})t} - \left(\zeta - \sqrt{\zeta^2-1}\right) \times e^{-\omega_n(\zeta + \sqrt{\zeta^2-1})t} \right] \tag{43}$$

Appendix C

For k1(t) >> k2(t), Equation 5 reduces to:

$$A(t) \approx 1 - \frac{\zeta + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t}{\tau_1}} \tag{44}$$

In order for Equation 44 to satisfy the criteria in Equation 12 for the minimum acquisition time t_{ACQ}:

$$\frac{1}{2^{N+1}} \geq \frac{\zeta + \sqrt{\zeta^2 - 1}}{2\sqrt{\zeta^2 - 1}} \times e^{-\frac{t_{ACQ}}{\tau_1}} \tag{45}$$

Re-arranging the terms in Equation 45 and solving for t_{ACQ} yields:

$$t_{ACQ} \geq \tau_1 \times \left[N \times \ln(2) + \ln\left(\frac{\zeta + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{46}$$

Using Equation 6 to replace τ_1 in Equation 46 produces the inequality:

$$t_{ACQ} \geq \frac{1}{\omega_n(\zeta - \sqrt{\zeta^2 - 1})} \times \left[N \times \ln(2) + \ln\left(\frac{\zeta + \sqrt{\zeta^2 - 1}}{\sqrt{\zeta^2 - 1}} \right) \right] \tag{47}$$

Revision History

Changes from Original (November, 2009) to A Revision	Page
• Corrected equations for test cases 1 and 3	5
• Corrected typos in Table 1; changed units for f_1 and f_2 to MHz from kHz	5

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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