*Application Note*

# *Improving MSPS ADC's SFDR While Relaxing AAF Requirements and Using Integrated DDC Features*

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**ABSTRACT**

Achieving the best dynamic range in terms of spurious free dynamic range (SFDR) with high-speed MSPS converters are explored.

Anti-aliasing filter (AAF) techniques are covered at both lower and higher converter sampling rates and what this means to the filter design requirements.

Tradeoffs are given when using an external AAF in front of the ADC in combination with digital features included in most MSPS converters on the market today.

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## Trademarks

# 1 Introduction

With the advent of high-speed MSPS ADCs now climbing onto smaller process geometries, manufacturers are achieving 65nm and lower. This allows for inherent digital features such as the DDC, digital down converter, more commonly seen in GSPS ADCs IC designs, to be employed in the lower sampling rate brethren. This application note reveals how spurious performance can be improved significantly in your next MSPS converter signal chain design. Anti-aliasing filter requirements commonly used in many signal chain applications versus the true power of the inherent digital features, such as the DDC can also be explored. Using either, or a combination of both, techniques radically improves spurious free dynamic range in the next generation of MSPS converters on the market.

# 2 AAF Tradeoffs at Low Frequency and Low Sampling Rate

How to create more dynamic range (DR) in your system application is simple, just eliminate those pesky spurs in the noise floor. Usually, the HD2 and HD3, that is the second and third harmonic distortion, respectfully, are what typically define the DR limit for the converter. Removing spurious sounds simple on paper, but this concept can lead to other constraints that make this difficult to employ in the real *analog* world.

We know that having a spurious free dynamic range (SFDR) of -75dB or so is relatively achievable in today's modern MSPS converter technology without much effort. See Figure 2-1. Assuming clean power, clocking and input signals are provided, the example below, shows the ADC3664 sampling at 125MSPS in the second Nyquist zone with an analog input of approximately 70MHz. For more on sampling in the second Nyquist zone or sub-sampling ADC techniques please refer to *Precision labs series: Analog-to-digital converters (ADCs)* and *Ansys Nuhertz FilterSolutions*.

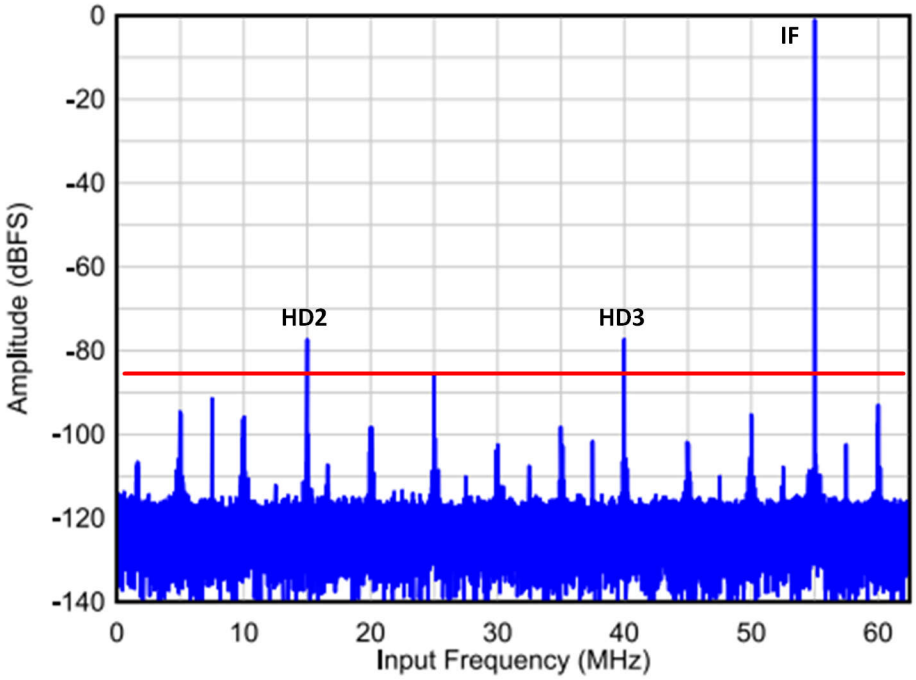


**Figure 2-1. Example of the ADC3664, 14bit, 125MSPS with 70MHz Analog Input Signal Applied**

However, if more DR is required for your application, say -85dB or more of SFDR. Then we typically have one of two options to tradeoff in the analog domain. Create a narrow band anti-aliasing filter, or AAF, around the center frequency of interest. Or go for a higher sampling rate ADC, you still need the AAF, but this relaxes the AAF constraints by a fair amount. Let's explore these concepts deeper.

Say you want to filter the 94MHz IF tone in the second Nyquist zone with 125MSPS ADC. This means you need to design a filter with sufficient rolloff to decrease down the -85dB+ SFDR dynamic range requirement in less than a 62.5MHz (+/-31.25MHz) passband or Nyquist zone. See Figure 2-2. This significantly ups the order of

the AAF design, the number of the components and variance in component tolerance also increases therefore, creating a filter that is difficult to make realizable and repeatable.

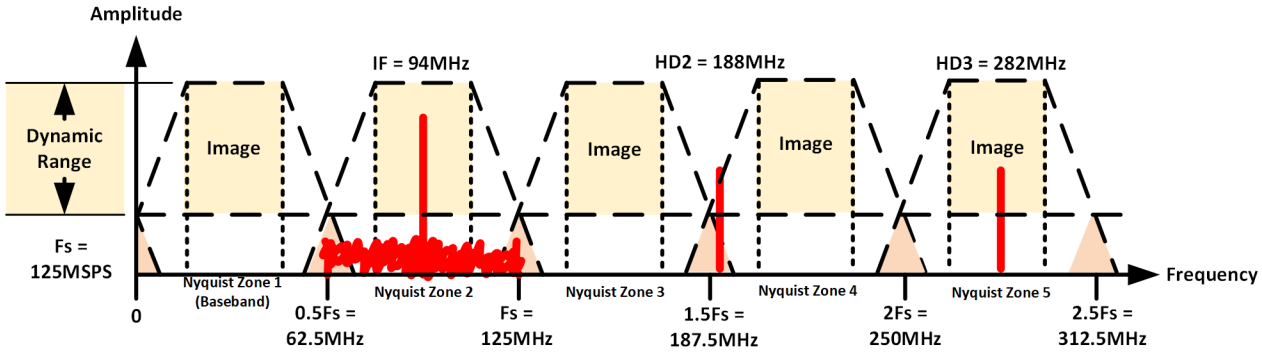


**Figure 2-2. 125MSPS AAF/DR Example**

To prove the point, using a simple filter modeling tool, see *How anti-aliasing filter design techniques improve active RF converter front ends*, we need to design and create at least a 9th order filter even to start to get close to that -85dB SFDR requirement. See Figure 2-3 for the simulated frequency response plot of the filter design. This is a 9th order Butterworth topology, centered at 94MHz, with 10MHz (or ±5MHz) of passband.

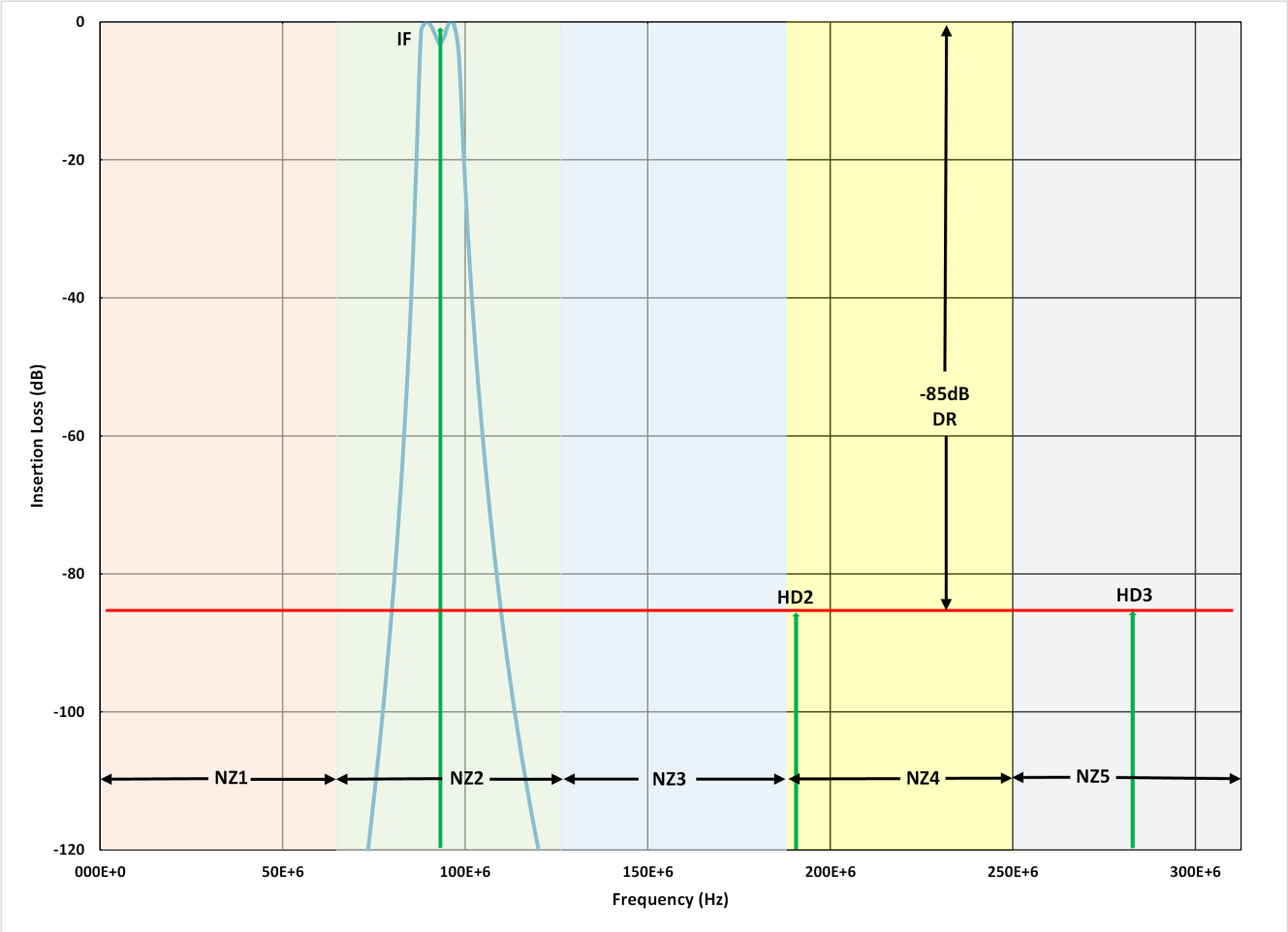


**Figure 2-3. Simulated Response of 9th Order, 94MHz Butterworth Filter Topology With 10MHz Passband**

As discussed, the number of components can also increase with such a high order filter. In this case, 28 components can need to be configured as per Figure 2-4. Keep in mind, this is just for the filter, this does not

include any resistive elements that can also likely need to be added, depending on the ADC's common mode voltage needs, any back terminations or other data sheet recommendations. Filters of this size also take up a significant amount of real estate on the printed circuit board, or PCB, using at least a 1085 mil x 200 mil total space for this specific example. See Figure 2-5.

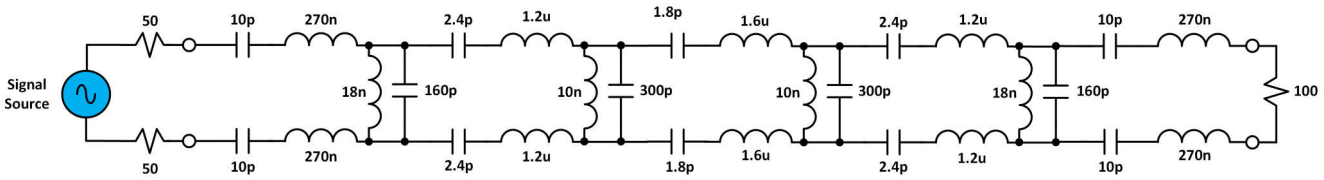


**Figure 2-4. 9th Order Simulated Filter, Synthesized**

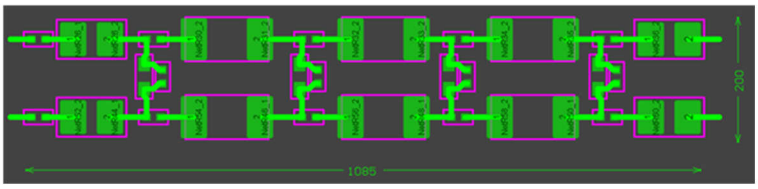


**Figure 2-5. 9th Order Simulated Filter, PCB/Layout Mockup**

One other note worth mentioning, low frequency filters typically run up against the Physics limit in terms of their size. Therefore, components sizes in the nH and uH region typically run much larger to accommodate lower frequencies and are typically available in 0805 package sizes or larger. This is another reason why so much area needs to be dedicated to this type of high order, low frequency AAF design.

Lastly, to be fair, the AAF design shown in Figure 2-5 is differential, which is a commonly used in implementations between an amplifier and ADC interface. If using a single-ended AAF approach and a balun to interface with the ADC's analog inputs, this can half the number of AAF components required, as shown above. However, the size of the balun and extra ADC components to finish off this type of interface can vary. For a deep dive on AAF design, please see *How anti-aliasing filter design techniques improve active RF converter front ends*

# 3 AAF Tradeoffs at Low Frequency and Higher Sampling Rate

Now let us turn this around and use a higher sampling rate, for example, a 500MSPS ADC, to help relax the AAF challenge as previously discussed. What we gain here is a wider Nyquist zone, which therefore, co-locates those pesky harmonic signals, HD2/HD3 within the same Nyquist zone. They are effectively not farther away, but now they cannot be aliased back within the band of interest due to their co-location. This simply allows for relaxation of the AAF design from a 9th order to a 4th order filter as shown in Figure 3-1.

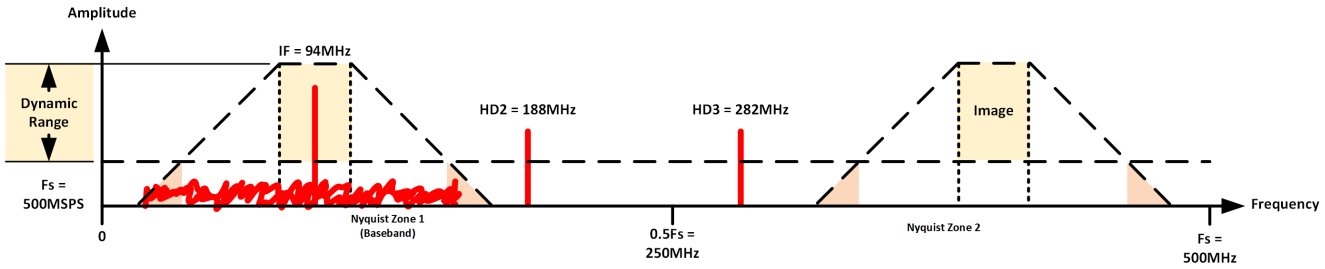


**Figure 3-1. 500MSPS AAF and DR Example**

Using a simple filter modeling tool again, we now only need to design and create a 4th order filter to get close to that -85dB SFDR requirement. See Figure 3-2 for the simulated frequency response plot of the filter design. This is a 4th order Butterworth topology, centered at 94MHz, with 10MHz (or +/-5MHz) of passband.

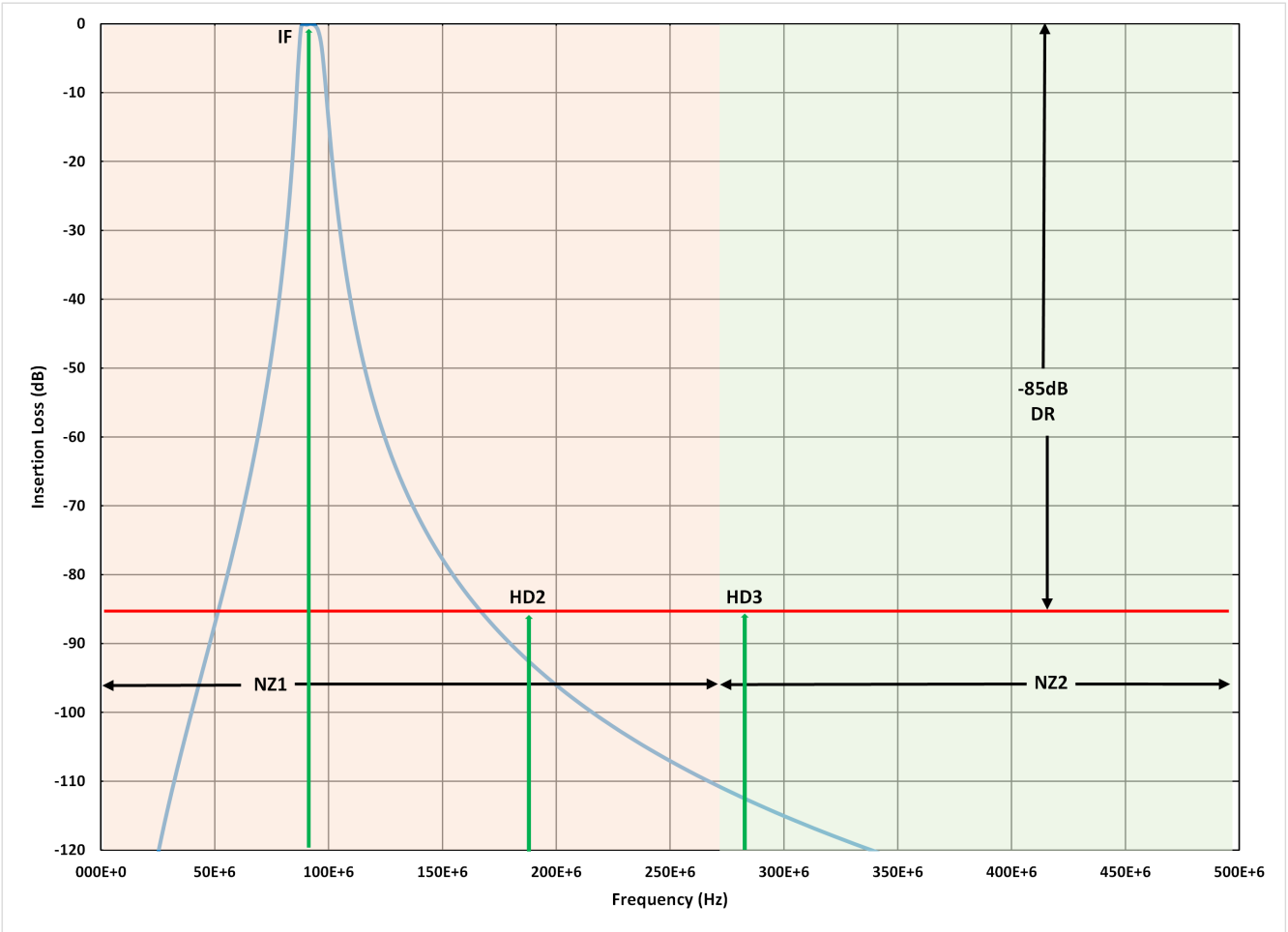


**Figure 3-2. Simulated Response of 4th Order, 94MHz Butterworth Filter Topology With 10MHz Passband**

As the number of components decrease, the filter design becomes more realizable and repeatable as there are less components tolerances deviating against each other with respect to their differential counterpart, see Figure 3-3. Now there are less than half the number of components is required now to do the job, and sufficiently reject the HD2/HD3 harmonics. This smaller filter design now uses a total footprint of 530 mil x 200 mils, which is again, roughly half the size as the equivalent differential filter design, see Figure 3-4.

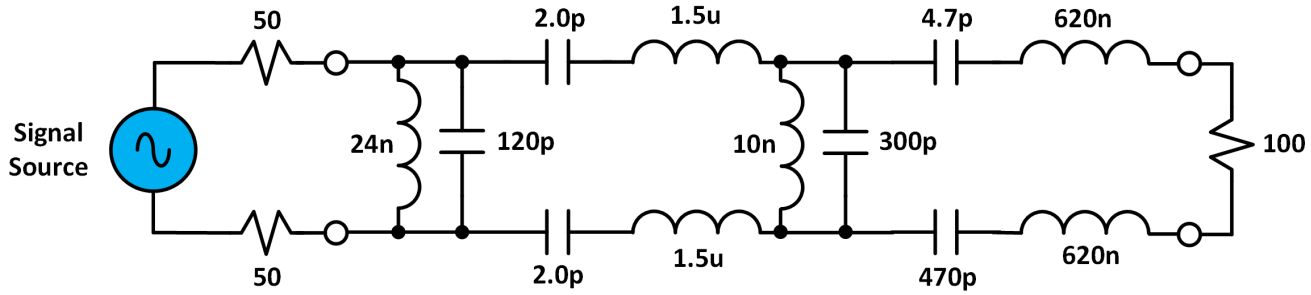


**Figure 3-3. 4th Order Simulated Filter, Synthesized**

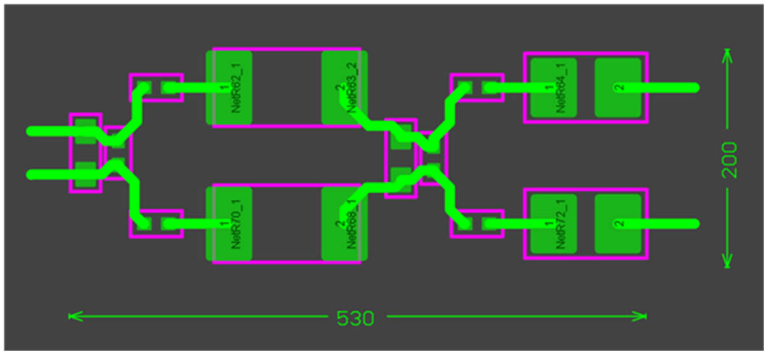


**Figure 3-4. 4th Order Simulated Filter, PCB or Layout Mockup**

Again, as mentioned previously, Figure 3-4 shows a differential filter approach, which is a commonly used implementation between an amplifier and ADC interface. If using a single-ended AAF approach, this can half reduces the number of components needed for the AAF design and balun interface to the ADC.

# 4 The Power of the ADC's Integrated DDC

With smaller IC process geometries more readily available, it is now possible to design ADCs that are both high-speed (MSPS) and rich in digital features, similar to the GSPS converters currently on the market. The digital down converter (DDC) is integral to these added digital features, allowing users to improve the digital backend processing in numerous ways. With proper frequency planning, see *FREQ-DDC-FILTER-CALC RF-Sampling Frequency Planner, Analog Filter, and DDC Excel™ Calculator*, the user can sample the signal, employ the integrated DDC within the ADC, and move only a portion of the bandwidth of interest digitally with little to no analog filtering.

For example, using the ADC3669, 16bit, 500MSPS ADC, we can configure the ADC to sample only a portion of the band, as outlined in Figure 4-1, so that HD2 and HD3 harmonics fall out of band. This first example shows an undecimated signal, when the ADC is in *DDC Bypass* mode. Ignoring the highlighted region, you can see the undesired harmonics are in band, and are negatively affecting the ADC's dynamic range performance.

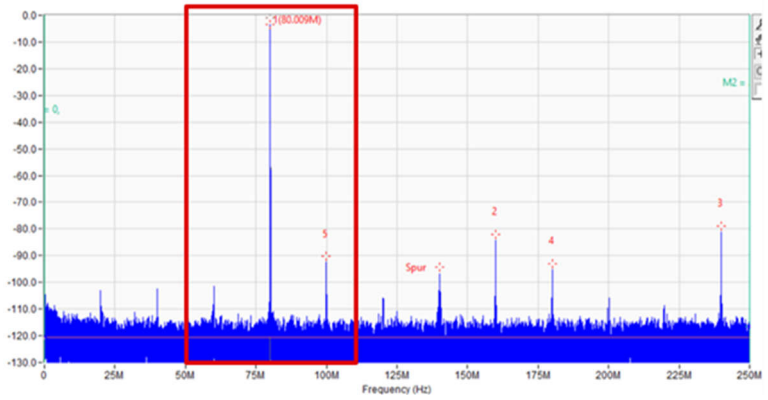


**Figure 4-1. ADC3669, 500MSPS ADC in Full DDC Bypass Mode**

Next is an example of an FFT capture using the same ADC3669 device in Real Decimation mode, with a complex decimation factor of 8. As seen, the undesired harmonic spurs now fall out of band, and are effectively filtered out in the digital domain. This improves our performance in two dimensions; a +6dB improvement in SNR, this is due to the processing gain in Equation 1 or in Equation 2.

$$10 \times \log_{10}\left(\frac{Fs}{2 \times BW}\right) \quad (1)$$

$$SNR \quad = 6.02 \times N + 1.76dB + 10 \times \log_{10}\left(\frac{Fs}{2 \times BW}\right) \quad (2)$$

Where: N = Number of ADC bits

Fs = ADC sampling frequency

BW = bandwidth of interest within the Nyquist zone

As well as removing the undesired harmonic spurs (HD2/HD3) to fall out of band, yielding an SFDR of -85dB or better. Thank you DDC! Check out Figure 4-2 and *Addressing High Data-Throughput Challenges, Chase Wood, Embedded Computing Design*, Unlocking RF Potential with Down converters, Chase Wood, Embedded Computing Design , and *Analyzing High-Bandwidth Spectrum Clusters, Chase Wood, Embedded Computing Design* for a deep dive on decimation basics and tradeoffs.

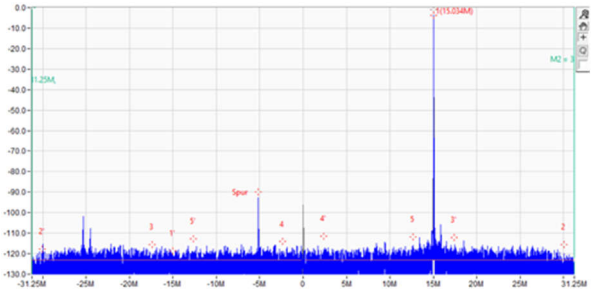

**Figure 4-2. ADC3669, 500MSPS With Complex Decimation-by-8 Enabled**

## 5 Summary

In summary, increasing the sampling rate of the ADC and/or using an ADC with digital processing features play an important role in increasing the overall system DR performance. To be upfront, there can be a downside with a slight increase in the ADC's power consumption when the DDC is employed. This is due to the higher sampling rate ADC and use of the extra digital features within the ADC. However, this can be a wash in terms of power if your application is still using an older generation ADC.

The analog tradeoffs involved in AAF design and the advantages of using DDC features to address dynamic range limitations have also been revealed. Keep in mind, these tradeoffs help to attack pesky HD2 and HD3 harmonics, but sometimes are not as effective on IMD3 spurious when using multi-tone signals, so further filtering can be required in certain applications.

Either way, the use of one or a combination of both techniques help to facilitate a healthier dynamic range for your next high-speed signal chain application, whether you're using the latest MSPS or GSPS ADCs available on the market.

## 6 References

1. Texas Instruments, *Precision labs series: Analog-to-digital converters (ADCs)*
2. *Ansys Nuhertz FilterSolutions*
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4. *Addressing High Data-Throughput Challenges, Chase Wood, Embedded Computing Design*
5. *Unlocking RF Potential with Down converters, Chase Wood, Embedded Computing Design*
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10. Texas Instruments, *ADC3668, ADC3669 Dual-Channel, 16-Bit 250MSPS and 500MSPS Analog-to-Digital Converter (ADC)* data sheet
11. Texas Instruments, *DATACONVERTERPRO-SW High-speed data converter pro software*
12. Texas Instruments, *FREQ-DDC-FILTER-CALC RF-Sampling Frequency Planner, Analog Filter, and DDC Excel™ Calculator*

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