Application Brief

Half-duplex Power Line Communication in TI's Programmable Logic Devices (TPLD)

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Introduction to Power Line Communication

Power line communication (PLC) is the practice of transmitting data over a power line. By combining the power line with a signal line, the total number of signal lines necessary can be reduced. This allows for several benefits to the designer. The reduction in signal lines reduces the total design size, while also potentially reducing the system BOM. It can also allow for a simpler interface with external systems

PLC is particularly attractive for designs which are extremely space constrained, such as wearable electronics. In these systems, PLC can be implemented on either internal or external lines. Internally, PLC can be used to transmit data from one area of the device to another without adding an additional trace or wire. Externally, PLC can be implemented on the charging line to simplify the charging contacts to only ground and VCC contacts, while still allowing for communication with a charging dock or controller. This reduces the complexity of the charging line and external contacts on the device and the charging peripheral, reducing the potential for wear and tear and hacking.

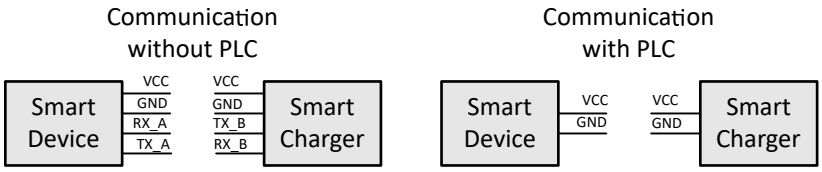

Figure 1. PLC Block Diagram

PLC does have limitations: interference from the power line can lead to signal degradation, and microcontrollers are not designed to interface with and modulate/demodulate signals to and from the PLC system. For effective PLC, ICs meant for PLC must be used.

TPLD for Half-Duplex PLC

All of the ICs in TI's Programmable Logic Device (TPLD) family can be programmed for effective PLC, using the internal logic and timing elements to modulate and demodulate PLC signals. This is a half-duplex design, meaning only one side can send data at a time. The TPLD does not have the capability to control or interpret the data that is sent, so any communication protocol across the PLC line must be implemented by the MCU. This design uses UART to communicate with an MCU on either side of the PLC.

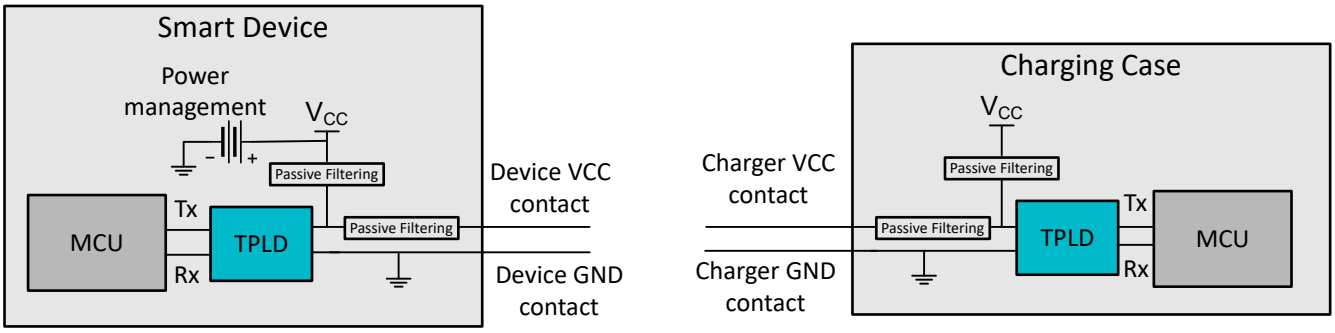

Figure 2. TPLD PLC Block Diagram

TPLD PLC Internal Diagram

Internally, the TPLD modulates the UART input with a high frequency signal and sends the result to the PLC output. The PLC input demodulates the high frequency signal from the PLC line and sends the result to the UART output.

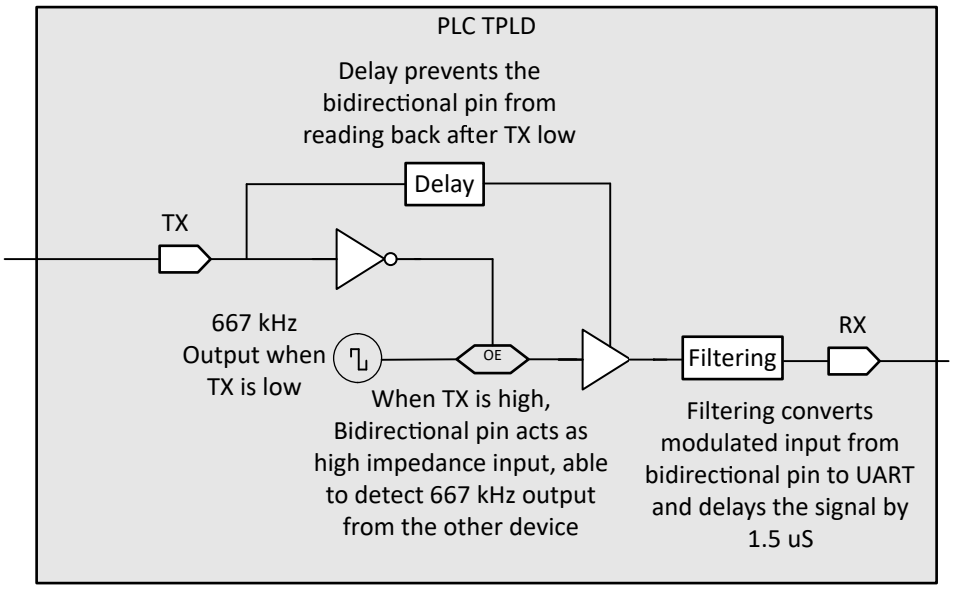

Figure 3. TPLD PLC Internal Block Diagram

This block diagram is implemented using the TPLD configuration shown below. This circuit diagram is from TI's InterConnect Studio, TPLD's programming GUI. Both TPLD in the system share the same configuration.

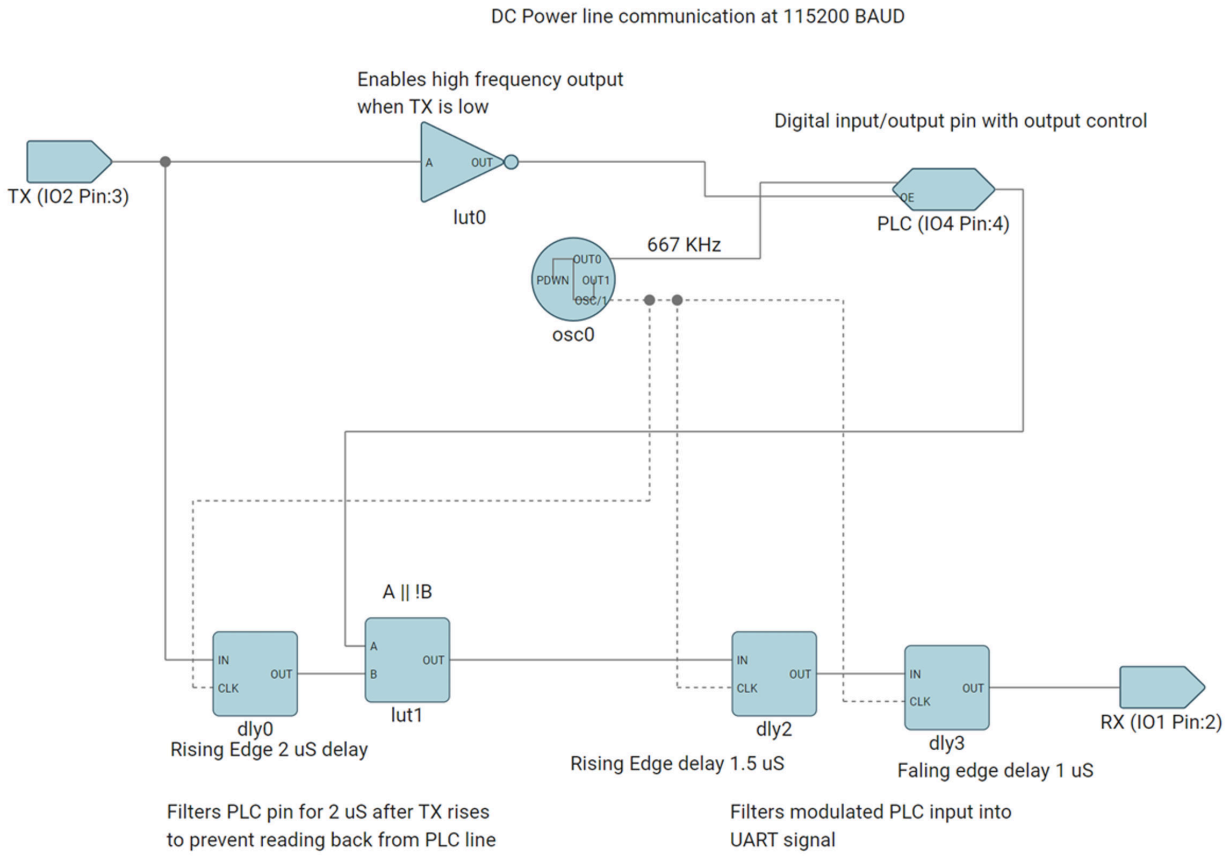

Figure 4. PLC Design in ICS

The Lut0 block enables the PLC as an output when the TX pin is low, causing the PLC pin to output the high frequency signal from Osc0.

The Dly0 and Lut1 blocks prevent the TPLD from reading back feedback from the pulses it produces as an output. The Dly2 block acts as filtering stage, recovering the high frequency modulated signal into the UART signal by extending any falling edge input into a 1.5uS negative pulse. The Dly3 block extends the positive side of the pulse, extending the positive edges slightly and recovering their original length.

TPLD PLC System Diagram

The PLC output from the first TPLD is shunted through the capacitor, creating high frequency noise on the PLC line, which is then shunted to the PLC input line of the second TPLD. Since the PLC input to the second TPLD is biased to a DC voltage of 2.5V, which is around the switching threshold of the TPLD. The second TPLD can detect the high frequency noise. The inductors isolate the communication line from the VCC rails, preventing the noise from being filtered out on the PLC line or from disrupting other components on the VCC rail.

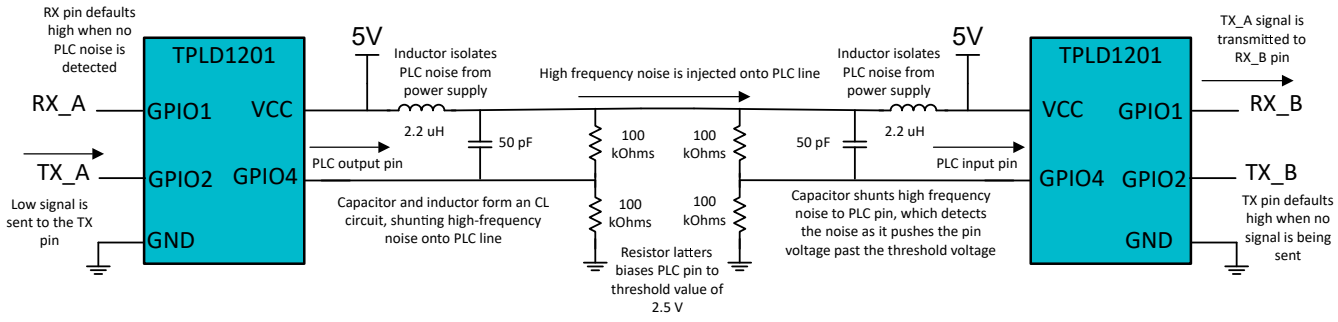

Figure 5. TPLD PLC System Diagram

The oscilloscope shot below shows the behavior of the transmitting TPLD and the signal on the DC line. The DC line is biased to 5V and the PLC line of the TPLDs is biased to 2.5V.

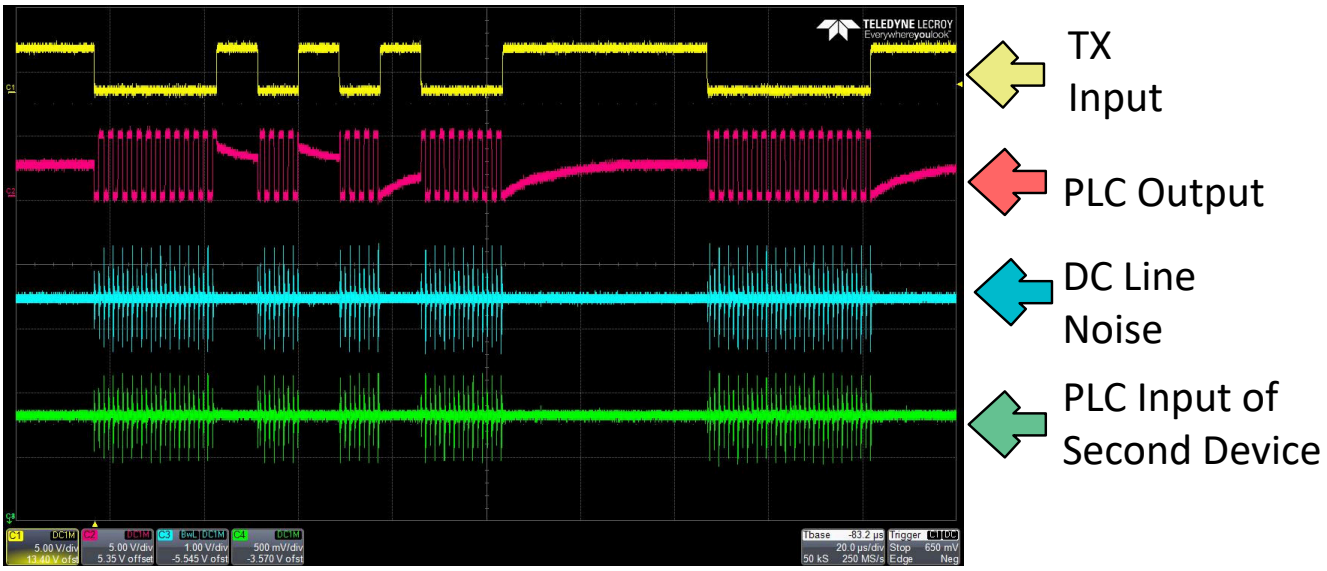

Figure 6. PLC TX Side Oscilloscope Pictures

The next oscilloscope shot shows the behavior of the receiving TPLD. The PLC input signal is converted to a digital data input by the TPLD, which the Dly2 block converts back to a UART stream by extending each negative pulse by 1.5uS. The Dly3 block truncates the negative pulses slightly, restoring the original data stream.

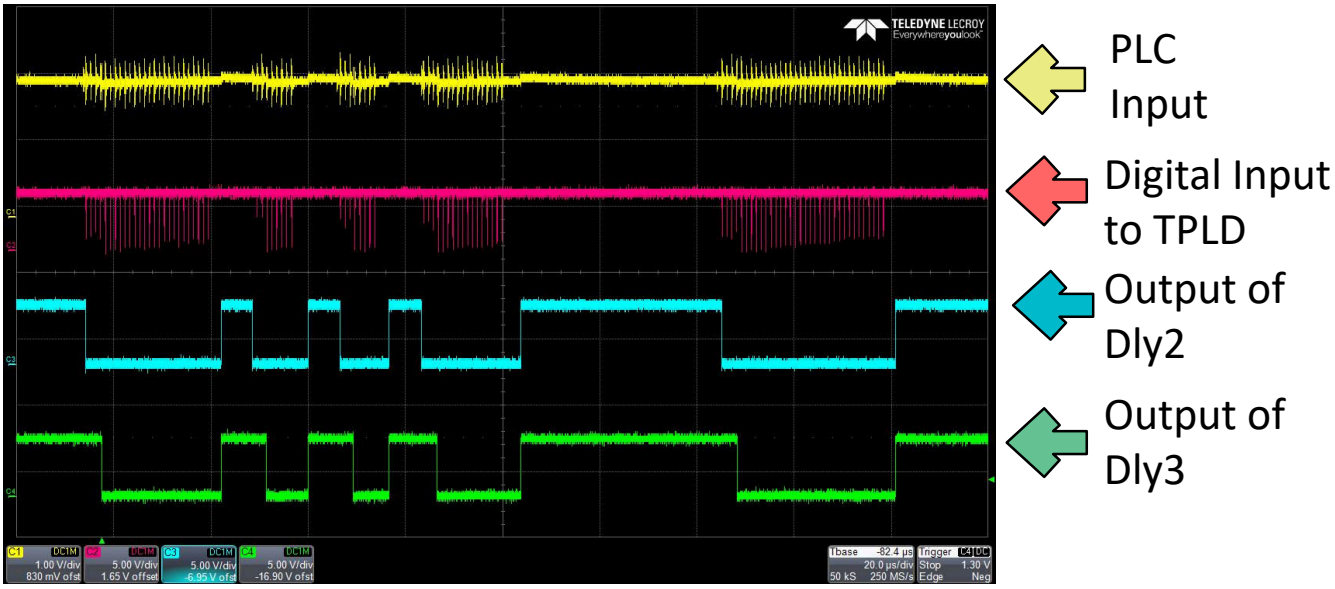

Figure 7. PLC RX Side Oscilloscope Pictures

Design Considerations

The values of the resistor divider pairs are selected to bias the PLC pins on the TPLD to the TPLD's switching threshold. This is typically ½ of the VCC of the TPLD. This also prevents the voltage oscillation on the pin from driving the pin's voltage negative. If necessary, the TPLD can operate from a different voltage level than the PLC line. The capacitor isolates the TPLD pin from the PLC power rail, so PLC can function as long as the TPLD is operating at a voltage level within the recommended operating conditions of the device and the PLC pin is biased to ½ of the VCC of the device.

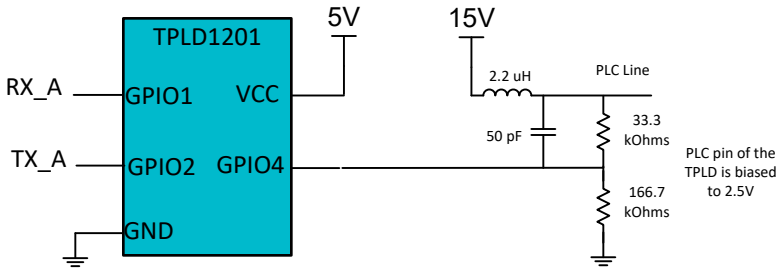

Figure 8. PLC with 15V Rail

The inductor and capacitor pairs are chosen to create noise on the PLC line at a frequency that is not filtered out by the inductors. Because this is determined by the system as a whole, the easiest way to determine the frequency of the noise produced by an LC combination is to simulate the system and produce a Fourier transform of the output. The system shown in Figure xxx has an expected noise frequency of around 21 MHz, as shown below. Performing a Bode analysis on the same system shows that frequencies of 21 MHz are not filtered out by the system. Thus, this LC combination works for this design.

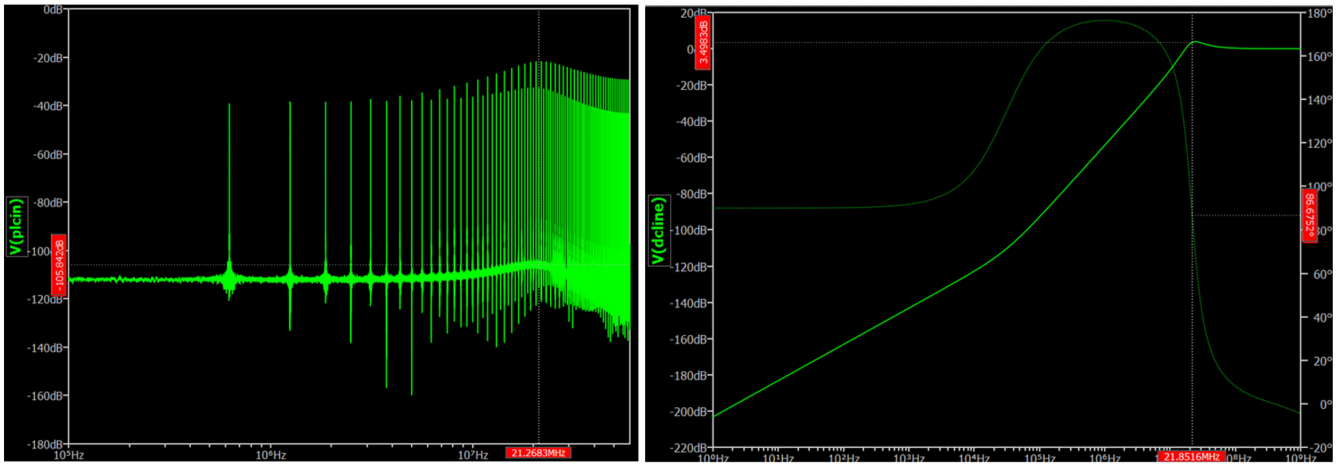

Figure 9. PLC FFT and Bode Plot

Advantages of PLC Using TPLD

TPLD1201 offers a small, inexpensive design for PLC, as shown in the table below. This is roughly half the cost of comparable dedicated PLC ICs.

Table 1. Solution Size and Cost Estimate

Device	Quantity per Side	Cost ($) (1ku)	Footprint	Area (mm2)
TPLD1201RWB	1	0.45	RWB	2.56
100nF Cap (Bypass)	1	0.02	402	0.5
2.2uH Ind	1	0.11	806	3.2
50pF Cap	1	0.0075	402	0.5
100 kOhm Res	2	0.0022	402	0.5
	Total cost (dollars/1ku):	0.5919	Total size:	7.76

When used for PLC, the TPLD1201 has several unused pins and logic blocks that can be configured to allow for other functions, such as button debouncing, smart button control, or reset and timing logic. This allows for more integration into the device, further reducing the total system BOM and design size.

Table 2. Remaining blocks in TPLD1201

Block	Number Remaining
IO pins	5
Counter/Delay	1
Lookup Table/Flip-Flop	4
Lookup table	3
Edge detect	1

An example of possible further integration is shown below. The timing and logic elements in the TPLD can be used to generate a timed, controlled reset pulse from a user-controlled button input. This integration can result in further space and cost savings and reduce the complexity of the system.

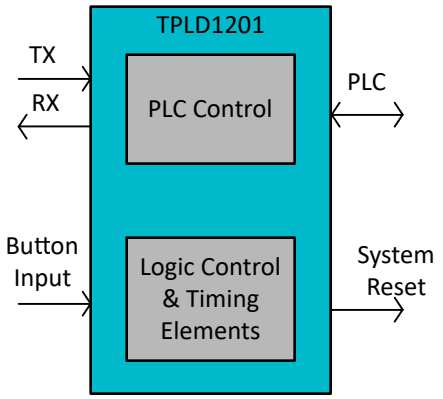

Figure 10. PLC and System Reset in Parallel

The TPLD design is modular, and there is room for customization of the design to better match system requirements.

For more information on TPLD, visit the TPLD product page or ask our engineers a question on the TI E2E™ Logic Support Forum. The programming GUI InterConnect Studio is available on the web at no cost to start building, simulating, and programming a TPLD configuration.

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