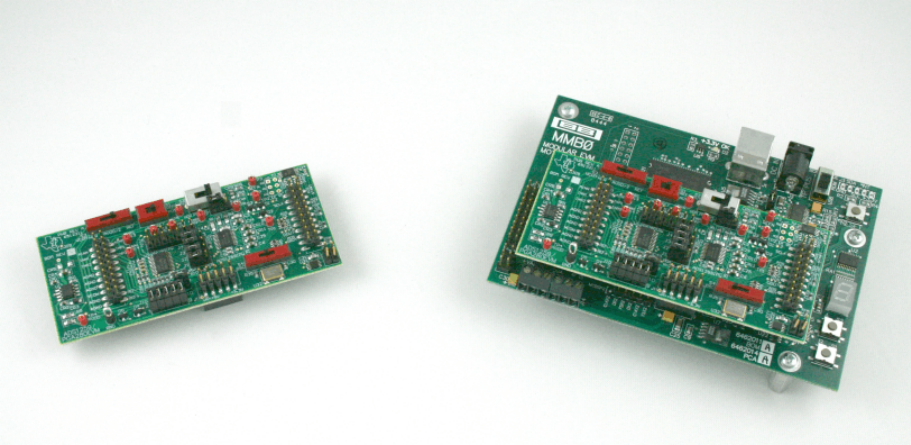
ADS1259EVM, ADS1259EVM-PDK



ADS1259EVM (Left) and ADS1259EVM-PDK (Right)

This user's guide describes the characteristics, operation, and use of the ADS1259EVM, both by itself and as part of the ADS1259EVM-PDK. This evaluation model (EVM) is an evaluation board for two different devices. First, it can be used to evaluate the ADS1259, a low-noise, 24-bit, single-channel, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1259 can be used either in standalone applications or with the PGA280. The PGA280 is a high-precision instrumentation amplifier with digitally-controllable gain and signal integrity test capability. The combination of these two devices forms a high-resolution measurement system able to digitize a wide range of signals.

This EVM allows performance evaluations of both the ADS1259 and the PGA280. The EVM also allows for PGA280 control of the ADS1259 through the use of the external chip select modes. Complete circuit descriptions, schematic diagrams, printed circuit board (PCB) layouts, and bill of material are included in this document.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Related Documents

Device	Literature Number
ADS1259	SBAS424A
PGA280	SBOS487A
REF5025	SBOS410C
SN74LVC2G157	SCES207K

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1 EVM Overview

1.1 Features

ADS1259EVM:

- Contains all support circuitry needed for the ADS1259
- PGA280 can be evaluated as a buffer and integrated control
- Voltage reference options: external or onboard
- Clock options: External clock source or 7.3728MHz onboard crystal oscillator
- Compatible with the TI Modular EVM System

ADS1259EVM and ADS1259EVM-PDK Features:

- Easy-to-use evaluation software for Microsoft® Windows®XP
- Data collection to text files
- Built-in analysis tools including scope, FFT, and histogram displays
- Complete control of board settings
- Easily expandable with new analysis plug-in tools from Texas Instruments

For use with a computer, the ADS1259EVM-PDK is available. This kit combines the ADS1259EVM board with the DSP-based MMB0 motherboard, and includes ADCPro™ software for evaluation.

The MMB0 motherboard allows the ADS1259EVM to be connected to the computer via an available USB port. This manual shows how to use the MMB0 as part of the ADS1259EVM-PDK, but does not provide technical details about the MMB0 itself.

ADCPro™ is a program for collecting, recording, and analyzing data from ADC evaluation boards. It is based on a number of plug-in programs, so it can be expanded easily with new test and data collection plug-ins. The ADS1259EVM-PDK is controlled by a plug-in running in ADCPro. For more information about ADCPro, see the *ADCPro™ Analog-to-Digital Converter Evaluation Software User's Guide* (SBAU128), available for download from the TI web site.

This manual covers the operation of both the ADS1259EVM and the ADS1259EVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1259EVM.

1.2 Introduction

The ADS1259EVM is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card.

The ADS1259EVM is available as a standalone printed circuit board (PCB) or as part of the ADS1259EVM-PDK, which includes an MMB0 motherboard and software. As a standalone PCB, the ADS1259EVM is useful for prototyping designs and firmware.

Note that the ADS1259EVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

2 Analog Interface

For maximum flexibility, the ADS1259EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D–VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J8. This header/socket provides access to the analog input pins of the ADS1259 and the PGA280. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

The input pins on the ADS1259EVM do not connect directly to the part, but connect to the inputs of the ADS1259 through switch S2 and modest filtering. Along with the analog header, these analog inputs can be easily accessed through test loops TP7 and TP8. Analog input pins INN1 and INP1 of the PGA280 can also be accessed through test loops TP13 and TP14 (INP2 and INN2 can only be accessed through the analog header). For all analog inputs, it is important that appropriate caution is taken when handling the pins.

Table 1 summarizes the pinouts for analog interface header J8.

Table 1. J8: Analog Interface Header Pinout

Pin Number	Signal	Description
J8.1	A0N	AINN, ADS1259, through switch S2 and low-pass filter, R1-2, C1-3
J8.2	A0P	AINP, ADS1259, through switch S2 and low-pass filter, R1-2, C1-3
J8.3	A1N	INN1, PGA280, through R7
J8.4	A1P	INP1, PGA280, through R6
J8.5	A1N	INN2, PGA280, through R5
J8.6	A1P	INP2, PGA280, through R4
J8.9-13 (odd)	AGND	Analog ground connections
J8.15	VCOM	VOCM, PGA280, via switch S3 and R3
J8.17-19 (odd)	AGND	Analog ground connections
J8.18	REFN	External reference source input (– side of differential input)
J8.20	REFP	External reference source input (+ side of differential input)
J8.10-16 (even)	Unused	—

The output pins of the PGA280 (VOP and VON) can be accessed through TP11 and TP12, but there is no connection to the analog interface J8. Figure 1 shows TP11 and TP12.

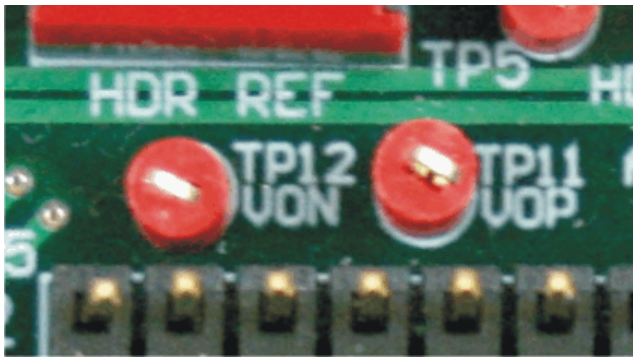


Figure 1. Test Points TP11 and TP12

The input of the ADS1259 is selectable through switch S2. From settings left-to-right, this three-way switch selects the ADC input from the AINP or AINN inputs from the analog interface header, the VOP and VON outputs of the PGA280, or allows for the self calibration inputs in combination with jumper J15.

As an indicator, the three settings of S2 are labeled HDR, PGA, and CAL below the switch, as Figure 2 illustrates.

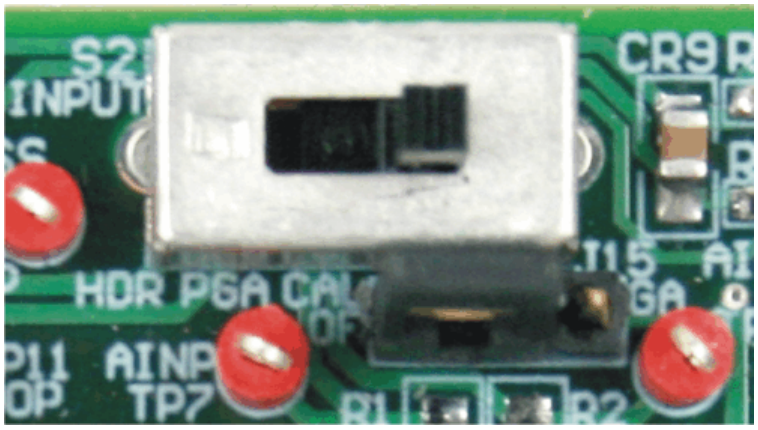


Figure 2. Switch S2 and Jumper J15

When switch S2 is set to the right, jumper J15 is used in the system calibration modes for the ADS1259. When the jumper is set to the left, pins 1 and 2 of jumper J15 are connected. The inputs of the ADS1259 are shorted together and tied to REFP. With this connection, the user can run an offset calibration. When the jumper is set to the right, pins 2 and 3 of jumper J15 are connected. The inputs of the ADS1259 are tied to REFP and REFN, measuring the reference voltage. At this point, the user can run a gain calibration. On either side of J15, OF and GA indicate the sides of jumper J15 used for offset and gain calibrations.

Another three-way switch (S3) sets the source of the output common-mode of the PGA280. Setting the switch to the left connects the output common-mode to pin J8.15 of the analog interface header. The center setting of the switch connects it to the midpoint between AVDD and AVSS via the voltage divider of R8 and R9. The right setting connects it to the REFOUT of the ADS1259. These options are labeled under the switch as HDR, AVDD/2, and REF respectively. Figure 3 shows S3 as it appears on the ADS1259EVM.

Figure 3. Switch S3

3 Digital Interface

The ADS1259EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D–VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row, header/socket combination at J7. This header/socket provides access to the digital control and serial data pins of the ADC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

All logic levels on J7 are 3.3V CMOS, except for the I²C™ pins. These pins conform to 3.3V I²C rules. Table 2 describes the J7 serial interface pins.

Table 2. J7: Serial Data Interface Pins

Pin No.	Pin Name	Signal Name	I/O Type	Pull-up	Function
J7.1	CNTL	Unused	—	—	—
J7.2	GPIO0	START	In	High	ADS1259 START Pin
J7.3	CLKX	SCLK	In	None	ADS1259/PGA280 SPI clock
J7.4	DGND	DGND	In/Out	None	Digital Ground
J7.5	CLKR	Unused	—	—	—
J7.6	GPIO1	$\overline{\text{RST}}$/PDWN	In	High	ADS1259 $\overline{\text{RST}}$/PDWN
J7.7	FSX	$\overline{\text{CS}}$	—	—	ADS1259 SPI Chip Select
J7.8	GPIO2	DOUT	Out	High	PGA280 SPI data out
J7.9	FSR	Unused	—	None	—
J7.10	DGND	DGND	In/Out	None	Digital Ground
J7.11	DX	DIN	In	None	ADS1259 SPI data in
J7.12	GPIO3	$\overline{\text{CS}}$	In	High	PGA280 SPI Chip Select
J7.13	DR	DOUT	Out	None	ADS1259 SPI data out
J7.14	GPIO4	Unused	—	None	—
J7.15	INT	$\overline{\text{DRDY}}$	Out	None	ADS1259 SPI Data Ready signal
J7.16	SCL	SCL	I²C	n/a	I²C clock
J7.17	TOUT	CLK	In	None	Can be used to provide a clock from a processor
J7.18	DGND	DGND	In/Out	None	Digital Ground
J7.19	GPIO5	EXTCLK	In	None	External Clock input
J7.20	SDA	SDA	I²C	n/a	I²C data

Many pins on J7 have weak pull-up/-down resistors. These resistors provide default settings for many of the control pins. Furthermore, many pins on J7 correspond directly to pins on the ADS1259. See the ADS1259 product data sheet for complete details on these pins.

4 Power Supplies

J11 is the power-supply input connector. Table 3 lists the configuration details for J11. The ADS1259 and PGA280 output amplifier are powered from +5V that can be supplied through the +5VA supply that can be found on pin J11.3. An additional bipolar supply is needed to power the PGA280 through +VA and –VA through pins J11.1 and J11.2.

Table 3. J11 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J11.1	+VA	+10V to +15V	Yes
J11.2	–VA	-10V to -15V	Yes
J11.3	+5VA	+5V analog supply	Always
J11.4	-5VA	-5V analog supply	No
J11.5	DGND	Digital ground input	Yes
J11.6	AGND	Analog ground input	Yes
J11.7	+1.8VD	1.8V digital supply	No
J11.8	VD1	Not used	No
J11.9	+3.3VD	3.3V digital supply	Always
J11.10	+5VD	+5V	No

Between the power-supply input connector of J11 and the devices on the EVM, jumper J10 allows a point to either bypass the supply connection or measure the supply current. With all the jumpers in J10 inserted, the components on the EVM are powered through the power-supply header. In this configuration, AVDD = +5V, DVDD = +3.3V, and AGND and DGND are both 0V (AGND and DGND are connected together on the EVM). Jumper J10 is shown in Figure 4.

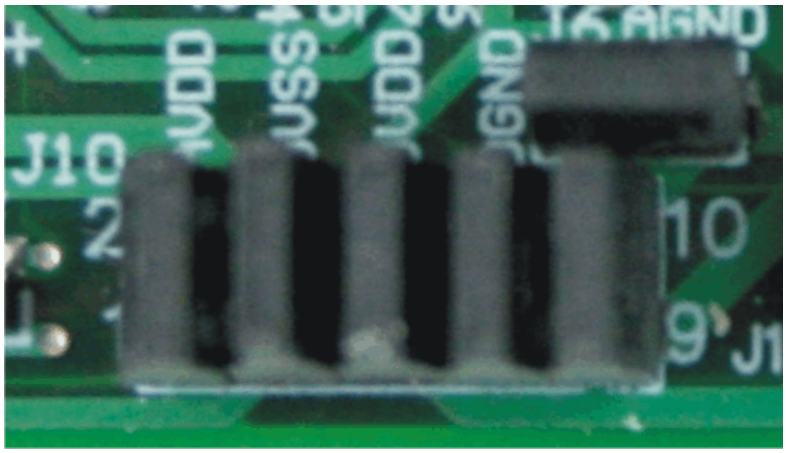


Figure 4. Jumper J10

Note that the high-voltage supplies for the PGA280 can only be accessed through pins 1 and 2 of jumper J11. The supplies +VA and –VA can be set to +10V to +15V, and –10V to –15V, respectively.

5 Voltage Reference

The ADS1259EVM has three options for supplying a reference voltage to the ADS1259. There are two options for an external reference and one option with the internal ADS1259 reference.

Switch S1 selects an external reference from an external reference voltage using pins J8.18 (REF–) and J8.20 (REF+) from the analog interface header or the REF5025 reference (U11). With the switch set to the left, switch S1 selects the external reference voltage that is connected to the header of J8. With the switch set to the right, S1 selects the onboard reference from the REF5025. Figure 5 shows switch S1 as it appears on the EVM.

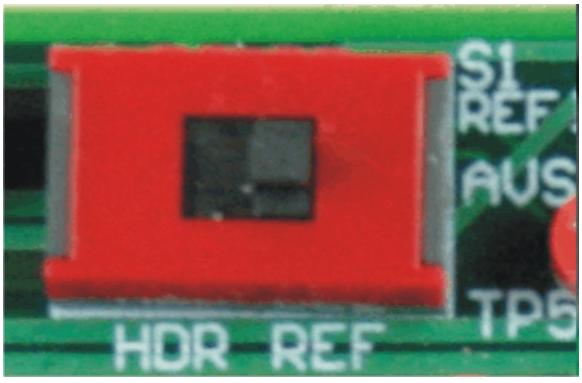


Figure 5. Switch S1

Alternately, the ADS1259 also has an internal reference that can be used. The REFOUT pin allows for measurement of this reference as well as a source that can be used to drive other functions, such as a measurement bridge or the output common mode of the PGA280. If the internal reference is selected, set switch S1 to the analog interface header, and leave the reference inputs at J8 unconnected.

6 ADS1259 Control

The ADS1259 can be used as a standalone device on the EVM or can be controlled using the interface with the PGA280. However, to use the ADS1259EVM-PDK with the ADCPro software, the PGA280 must be used as the control for the ADS1259.

To operate the ADS1259 without the PGA280, all the jumpers from J2, J3, and J4 should be moved to the right, connecting pins 2 and 3 of each jumper. These jumpers connect the ADS1259 to the EVM serial interface header and allow control of the ADS1259 $\overline{CS}$, START, and $\overline{RST}$/PDWN pins through J7.

Communications with the ADS1259 are handled with an SPI™-compatible serial interface. From the serial interface header, SCLK is handled with CLKX, chip select is handled by FSX, DIN comes from DX, DOUT goes to DR, and $\overline{DRDY}$ goes to INT. Additionally, the START pin (used to start a conversion) is run from GPIO0; reset and the power-down pin can be controlled by GPIO1.

The ADS1259 can also be controlled through communications from the PGA280. The PGA280 can generate an extended chip select ($\overline{ECS}$) for other devices that are connected to the same SPI wires: SDO, SDI, and SCLK. This ECS signal redirects the SPI communication to the connected device, while the PGA280 ignores data and SCLK. For this type of control, all the jumpers from J2, J3, and J4 should be moved to the left, connecting pins 1 and 2 of each jumper. This configuration connects the PGA280 to the ADS1259 though several of the PGA GPIOs. Note that this method of control is used in the ADS1259EVM-PDK, and that jumpers J2, J3, and J4 must be set to the left to enable control through ADCPro and the ADS1259EVM plug-in.

PGA280:GPIO0-2 can be used to control external functions, such as a mux.

PGA280:GPIO3 can be used to enable a reset or power-down of the ADS1259.

PGA280:GPIO4 can be used to toggle the START pin of the ADS1259 to trigger a conversion.

PGA280:GPIO5 is used to generate chip select ($\overline{ECS}$) for the ADS1259.

PGA280:GPIO6 receives the ACLKOUT signal from the ADS1259. This port sends out an $f_S/8$ clock from the ADS1259 that can be used as a synchronized chopper clock for the PGA280. Note that this configuration requires J1 to be set so that pins 2 and 3 are connected.

For more details, see the PGA280 data sheet.

7 Clock Source

The ADS1259 clock can come from one of several sources. It can be selected through switch S4, as illustrated in Figure 6.

Figure 6. Switch S4

- A crystal dropped into X1 with switch S4 set to the unconnected setting to the right.
- The ADS1259 can start an internal oscillator upon power up with switch S4 switched to ground to the center.
- The crystal oscillator (U32) can be selected through GPIO5 HIGH and switch S4 set to the left, selecting the multiplexer (U31) output.
- A TOUT clock coming from the serial header (J7.17) can be selected through GPIO5 LOW, with switch S4 selecting the multiplexer (U31)

7.1 Usage in PDK

If using the ADS1259EVM as part of the ADS1259EVM-PDK, switch S4 should be set to the left, using the multiplexer output. Using the onboard 7.3728MHz crystal oscillator allows the ADS1259EVM-PDK software to recognize the EVM using the software provided.

7.2 Usage as a standalone EVM

If using the EVM in your own system and not with the PDK hardware and software, switch S4 can be used to select the clock. The switch can be used to select the 7.3728MHz crystal (through multiplexer U31) or to allow the onboard oscillator to be enabled when S4 is set to ground.

8 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the ADS1259EVM.

8.1 Analog Input

A single-channel differential input source can be applied directly to J8 (top or bottom side) or through signal-conditioning modules available for the modular EVM system. The input is connected through switch S2 and through a low-pass filter (R1, R2, C10, C11, and C12) before reaching the ADS1259.

The common-mode voltage (VCOM) for the PGA280 input buffer is 2.5V supplied from the REFOUT of the ADS1259, the VCOM pin at the analog header (J8.15), or a voltage divider set to $AV_{DD}/2$. This configuration can be selected through switch S3.

8.2 Digital Control

The digital control signals can be applied directly to J7 (top or bottom side). The modular ADS1259EVM can also be connected directly to a DSP or microcontroller interface board, such as the 5-6k Interface or HPA-MCU Interface boards available from Texas Instruments, or the MMB0 if purchased as part of the ADS1259EVM-PDK. For a list of compatible interface and/or accessory boards for the EVM or the ADS1259, see the relevant product folder on the TI web site. Some of the digital signals are controlled directly with pins on J7.

Other pins on the ADS1259 may be accessed via J7 through J2, J3, and J4. The ADS1259EVM-PDK uses the PGA280 external chip select function to control the ADS1259; therefore, these jumpers must be set to allow for access through J7.

8.3 Default Jumper Settings and Switch Positions

Jumpers connect the power supplies and enable PGA280 control of the ADS1259. J1, J2, J3, and J4 are all set to the left and connect the PGA280 to ADS1259. All the jumpers on J6 and J10 are used to connect power supplies and grounds. J15 is used to short the inputs together during an offset calibration. Figure 7 shows the jumpers found on the EVM and the respective factory default conditions for each.

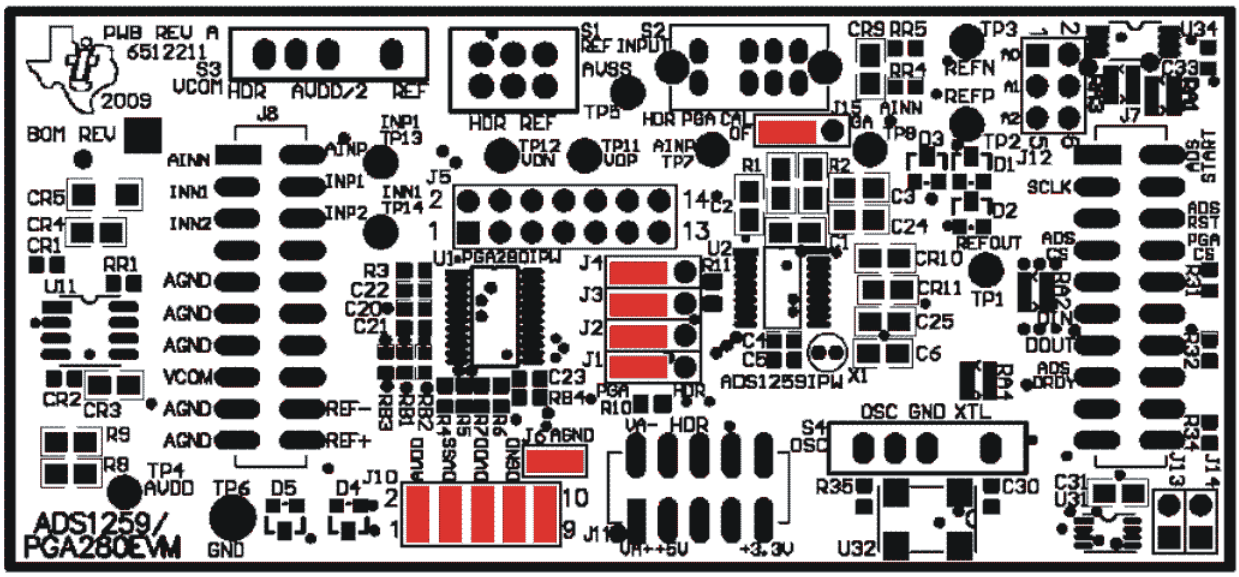


Figure 7. ADS1259EVM Default Jumper Positions

Four switches are used on the ADS1259/PGA280. Three-way switch S1 is set to the center position, setting the output common-mode of the PGA280 to AVDD/2. Switch S2 is set to the right, connecting the ADS1259 reference to the EVM onboard reference. Three-way switch S3 is set to the right to allow for calibration of the ADS1259, through jumper J15. Finally, three-way switch S4 is set to the left connecting the ADS1259 to the onboard oscillator. Figure 8 illustrates the switches on the EVM and the respective factory default configurations for each.

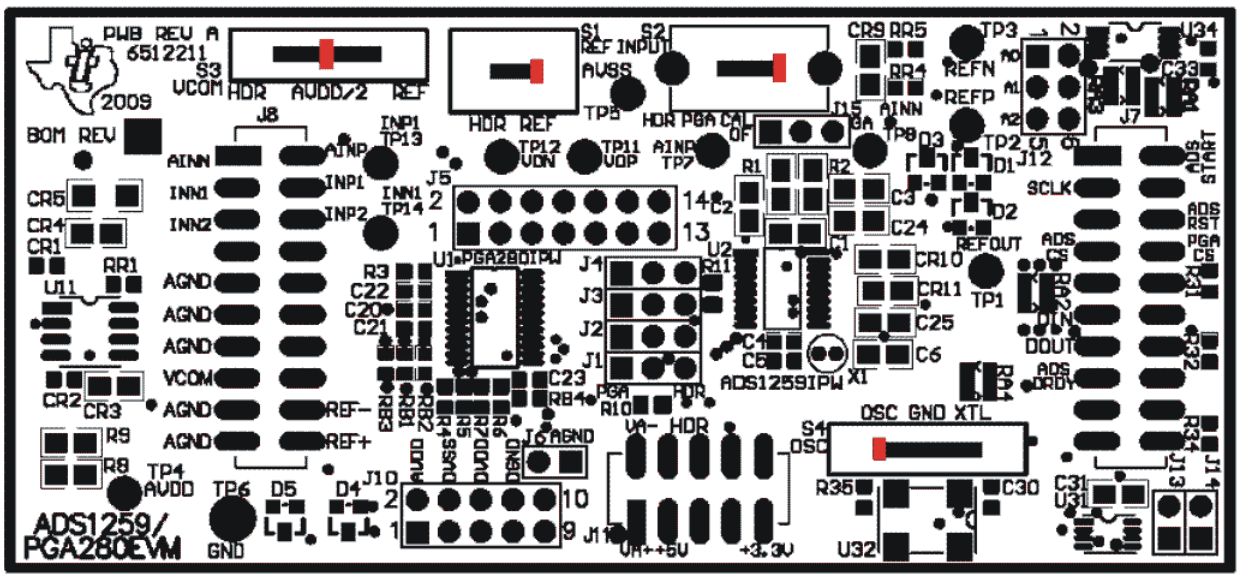


Figure 8. ADS1259EVM Default Switch Positions

9 ADS1259EVM-PDK Operation

This section provides information on using the ADS1259EVM-PDK, including setup, program installation, and program usage.

To prepare to evaluate the ADS1259 with the ADS1259EVM-PDK, complete the following steps:

Step 1. Install the ADCPro software (if not already installed) on a PC.
Step 2. Install the ADS1259EVM-PDK EVM plug-in software.
Step 3. Set up the ADS1259EVM-PDK.
Step 4. Connect a proper power supply or ac adapter.
Step 5. Complete the NI-VISA™ USB driver installation process.
Step 6. Run the ADCPro software.
Step 7. Complete the Microsoft Windows USB driver installation process.

Each task is described in the subsequent sections of this document.

9.1 Installing the ADCPro Software

CAUTION

Do not connect the ADS1259EVM-PDK before installing the software on a suitable PC. Failure to observe this caution may cause Microsoft Windows to not recognize the ADS1259EVM-PDK.

The latest software is available from the TI website at http://www.ti.com/tool/ADS1259EVM-PDK. Refer to the ADCPro User's Guide for instructions on installing and using ADCPro.

To install the ADS1259EVM-PDK plug-in, run the file: **ADS1259EVM-pdk-plug-in-1.0.0.exe** (*1.0.0* is the version number, and increments with software version releases). Double-click the file to run it; then follow the instructions shown.

Installation for the ADS1259EVM plug-in should be relatively straightforward. The plug-in comes as an executable file. Once started, the program leads the user through the screens shown in Figure 9 through Figure 12.

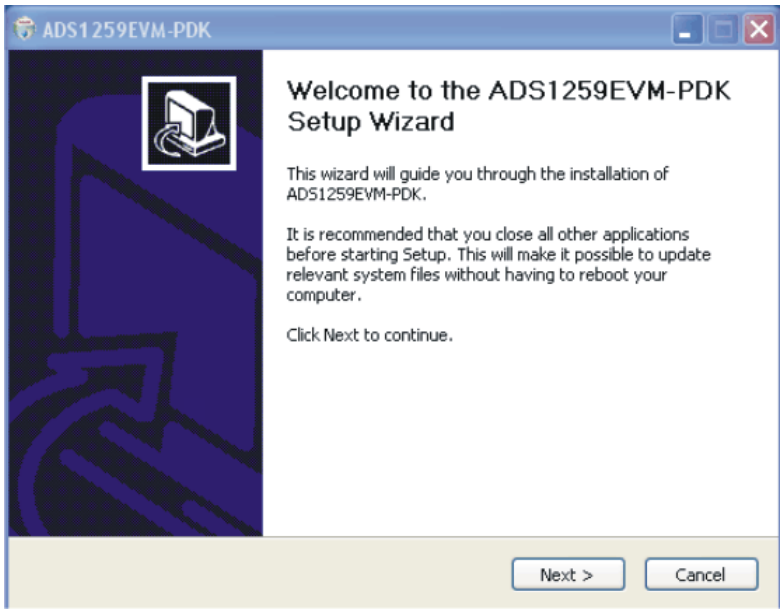


Figure 9. ADS1259EVM-PDK Setup Wizard: Screen 1

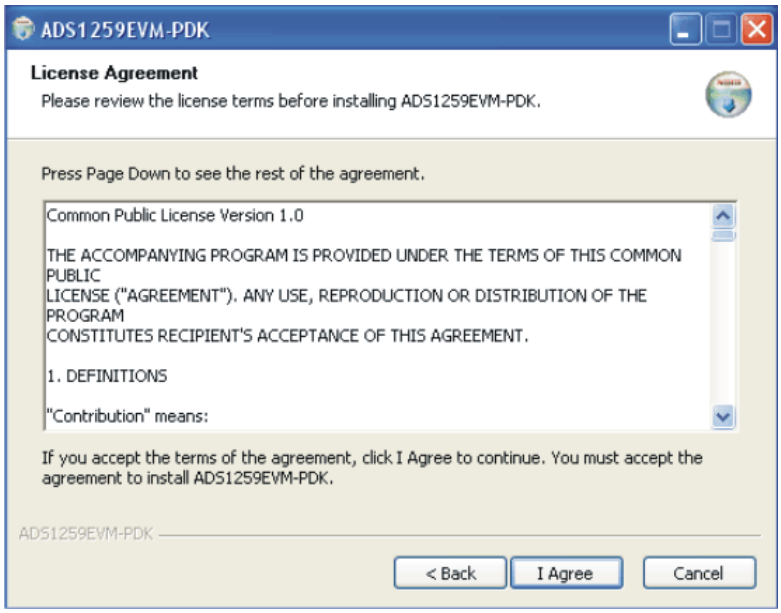


Figure 10. ADS1259EVM-PDK Setup Wizard: Screen 2

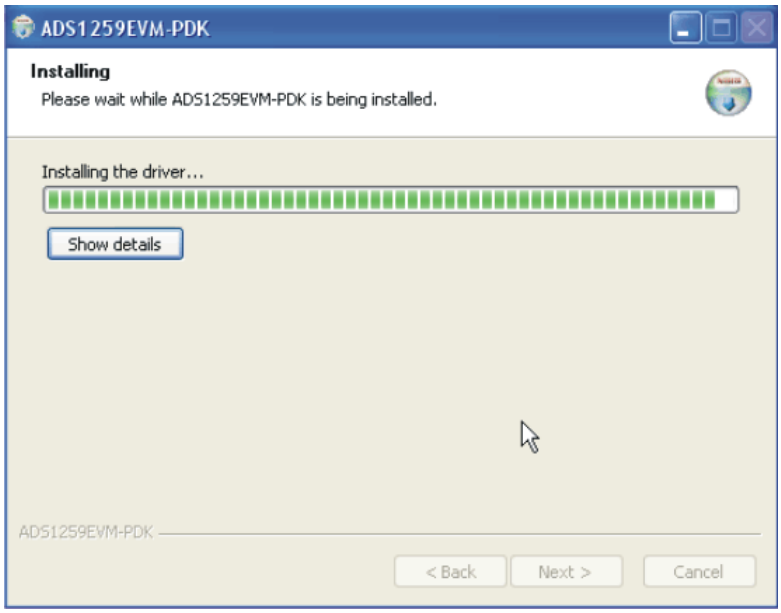


Figure 11. ADS1259EVM-PDK Setup Wizard: Screen 3

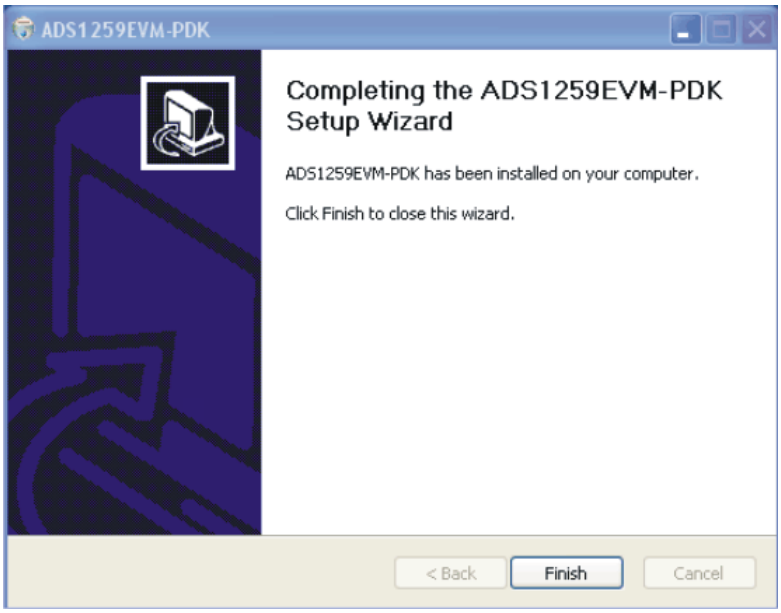


Figure 12. ADS1259EVM-PDK Setup Wizard: Screen 4

The software should now be installed, but the USB drivers may not yet have been loaded by the PC operating system. This step completes when the ADCPro software is executed; see Section 9.4, *Running the Software and Completing Driver Installation*.

9.2 Setting Up the ADS1259EVM-PDK

The ADS1259EVM-PDK contains both the ADS1259EVM and the MMB0 motherboard; however, the devices are shipped unconnected. Follow these steps to set up the ADS1259EVM-PDK:

Step 1. Unpack the ADS1259EVM-PDK package.

Step 2. Set the jumpers and switches on the MMB0 as shown in Figure 13.

- Set the Boot Mode switch to USB.
- Connect +5V and +5VA on jumper block J13 (if +5V is supplied from J14 +5VA).
- Leave +5V and +5VA disconnected on jumper block J13.
- If the PDK will be powered from an ac adapter, connect J12. If the PDK will be powered through the terminal block, disconnect J12 (see Section 9.3 for details on connecting the power supply).

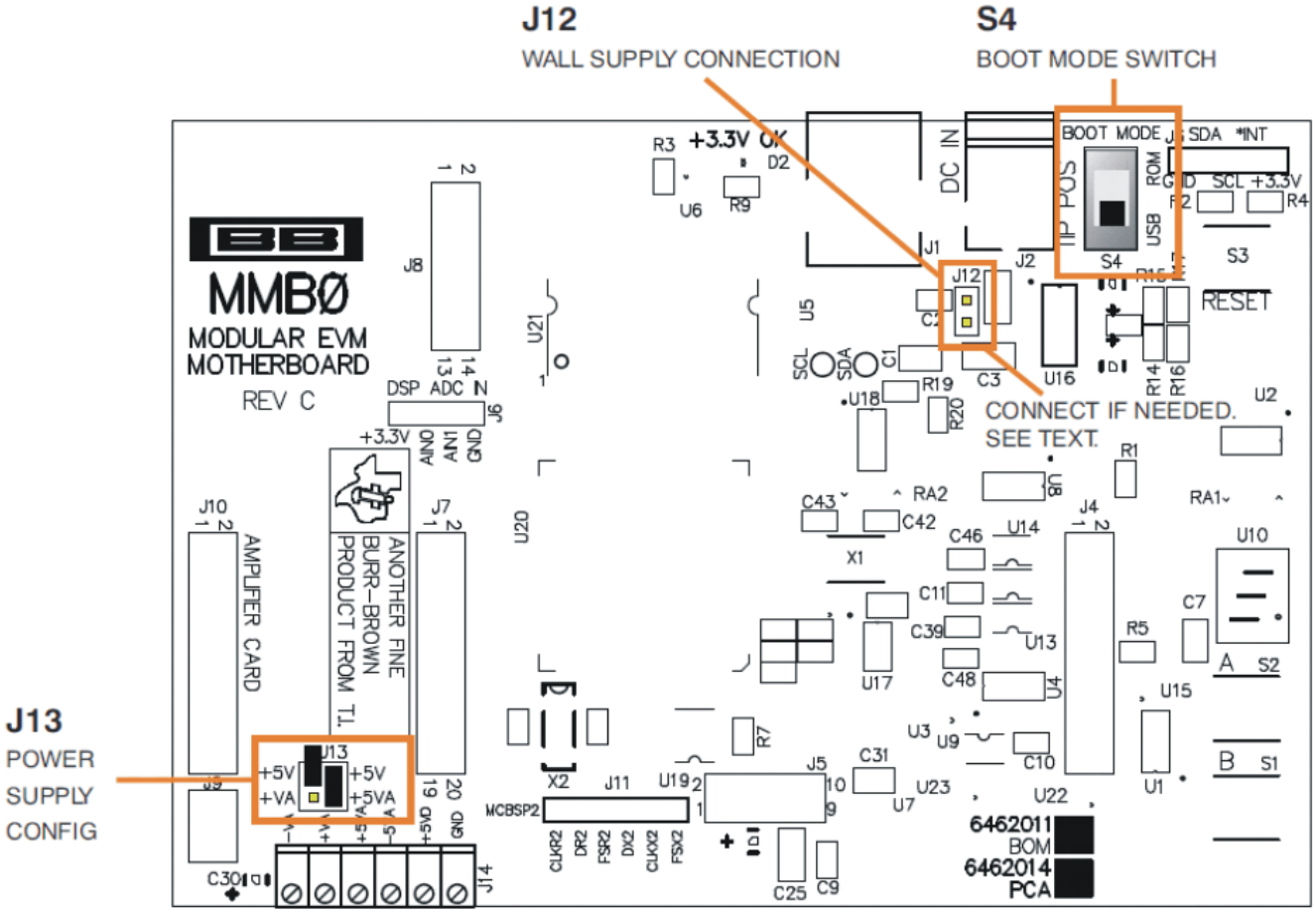


Figure 13. MMB0 Initial Configuration

Step 3. Plug the ADS1259EVM into the MMB0 as Figure 14 illustrates.

CAUTION

Do not misalign the pins when plugging the ADS1259EVM into the MMB0. Check the pin alignment carefully before applying power to the PDK.

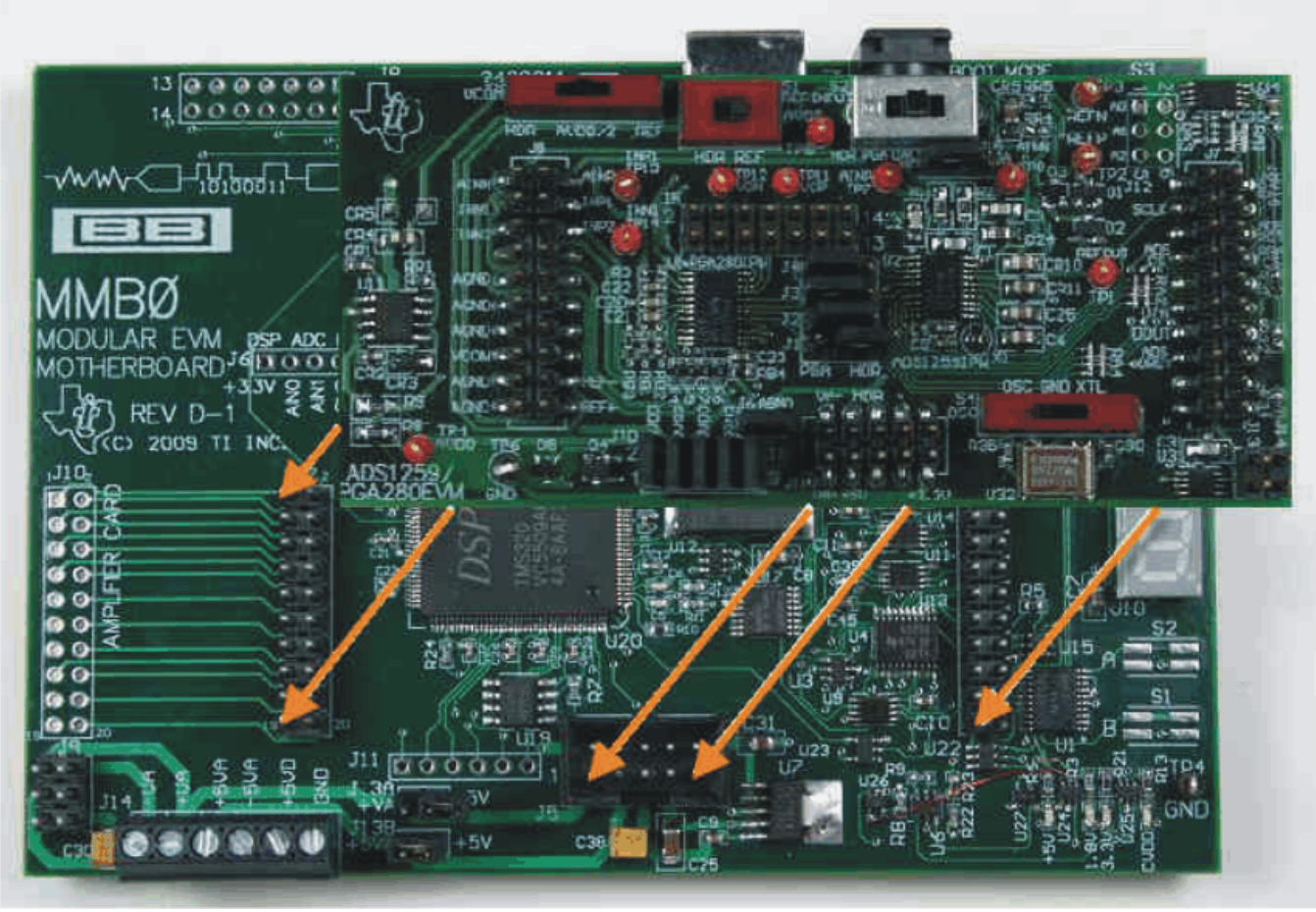


Figure 14. Connecting the ADS1259EVM to the MMB0

9.2.1 About the MMB0

The MMB0 is a Modular EVM System motherboard. It is designed around the TMS320VC5507, a DSP with an onboard USB interface from Texas Instruments. The MMB0 also has 16MB of SDRAM installed.

The MMB0 is not sold as a DSP development board, and it is not available separately. TI cannot offer support for the MMB0 except as part of an EVM kit. For schematics or other information about the MMB0, contact Texas Instruments.

9.3 Connecting the Power Supply

The ADS1259EVM-PDK can be operated with a combination of +5V and bipolar (±10V to ±15V) supply.

When the MMB0 DSP is powered properly, LED D2 glows green. The green light indicates that the 3.3V supply for the MMB0 is operating properly. (It does **not** indicate that the EVM power supplies are operating properly.)

9.3.1 Using a Wall Supply for +5V

An ac adapter can be connected to barrel jack J2 on the MMB0. J2 is located next to the USB connector.

Jumper J12 on the MMB0 connects a wall-mounted power supply to the board. To use the wall-mount supply, J12 must be shorted. Figure 15 illustrates how to connect an ac adapter to the MMB0.

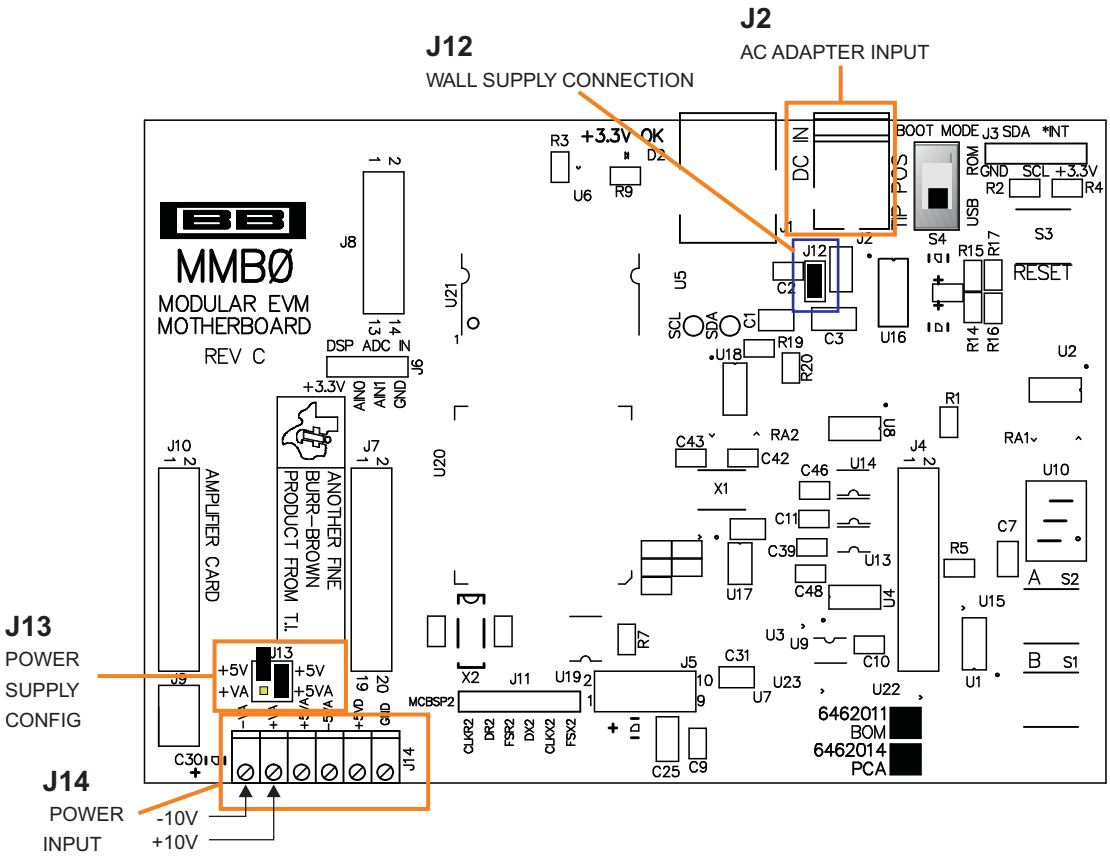


Figure 15. Using a Wall Supply for +5V

9.3.1.1 External Wall-Adapter Power-Supply Requirements

The external wall-adapter power-supply requirements are as follows:

- Output voltage: 6 VDC to 7 VDC
- Maximum output current: ≥ 2 A
- Output connector: barrel plug (positive center), 2.0-mm I.D. × 5.5-mm O.D. (9-mm insertion depth)

NOTE: Use an external power supply that complies with applicable regional safety standards; for example, UL, CSA, VDE, CCC, PSE, and so forth.

9.3.2 Using an External Supply for +5V

A laboratory power supply can be connected through terminal block J14 on the MMB0, as shown in Figure 16. Both unipolar and bipolar configurations are supported.

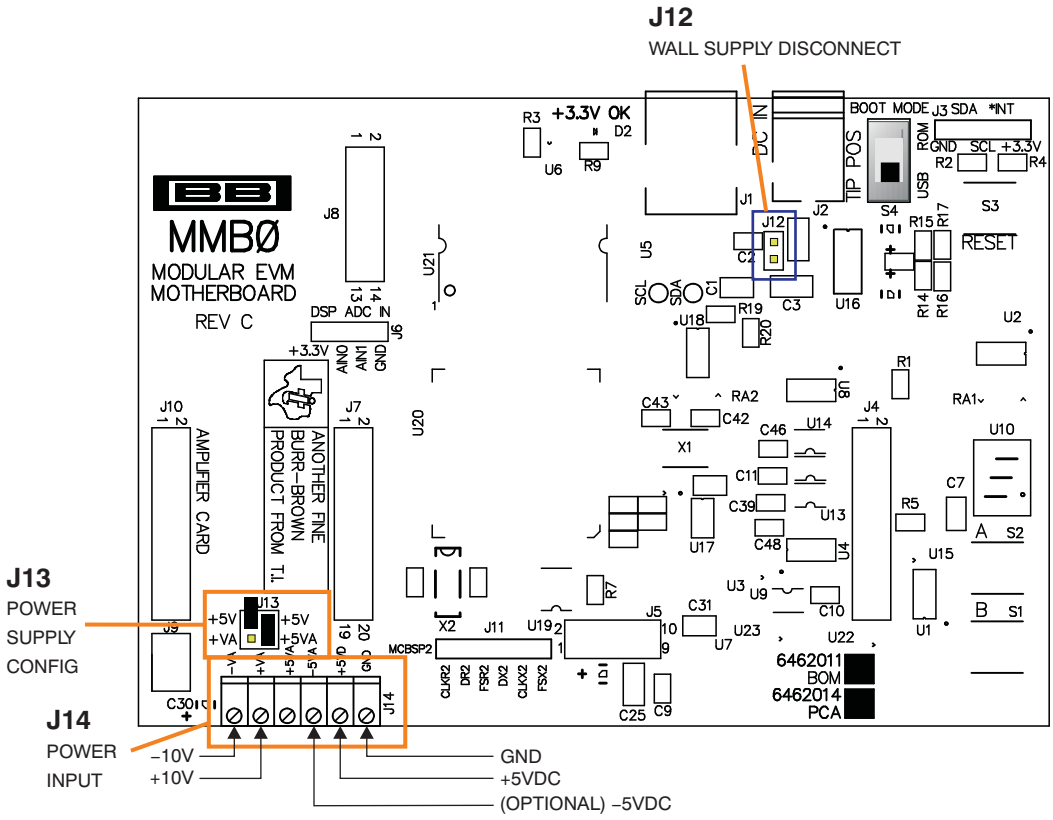


Figure 16. MMB0 Configured for Lab Power Supply

To use a lab power-supply configuration:

- Disconnect J12 on the MMB0.
- Connect a +5V dc supply to the +5VA terminal on J14.
- Connect ground of the dc supply to the GND terminal on J14.
- Connect a –10V dc supply to the –VA, and +10V on the +VA terminals on J14.

For bipolar mode, connect at –5V supply to –5VA.

It is not necessary to connect a +5V dc supply voltage to the +5VA terminal on J14 if the +5V/+5VA position on J13 is shorted.

9.4 Running the Software and Completing Driver Installation

NOTE: The software is continually under development. These instructions and screen images are current at the time of this writing, but may not exactly match future releases.

The program for evaluating the ADS1259EVM-PDK is called ADCPro. This program uses plug-ins to communicate with the EVM. The ADS1259EVM-PDK plug-in is included in the ADS1259EVM-PDK package.

The program currently runs only on Microsoft Windows platforms of Windows XP; Windows Vista and Windows 7 are **NOT** supported.

If this is the first time installing ADCPro and plug-ins, follow these procedures to run ADCPro and complete the necessary driver installation. Make sure the ADCPro software and device plug-in software are installed from the CD-ROM as described in Section 9.1.

9.4.1 NI-VISA USB Device Driver Installation

1. After the ADCPro software is installed, apply power to the PDK and connect the board to an available PC USB port.
2. The computer should recognize new hardware and begin installing the drivers for the hardware. Figure 17 through Figure 20 are provided for reference to show the installation steps.
   - For the first screen, Figure 17, it is not necessary to search for the software; it has already been installed on your PC.
   - For the remaining steps, accept the default settings.

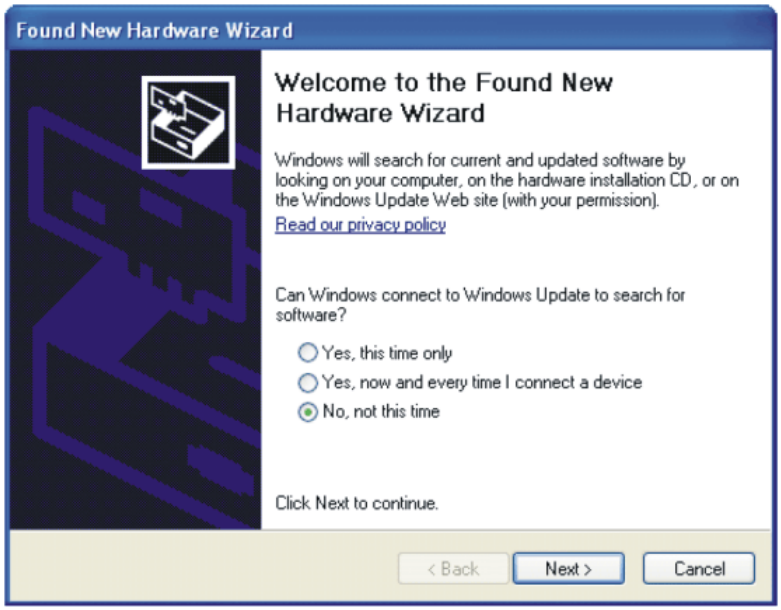


Figure 17. NI-VISA Driver Installation Wizard, Screen 1

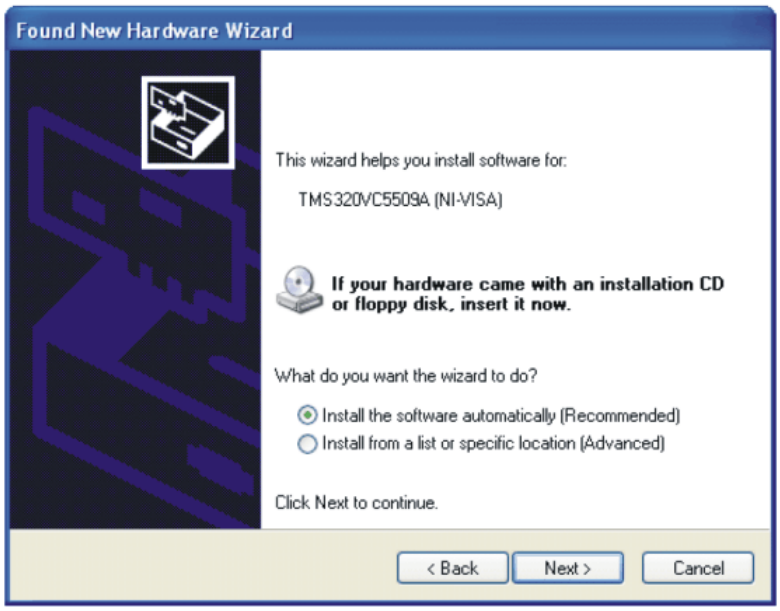


Figure 18. NI-VISA Driver Installation Wizard, Screen 2

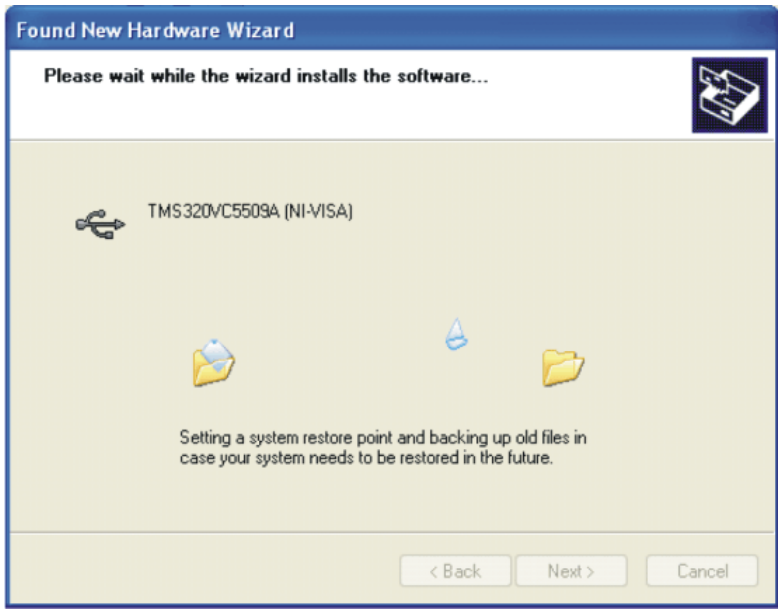


Figure 19. NI-VISA Driver Installation Wizard, Screen 3

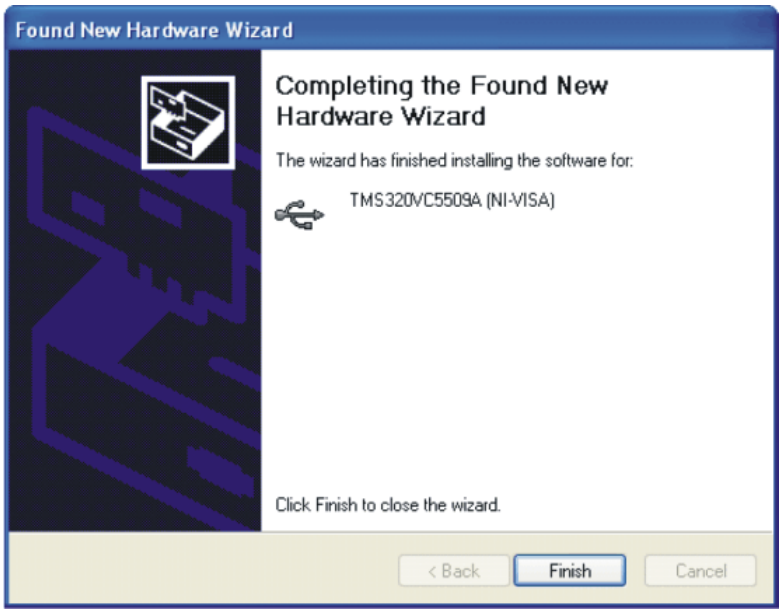


Figure 20. NI-VISA Driver Installation Wizard, Screen 4

This procedure should complete the installation of the NI-VISA drivers. You can verify proper installation by opening the Windows Device Manager and locating the drivers as shown in Figure 21.

Figure 21. NI-VISA Driver Verification Using Device Manager

9.4.2 USBStyx Driver Installation

1. Start the software by selecting *ADCPro* from the Windows Start menu. The screen in Figure 22 appears.

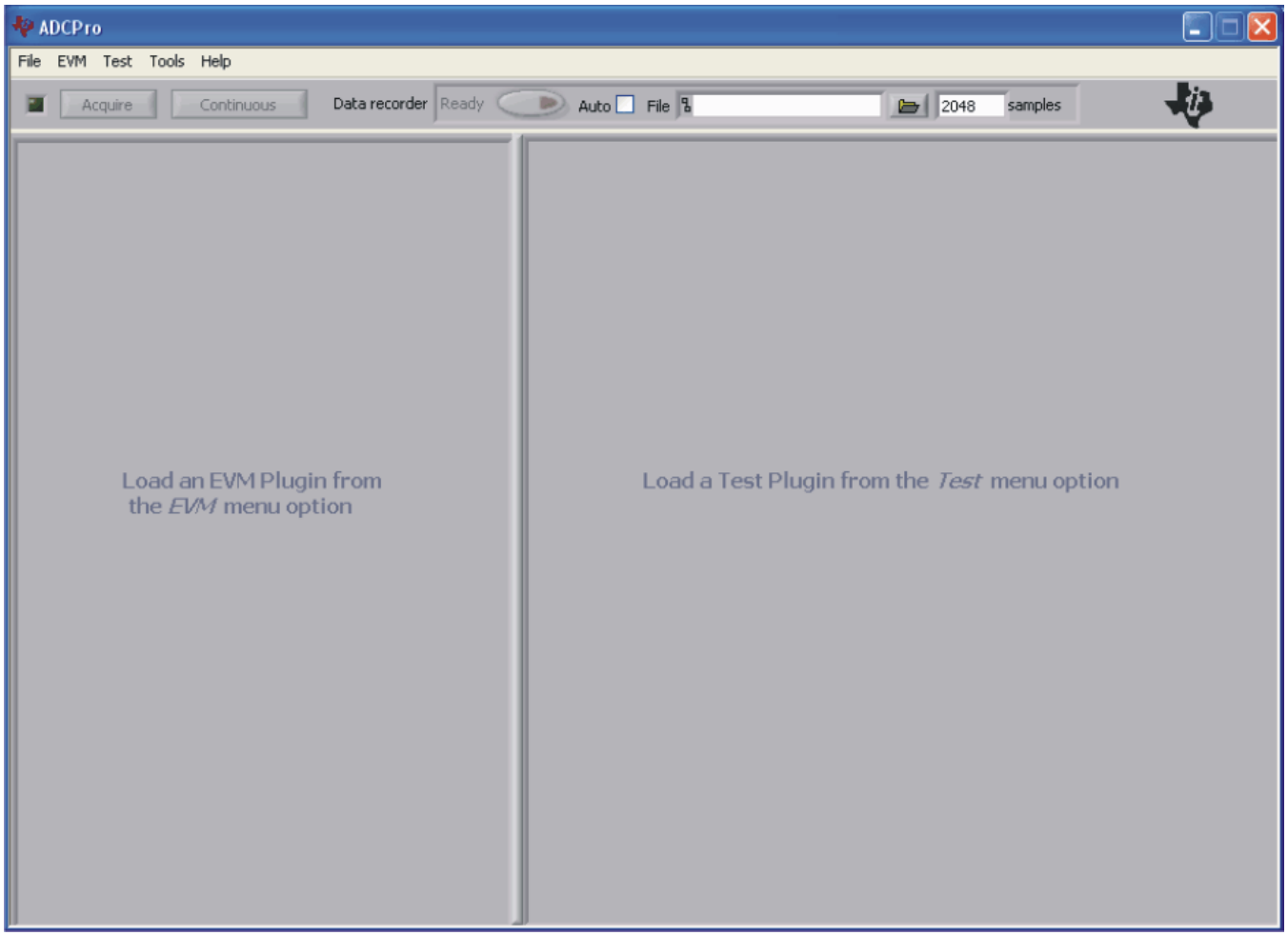


Figure 22. ADCPro Software Start-up Display Window

2. Select *ADS1259EVM* from the EVM drop-down menu. The ADS1259EVM-PDK plug-in appears in the left pane, as shown in Figure 23.

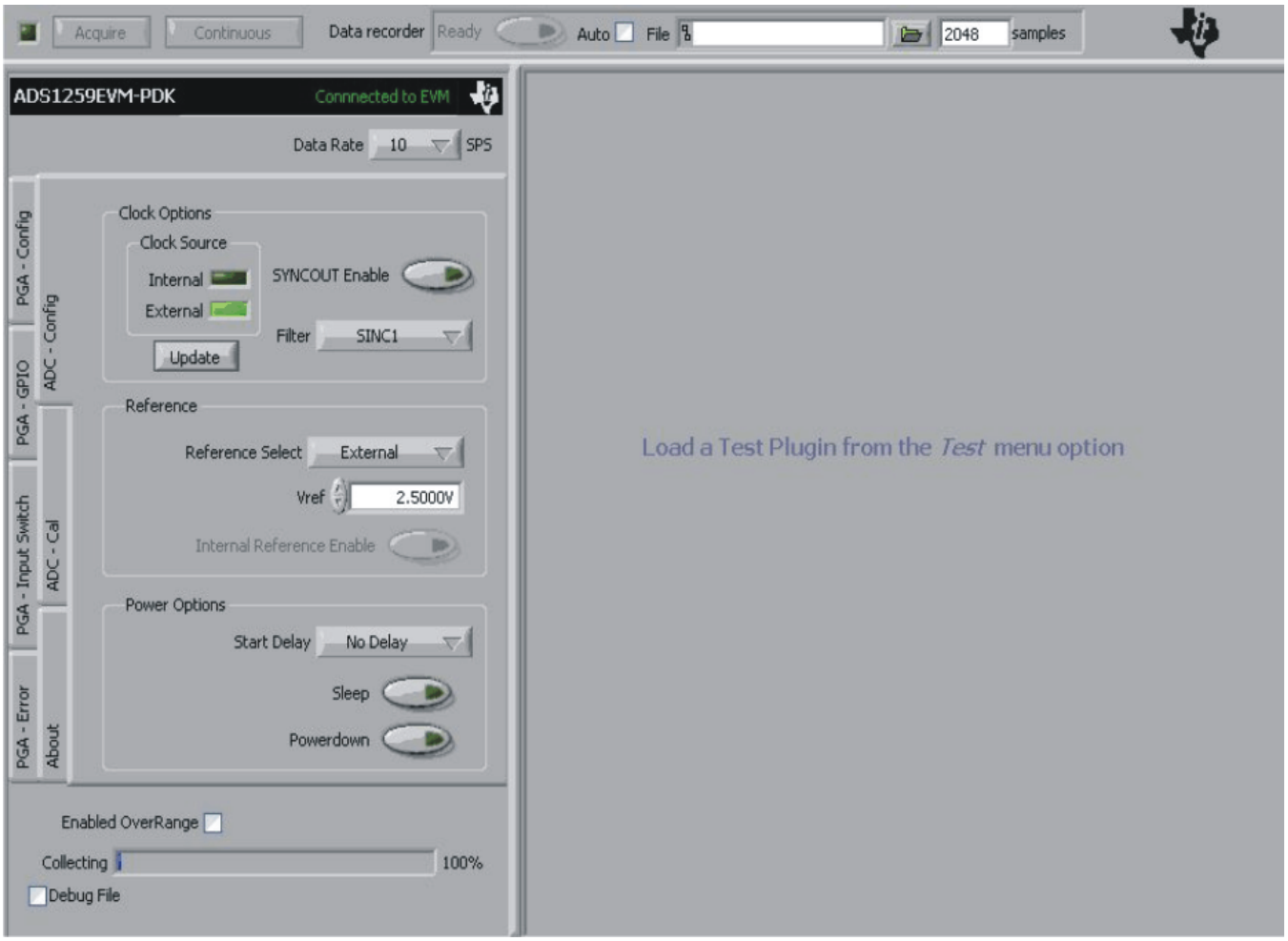


Figure 23. ADS1259EVM-PDK Plug-In Display Window

3. The ADS1259EVM-PDK plug-in window has a status area at the top of the screen. When the plug-in is first loaded, the plug-in searches for the board. You will see a series of messages in the status area indicating this action.
4. If you have not yet loaded the operating system drivers, Windows will display the Windows *Install New Driver Wizard* sequence (illustrated in Figure 24 through Figure 28). Accept the default settings.

NOTE: During the driver installation, a message may appear indicating the firmware load has TIMED OUT. Click OK and continue driver installation. The plug-in attempts to download the firmware again once the driver installation completes.

Figure 24. Install New Driver Wizard Screen 1

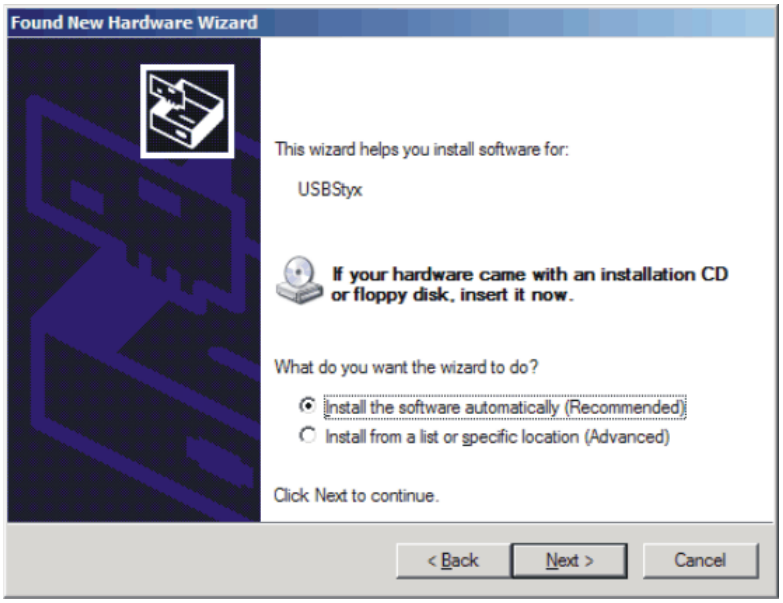


Figure 25. Install New Driver Wizard Screen 2

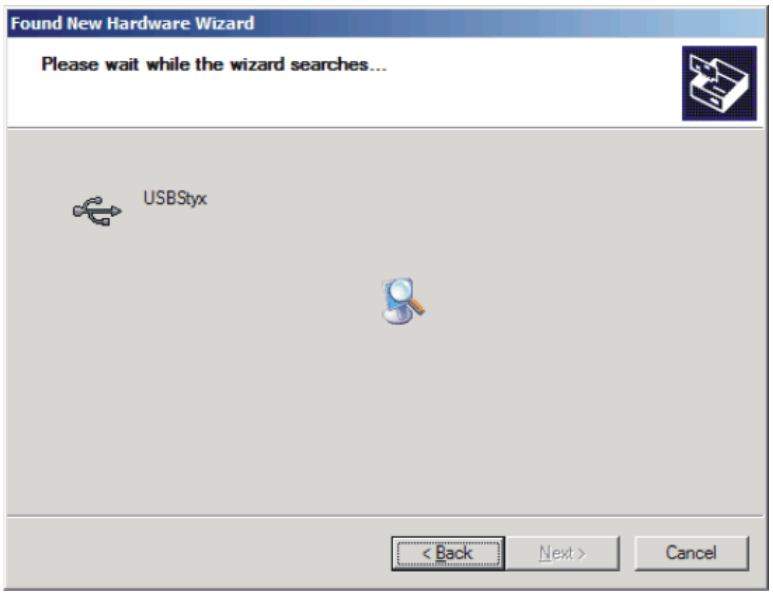


Figure 26. Install New Driver Wizard Screen 3

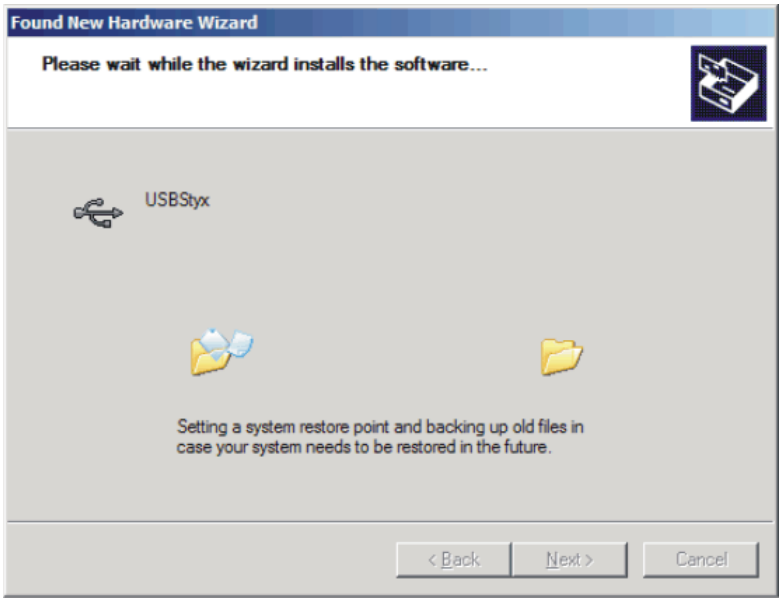


Figure 27. Install New Driver Wizard Screen 4

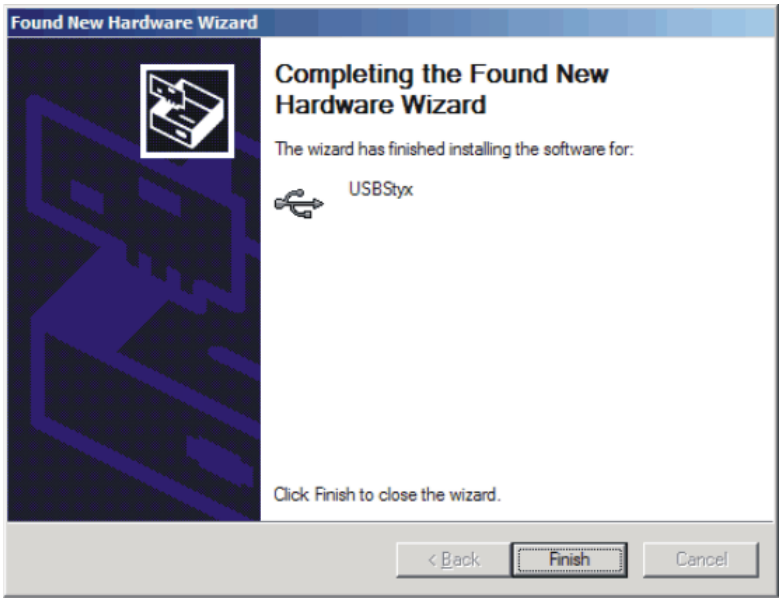


Figure 28. Install New Driver Wizard Screen 5

5. Once Windows finishes installing the software driver, the plug-in downloads the firmware to the MMB0. The status area displays *Connected to EVM* when the device is connected and ready to use. If the firmware does not load properly, you can try resetting the MMB0 by pressing *Reset* and then reloading the plug-in.
6. You can verify the proper installation of the USBStyx driver using the Device Manager. Note that the first driver item, NI-VISA USB Devices, disappears and a new item, LibUSB-Win32 Devices appears, as Figure 29 shows.

Figure 29. USBStyx Driver Verification Using Device Manager

The driver installation wizard sequence should not appear again, unless you connect the board to a different USB port.

10 Evaluating Performance with the ADCPro Software

The evaluation software is based on ADCPro, a program that operates using a variety of plug-ins. (The ADS1259EVM plug-in is installed as described in the installation section, Section 9).

To use ADCPro, load an EVM plug-in and a test plug-in. To load an EVM plug-in, select it from the *EVM* menu. To load a test plug-in, select it from the *Test* menu. To unload a plug-in, select the *Unload* option from the corresponding menu.

Only one of each kind of plug-in can be loaded at a time. If you select a different plug-in, the previous plug-in is unloaded.

10.1 Using the ADS1259EVM-PDK plug-in

The ADS1259EVM-PDK plug-in for ADCPro provides complete control over settings of the ADS1259 and the PGA280. It consists of a tabbed interface, with different functions available on different tabs. These controls are described in this section.

You can adjust the ADS1259EVM settings when you are not acquiring data. During acquisition, all controls are disabled and settings may not be changed.

When you change a setting on the ADS1259EVM plug-in, the setting immediately updates on the board.

Settings on the ADS1259EVM correspond to settings described in the ADS1259 data sheet and the PGA280 data sheet (available for download at www.ti.com) for details.

10.1.1 ADC Data Rate

ADCPro can receive data from the ADS1259 at eight different data rates. The data rate is controlled by the **Data Rate** control tab (shown in Figure 30) at the upper right portion of the plug-in window. The data rate default upon start up is 10 samples per second (SPS) with options to change the data rate to 16.67, 50, 60, 400, 1200, 3600, and 14,4400 SPS.

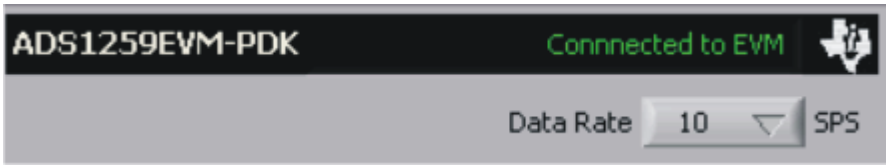


Figure 30. Data Rate Control

10.1.2 ADC Over Range Flag

The ADS1259 has over-range detection for the modulator. If the differential input exceeds 105% of the range, then the ADC Over Range Flag light indicates the condition, as Figure 31 illustrates. Note that this function must be enabled; it is implemented by using the 24th data bit as the over-range indicator. This indicator is only updated at the end of a data acquisition event by ADCPro. The indicator is located at the bottom right side of the ADS1259/PGA280 EVM plug-in.

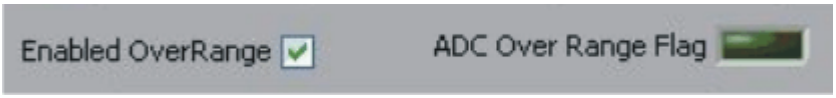


Figure 31. Over-Range Flag

10.1.3 ADC Configuration Tab

The first tab for the ADS1259EVM is the ADC Configuration Tab. This set of controls is used primarily for setting up the operation for the ADS1259. This tab is broken up into three subsections. The ADC Configuration tab is shown in Figure 32.

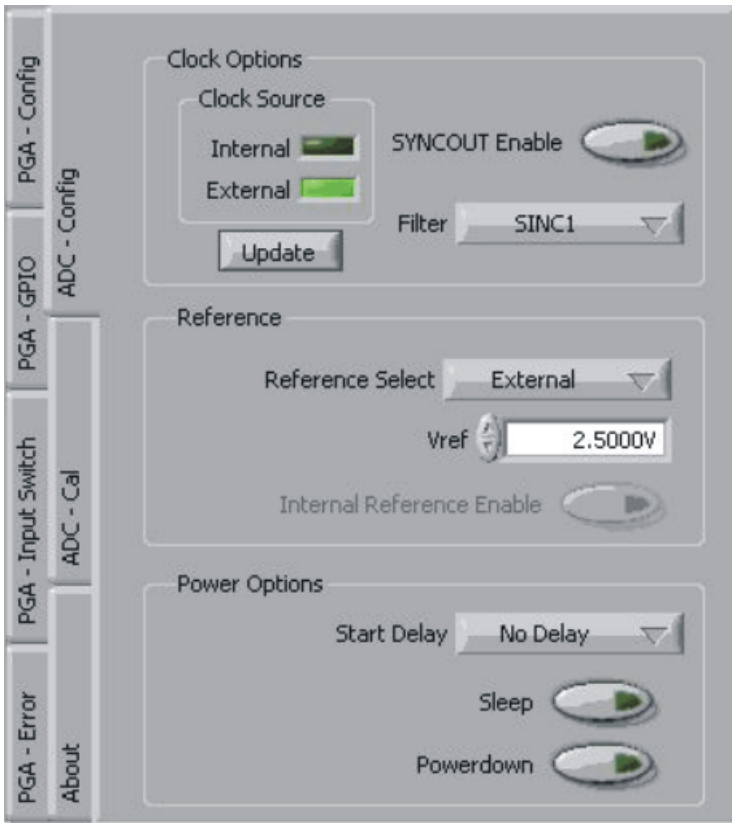


Figure 32. ADC Configuration Tab

The first subsection is **Clock Options**. This set of controls is used primarily for monitoring and setting different clock and filter options. First, two indicator lights show the clock source for the ADC, showing if the master clock source is generated from the internal oscillator, or from some external source. The clock source indicator is shown at the start up of the plug-in. It can be re-read with the Update button.

A push button labeled **SYNCOUT** allows for a divided modulator clock to be put onto the SYNCOUT pin of the ADS1259. This can be used to drive the input chopping of the PGA280. To synchronize the two devices, the PGA280 must be set to *External* (as shown in the PGA-Config tab under the Sync pull-down; see Figure 34) and connected through pins 2 and 3 of J1 on the ADS1259EVM.

There are two different digital filter options for the ADS1259. A fixed decimation sinc5 filter is then followed by either a sinc1 filter or a sinc2 filter that is selected by the pull-down menu labeled *Filter*.

The second subsection is used to control the reference. The ADC reference source can be selected here to be either the internal, onboard reference of the ADS1259 or the external reference seen on VREFP and VREFN. The VREF voltage is adjusted here for readings for plug-in tools.

In order to use the internal reference, it must be enabled with the Internal Reference Enable button.

The final subsection of the ADC Configuration tab is Power Options. With the ADS1259, conversions can be initiated by the rising edge of START. The pull-down menu labeled Start Delay, will delay the part coming out of startup to allow external circuitry to settle before a conversion is started. The pull-down menu can be used to set the delay to a fixed time as a function of the master clock period. While this function is not useful in reading out data from the device, it is observable by using one of the PGA280 GPIO pins to toggle the START pin of the ADS1259. Afterward, the delay of the $\overline{\text{DRDY}}$ pin can be seen.

There are two power reduction modes that can be used to reduce the quiescent current of the ADS1259 when the part is not in use. They are enabled by clicking the buttons labeled Sleep and Powerdown. In SLEEP mode, device power is reduced to a minimum; only essential internal functions are kept active. This condition includes the R_{BIAS} status to keep the reference on, if enabled, and some digital function. To exit SLEEP mode, toggling the button issues the WAKEUP command. The absolute lowest power is achieved in Power-Down mode. Both SLEEP mode and Power-Down modes can be accessed through the buttons at the bottom of this tab.

10.1.4 ADC Calibration Tab

A calibration feature is integrated into the ADS1259 to correct for offset and gain errors. The ADS1259EVM-PDK software is designed to allow the user to use the built-in system calibration commands or manually calibrate the device by directly entering the values for the offset and gain registers of the ADS1259. Figure 33 shows the ADC calibration tab.

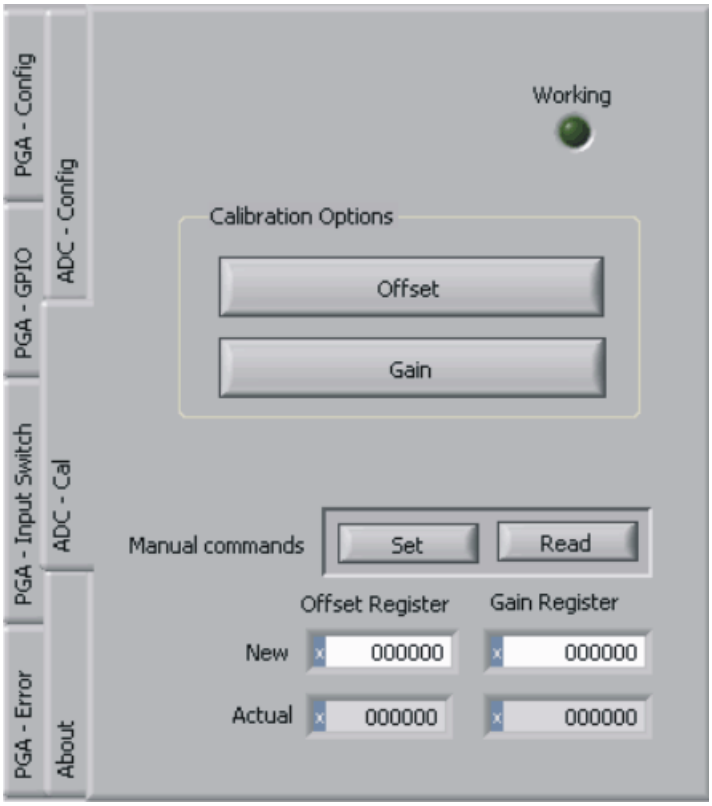


Figure 33. ADC Calibration Tab

In the Calibration Options subsection, two buttons allow for an offset calibration and a gain calibration. First, the offset calibration can be done when the inputs are shorted. As described earlier, the part can be shorted by setting the three way switch S2 to the right most position labeled CAL, and by setting a jumper across the left two pins of jumper J15. Then the gain calibration can be performed by keeping the setting of switch S2 and by moving the jumper to the right side of J15. During calibration, the Working indicator light shows that the device is performing the calibration and cannot be updated at that time.

At the bottom of this tab, there are two buttons that allow for reading and writing to the Offset Calibration Register and the Gain (Full-Scale) Calibration Register. To set a register value, enter it into the New space, and push the Set button. To read back the register push the Read button, and the value is updated in the space labeled Actual.

10.1.5 PGA Configuration Tab

The PGA Configuration Tab (shown in Figure 34) has options that allow for control of much of the PGA280.

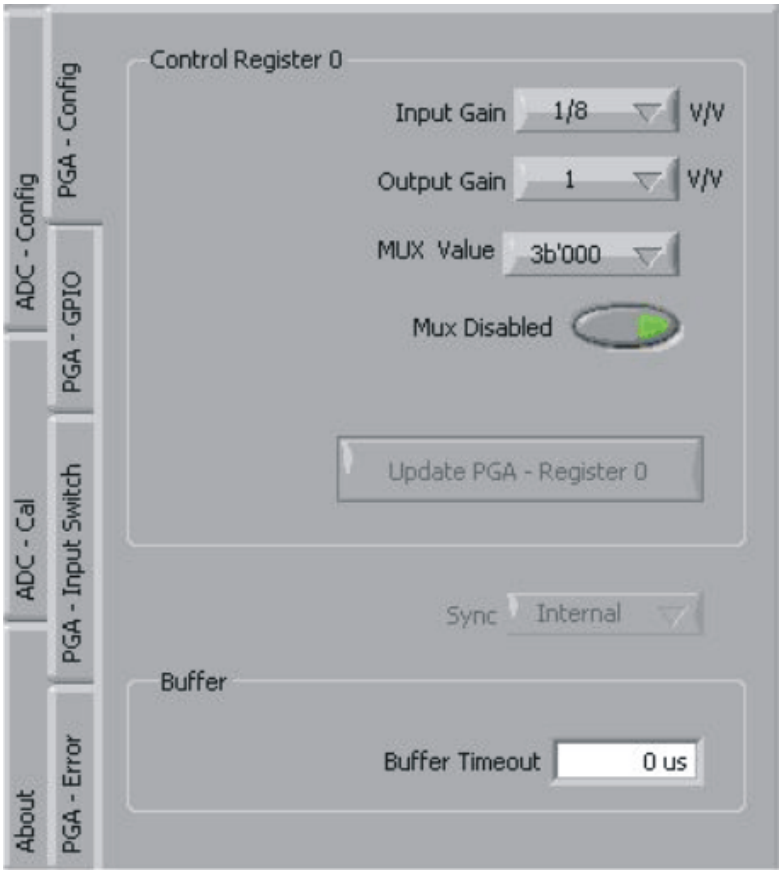


Figure 34. PGA Configuration Tab

The first subsection of this tab sets control register 0 in the PGA280. First, there is a pull-down menu that controls the input gain of the part, adjustable from 1/8V/V up to 128V/V with gains in factors of 2. A second pull-down menu sets the output gain to either 1V/V or 1-3/8V/V.

In this subsection, another pull-down menu allows the user to set an external multiplexer value through GPIO0-GPIO2. This option can be enabled with a push button and must also be set in the PGA GPIO tab.

Finally, control register 0 is written together with the Update PGA -Register 0 button. This feature allows for simultaneous switching of gain and the external mux. If the Input Gain, Output Gain, or MUX Value pull-down menus are changed, the Update PGA - Register 0 button becomes active and this button must be clicked to proceed with the changes.

A pull-down menu allows for the synchronization of the PGA280 chopper. The chopper can be synchronized to the internal clock of the PGA280 or to an external clock as supplied by the ADS1259. The two parts can be connected on the right side of J1 when the jumper connects pins 2 and 3. In order for this function to be enabled, the ADS1259 SYNCOUT pin must be enabled as found on the ADC Configuration tab (see Figure 32) with the SYNCOUT Enable.

The second subsection controls the Buffer of the PGA280. A pull-down menu allows for triggering the buffer based on a write to a register. The buffer is turned off after a preset time. This time is variable and can be written into the Buffer Timeout register in increments of 4µs, from 0µs to 252µs. To change the time, enter a value between 0 and 252, and the plug-in rounds the result to the nearest value divisible by four. Note that the buffer is only enabled with a change of the MUX value. For further information about the use of the current buffer, see the PGA280 data sheet.

10.1.6 PGA GPIO Tab

The PGA GPIO tab, as Figure 35 shows, allows for control of three of the GPIO pins (GPIO0-GPIO2) in the PGA280. These pins can be independently used as GPIO inputs, GPIO outputs, and external MUX mode. For each of these pins, select the desired function. If used as a GPIO output, a high or a low is selected with the Output push button. If used as a GPIO input, the value is shown by the indicator light on the right when the Read GPIO button is clicked.

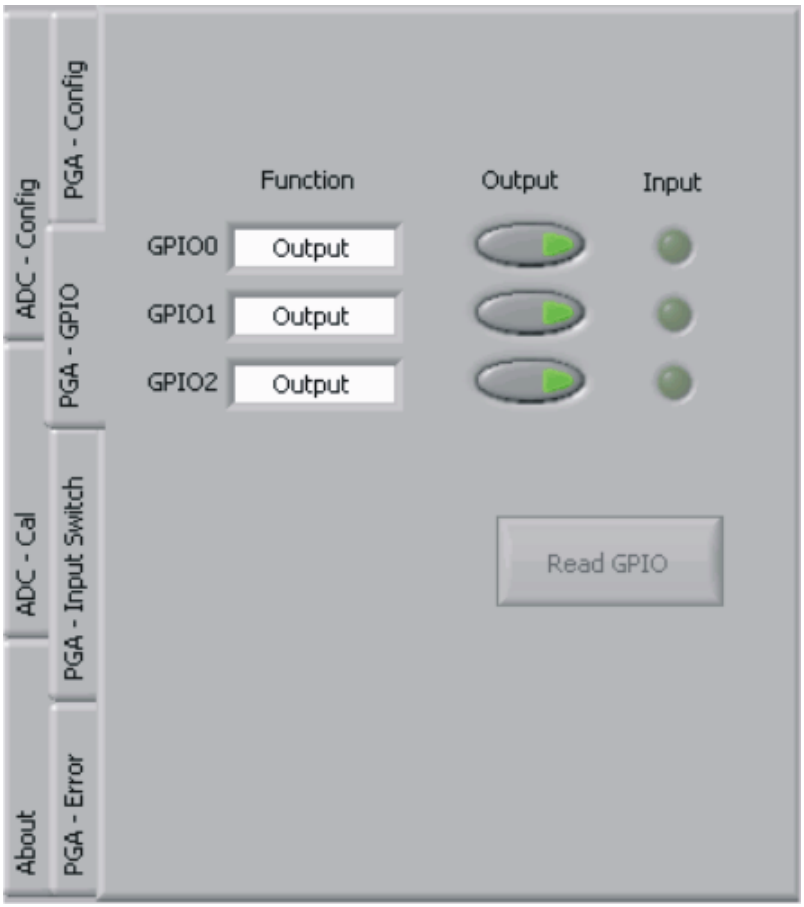


Figure 35. PGA GPIO Tab

Note that the control for setting the GPIO values in Mux mode is in the PGA Configuration tab, described in Section 10.1.5.

The remaining four GPIO pins (GPIO3-GPIO6) are reserved in $\overline{\text{ECS}}$ mode to control the ADS1259.

10.1.7 PGA Input Switch Tab

The PGA Input Switch Tab pulls up a diagram of the input switches available in the PGA280, as Figure 36 illustrates. These switches allow for switching in different inputs, buffers, supplies, and current sources. Click on the switch to enable or disable the switch. For more information about switch function and control, see the *Input Switch Network* section of the PGA280 data sheet.

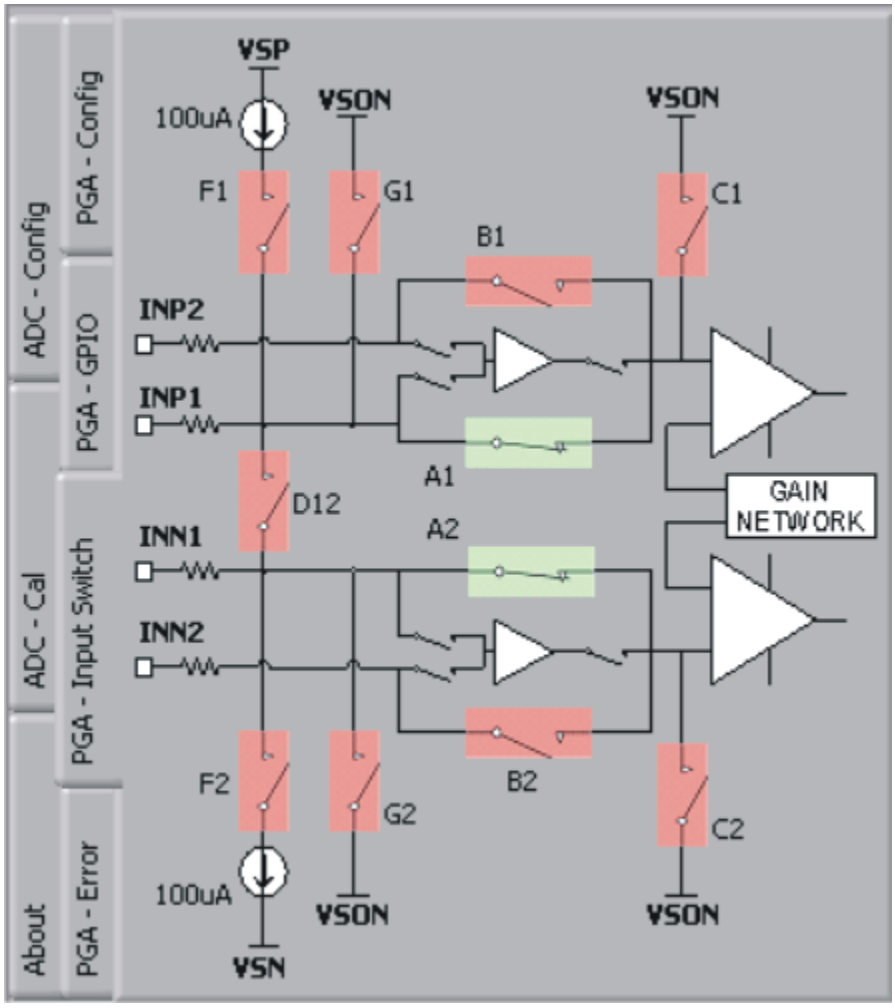


Figure 36. PGA Input Switch Tab

10.1.8 PGA Error Indicators Tab

The error indicators for the PGA280 can be seen on the PGA Error Indicator tab (shown in Figure 37). There are seven indicator lights that show error conditions in the PGA280.

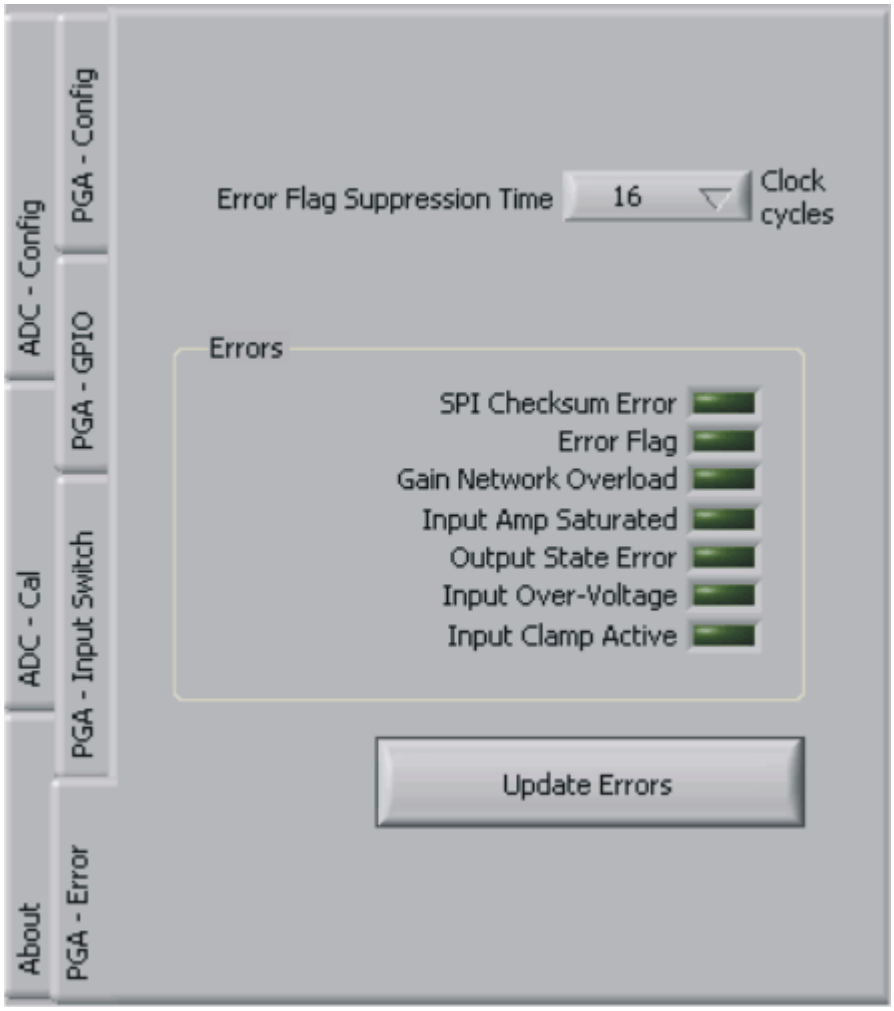


Figure 37. PGA Error Indicators Tab

Each error corresponds to a bit in the error register (register 4) of the PGA280. At the top of the tab, a pull-down menu selects the suppression time for the error flags. In the PGA280 data sheet, this period is referred to as FLAGTIM and can be found in register 11.

The Update Errors button clears the error register and updates the status of the error indicators on this tab. Note that as the device powers up for the first time, these error flags may be set. If you are going to use these flags, it is important to first clear them after the part has settled after start up.

10.1.9 About Tab

The About tab displays information about the EVM and software, as shown in Figure 38.

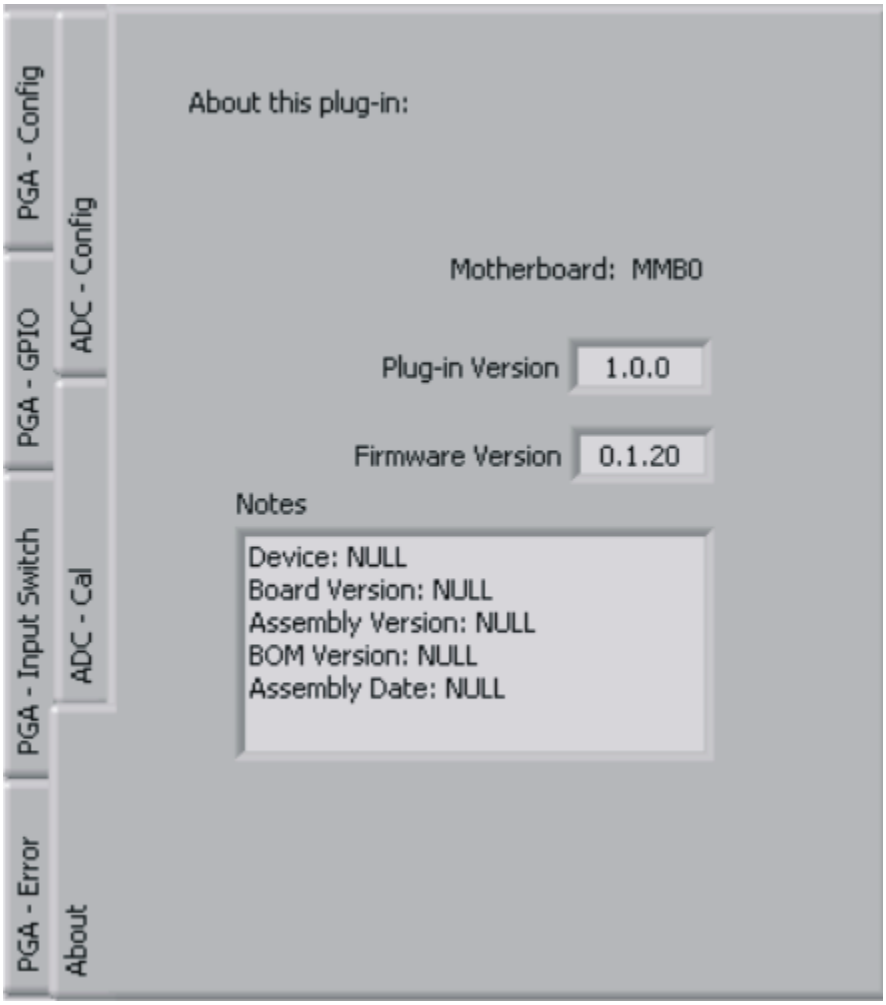


Figure 38. EVM Software About Tab

The Plug-in Version and Firmware Version indicators show the version numbers of the plug-in and firmware code, respectively.

The Notes indicator may show relevant notes about the plug-in or firmware code, if there are any.

10.1.10 Collecting Data

Once you have configured the ADS1259 for your test scenario, press the ADCPro **Acquire** button to start the collection of the number of data points specified in the Test plug-in *Block Size* control. The ADS1259EVM-PDK plug-in disables all the front panel controls while acquiring, and displays a progress bar as shown in Figure 39.

Figure 39. Software Progress Indicator

For more information on testing analog-to-digital converters in general and using ADCPro and Test plug-ins, refer to the ADCPro User's Guide.

10.2 Troubleshooting

If ADCPro stops responding while the ADS1259EVM-PDK is connected, try unplugging the power supply from the PDK. Unload and reload the plug-in before reapplying power to the PDK.

11 Schematics and Layout

Schematics for the ADS1259EVM are appended to this user's guide. The bill of materials is provided in Table 4.

11.1 Bill of Materials

Table 4. ADS1259EVM Bill of Materials

Item	RefDes	Quantity	Description	Part Number	MFR
1	N/A	1	Printed wiring board	6512211	Texas Instruments
2	C1, C31	2	Capacitor, C0G ceramic, 10nF ±5%, 25WV, Size = 0805	C2012C0G1E103J	TDK
3	C2, C3	2	Capacitor, C0G ceramic, 47pF ±5%, 50WV, Size = 0805	CC0805JRNP09BN470	Yageo
4	C4, C5	2	Capacitor, C0G ceramic, 18pF ±5%, 50WV, Size = 0603	C1608C0G1H180J	TDK
5	C6, CR9, CR10, CR11, C24, C25	6	Capacitor, X5R Ceramic 10uF ±20%, 16WV, Size = 0805	C2012X5R1C106MT	TDK
6	C20, C21, C22	3	Capacitor, X7R Ceramic 0.47uF ±10%, 25WV, Size = 0603	GRM188R71E474KA12D	Murata Electronics
7	C23	1	Capacitor, X7R Ceramic 0.1uF ±10%, 16WV, Size = 0603	C1608X7R1C104K	TDK
8	C33	1	Capacitor, X7R Ceramic 0.1uF ±10%, 25WV, Size = 0603	C1608X7R1E104KT	TDK
9	CR1, CR2, C30	3	Capacitor, X7R Ceramic 1µF ±10%, 16WV, Size = 0603	C1608X7R1C105KT	TDK
10	CR3	1	Capacitor, Tanatalum 10µF ±20%, 4WV, Size = 0805	TCP0G106M8R	Rohm
11	CR4	1	Capacitor, X5R Ceramic 22µF ±20%, 10WV, Size = 0805	LMK212BJ226MG-T	Taiyo Yuden
12	D1, D2, D4, D5	4	Diode, Schottky 30V 200mA SOT-23	BAT54FSCT	Fairchild
13	D3	1	Zener Diode SOT-23	MMBZ5231BLT1	ON Semiconductor
14	R3, R4, R5, R6, R7, R11	6	Resistor, Thick Film Chip 1kΩ, 1%, 1/10W, Size = 0603	ERJ-3EKF1001V	Panasonic
15	R1, R2	2	Resistor, Thick Film Chip 47Ω, 1%, 1/8W, Size = 0805	ERJ-6ENF47R0V	Panasonic
16	R8, R9	2	Resistor, Thick Film Chip 10kΩ, 1%, 1/8W, Size = 0805	ERJ-6ENF1002V	Panasonic
17	R10	1	Resistor, Thick Film Chip 100kΩ, 1%, 1/10W, Size = 0603	ERJ-3EKF1003V	Panasonic
18	R31, R32	2	Resistor, Thick Film Chip 2.7kΩ, 1%, 1/10W, Size = 0603	ERJ-3EKF2701V	Panasonic
19	R34, R35	2	Resistor, Thick Film Chip 470kΩ, 5%, 1/10W, Size = 0603	ERJ-3GEYJ474V	Panasonic
20	RA1	1	Resistor Array 100kΩ, 8-Term 4RES SMD	742C083104JP	CTS Resistor Products
21	RA2, RA4	2	Resistor Array 100Ω, 8-Term 4RES SMD	742C083101JP	CTS Resistor Products
22	RB1, RB2	2	Resistor, Thick Film Chip 22Ω, 1%, 1/10W, Size = 0603	ERJ-3EKF22R0V	Panasonic

Table 4. ADS1259EVM Bill of Materials (continued)

Item	RefDes	Quantity	Description	Part Number	MFR
23	RB3, RB4	2	Resistor, Thick Film Chip 10Ω, 1%, 1/10W, Size = 0603	ERJ-3EKF10R0V	Panasonic
24	RR1	1	Resistor, Thick Film Chip 10kΩ, 5%, 1/10W, Size = 0603	ERJ-3GEYJ103V	Panasonic
25	RR4, RR5	2	Resistor, Thick Film Chip 0Ω, 5%, 1/10W, Size = 0603	ERJ-3GEY0R00V	Panasonic
26	J1, J2, J3, J4, J15	5	1x3 100 mil male header	TSW-103-07-L-S	Samtec
27	J5	1	7x2 100 mil male header	TSW-107-07-L-D	Samtec
28	J6, J13, J14	3	1x2 100 mil male header	TSW-101-07-L-D	Samtec
29	J7A, J8A	2	Mini-EVM serial header: Top, 10x2x.1_SMT	TSM-110-01-L-DV-P	Samtec
30	J7B, J8B	2	Mini-EVM serial header: Bottom, 10x2x.1_SMT	SSW-110-22-F-D-VS-K	Samtec
31	J10	1	5x2 100 mil male header	TSW-105-07-L-D	Samtec
32	J11A	1	5x2x.1_SMT	TSM-105-01-L-DV-P	Samtec
33	J11B	1	Bottom, 5x2x.1_SMT	SSW-105-22-F-D-VS-K	Samtec
34	S1	1	Switch Slide Ultra Mini DPDT Top ACT	SS22SDP2	NKK Switches of America
35	S2	1	Switch Slide DP3T PC MNT	EG2305	E-Switch
36	S3, S4	2	Switch Slide Ultra Mini SP3T TOP ACT	SS14MDP2	NKK Switches of America
37	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP11, TP12, TP13, TP14	11	Keystone Electronics, PCB Test Point, Miniature, Through-Hole, MINILOOP	5000	Keystone Electronics
38	TP6	1	Keystone Electronics, PCB Test Point, Multipurpose, Through-Hole, LARGELOOP	5011	Keystone Electronics
39	U1	1	Programmable Gain Amplifier, 24TSSOP	PGA280IPW	Texas Instruments
40	U2	1	ADC, 20TSSOP	ADS1259IPW	Texas Instruments
41	U11	1	TI REF5025 +2.5V precision voltage reference, 8-SOIC	REF5025ID	Texas Instruments
42	U31	1	2:1 multiplexer, SM8	SN74LVC2G157DCT	Texas Instruments
43	U32	1	Oscillator, 7.3728 MHZ 3.3V SMD, CTS_CB3LV	CB3LV-3I-7M3728	CTS - Frequency Controls
44	U34	1	EEPROM, 1.8V, 256K, 8TSSOP	24AA256-I/ST	Microchip Technology
Additional Components					
45	N/A	11	Shunt, 2-Position	SNT-100-BK-T	Samtec

11.2 PCB Layout

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS1259EVM PCBs.

Figure 40 through Figure 44 show the PCB layouts for the ADS1259EVM.

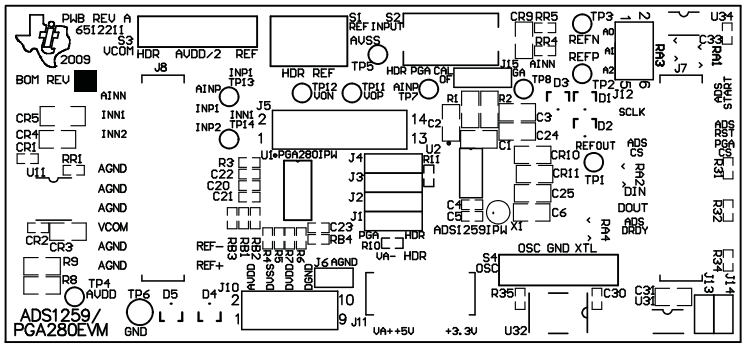


Figure 40. Top Silk Image

Top Layer 1

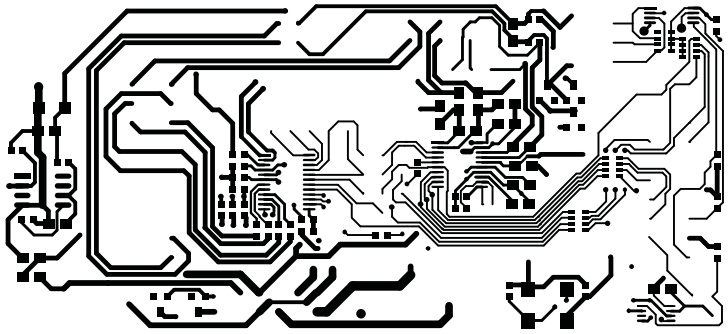


Figure 41. Top Side (Layer 1)

Mid Layer 2

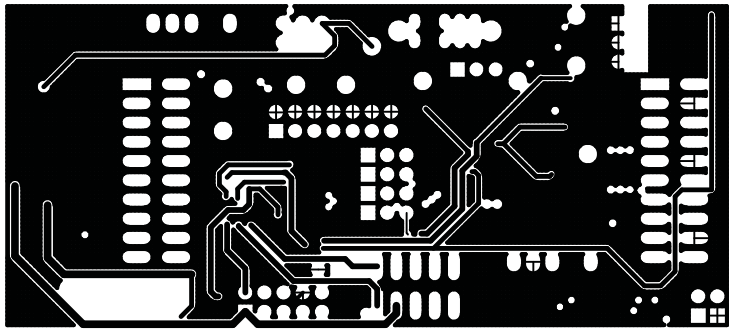


Figure 42. Internal Layer 1 (Layer 2)

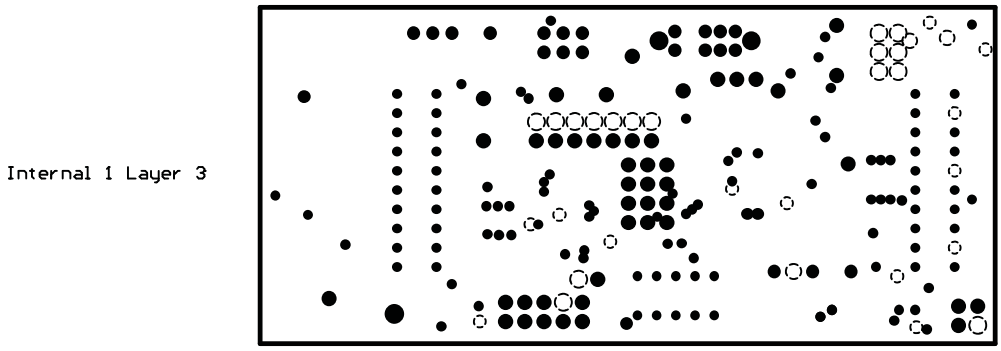


Figure 43. Internal Layer 2 (Layer 3)

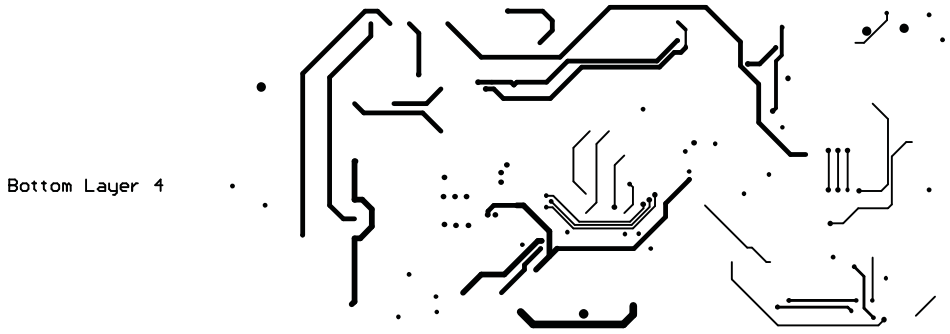
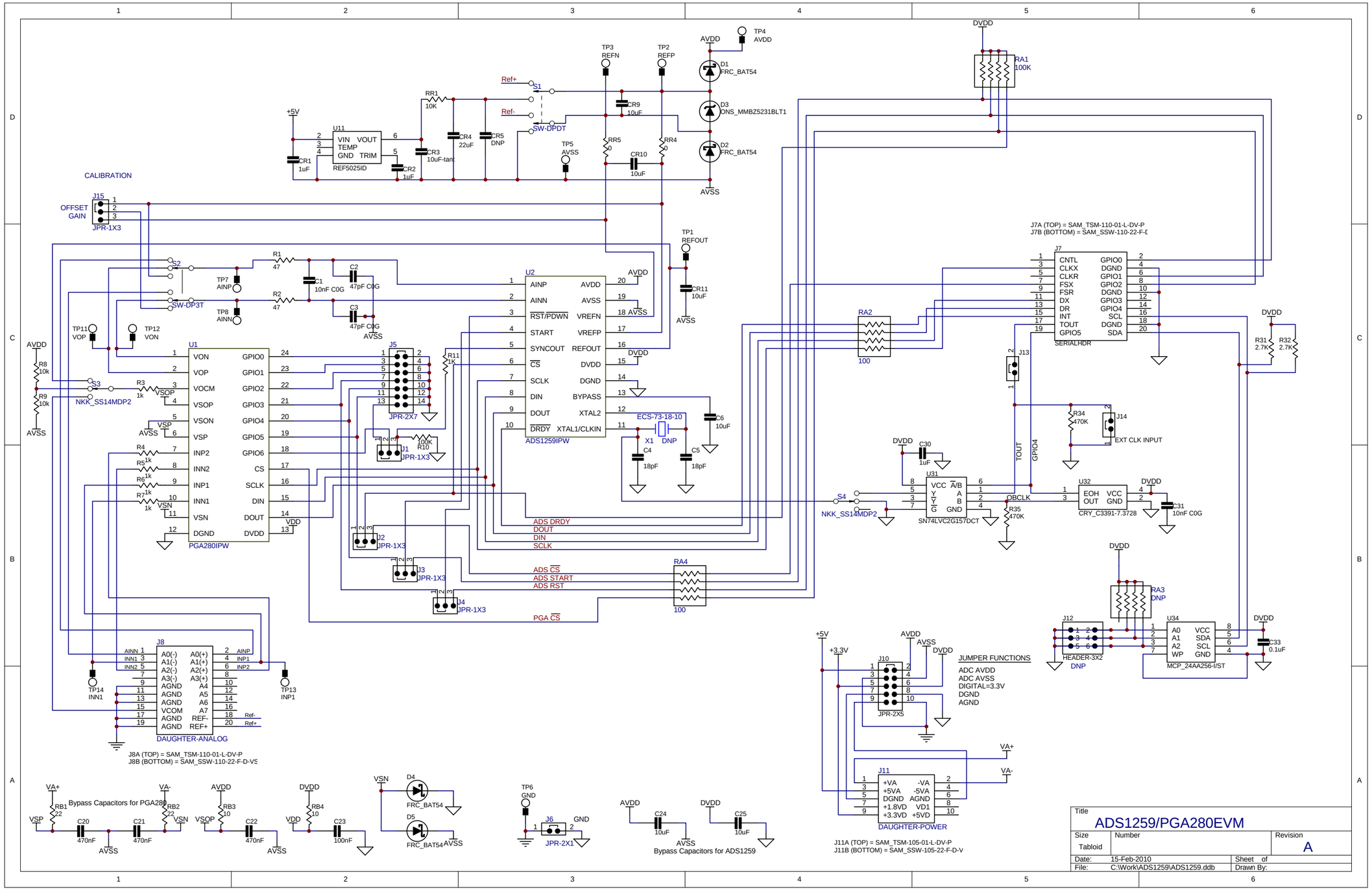


Figure 44. Bottom Side (Layer 4)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2011) to B Revision	Page
• Updated software download links and text in the *Installing the ADCPro Software* section.	12
• Added *External Wall-Adapter Power-Supply Requirements* section.	17


CALIBRATION
OFFSET
GAIN
J15
JPR-1X3
S2
SW-DP3T
S3
NKK_SS14MDP2
TP7
AINP
TP8
AINN
TP11
VOP
TP12
VON
R1
47
R2
47
C1
10nF C0G
C2
47pF C0G
C3
47pF C0G
AVDD
AVSS
U1
PGA280IPW
VON
VOP
VOCM
VSOP
VSON
VSP
INP2
INN2
INP1
INN1
VSN
DGND
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
CS
SCLK
DIN
DOUT
DVDD
VDD
R3
1k
R4
1k
R5
1k
R6
1k
R7
1k
R8
10k
R9
10k
VSP
VSN
J5
JPR-2X7
R11
1K
J1
JPR-1X3
R10
100K
J2
JPR-1X3
J3
JPR-1X3
J4
JPR-1X3
ADS DRDY
DOUT
DIN
SCLK
ADS CS
ADS START
ADS RST
PGA CS
U2
ADS1259IPW
AINP
AINN
RST/PDWN
START
SYNCOUT
CS
SCLK
DIN
DOUT
DRDY
AVDD
AVSS
VREFN
VREFP
REFOUT
DVDD
DGND
BYPASS
XTAL2
XTAL1/CLKIN
ECS-73-18-10
X1
DNP
C4
18pF
C5
18pF
C6
10uF
TP3
REFN
TP2
REFP
TP4
AVDD
TP5
AVSS
TP1
REFOUT
CR11
10uF
Ref+
Ref-
S1
SW-DPDT
RR1
10K
CR9
10uF
RR5
0
RR4
0
CR10
10uF
D1
FRC_BAT54
D3
ONS_MMBZ5231BLT1
D2
FRC_BAT54
+5V
U11
REF5025ID
VIN
TEMP
GND
VOUT
TRIM
CR1
1uF
CR2
1uF
CR3
10uF-tant
CR4
22uF
CR5
DNP
RA4
100
TP14
INN1
TP13
INP1
J8
DAUGHTER-ANALOG
A0(-)
A1(-)
A2(-)
A3(-)
AGND
VCOM
A0(+)
A1(+)
A2(+)
A3(+)
A4
A5
A6
A7
REF-
REF+
J8A (TOP) = SAM_TSM-110-01-L-DV-P
J8B (BOTTOM) = SAM_SSW-110-22-F-D-VS
VA+
VA-
RB1
22
RB2
22
C20
470nF
C21
470nF
Bypass Capacitors for PGA280
RB3
10
C22
470nF
RB4
10
C23
100nF
D4
FRC_BAT54
D5
FRC_BAT54
TP6
GND
J6
JPR-2X1
C24
10uF
C25
10uF
Bypass Capacitors for ADS1259
DVDD
RA1
100K
RA2
100
J7A (TOP) = SAM_TSM-110-01-L-DV-P
J7B (BOTTOM) = SAM_SSW-110-22-F-D
J7
SERIALHDR
CNTL
CLKX
CLKR
FSX
FSR
DX
DR
INT
TOUT
GPIO5
GPIO0
DGND
GPIO1
GPIO2
DGND
GPIO3
GPIO4
SCL
DGND
SDA
J13
R34
470K
J14
EXT CLK INPUT
C30
1uF
U31
SN74LVC2G157DCT
S4
NKK_SS14MDP2
OBCLK
R35
470K
U32
CRY_C3391-7.3728
EOH
OUT
VCC
GND
C31
10nF C0G
R31
2.7K
R32
2.7K
RA3
DNP
J12
HEADER-3X2
DNP
U34
MCP_24AA256-I/ST
A0
A1
A2
WP
SDA
SCL
C33
0.1uF
+5V
+3.3V
J10
JPR-2X5
JUMPER FUNCTIONS
ADC AVDD
ADC AVSS
DIGITAL=3.3V
DGND
AGND
J11
DAUGHTER-POWER
+VA
+5VA
DGND
+1.8VD
+3.3VD
-VA
-5VA
AGND
VD1
+5VD
VA+
VA-
J11A (TOP) = SAM_TSM-105-01-L-DV-P
J11B (BOTTOM) = SAM_SSW-105-22-F-D-V
Title
ADS1259/PGA280EVM
Size
Tabloid
Number
Revision
A
Date:
15-Feb-2010
Sheet of
File:
C:\Work\ADS1259\ADS1259.ddb
Drawn By:

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
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東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

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