Technical White Paper

Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors

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ABSTRACT

In this paper we provide a comprehensive analysis and new mathematical foundation to design any number of parallel LDO's using ballast resistors. Using this foundation, we show how to optimize the parallel LDO performance by including the parasitic PCB impedance in the ballast resistance analysis. This enables lower values of discrete ballast resistance and maximum performance in the design.

Table of Contents

Trademarks

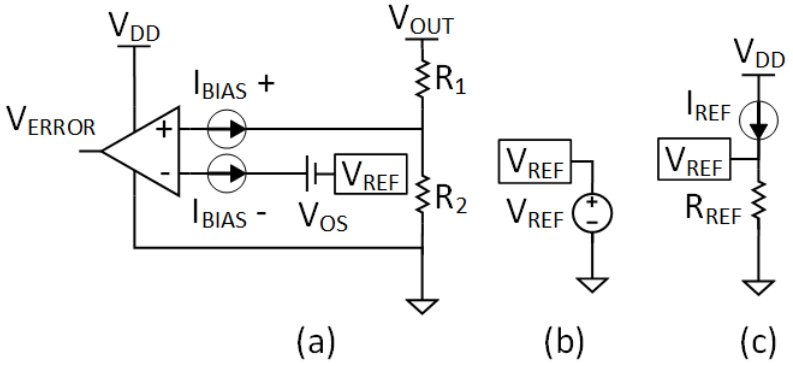
1 Introduction

Paralleling LDO's using ballast resistors have been discussed in the industry for many years. Previously, the analysis techniques that had been developed were limited to two parallel LDO's and did not take into consideration nonideal parasitic effects such as PCB impedance. Design and analysis of ballast resistance has not previously been fully explored, forcing the practicing engineer to use look up tables or common values such as 20 mΩ seen in many reference designs. Unfortunately, these look up tables give no methods to calculate how these ballast resistance values impact the load voltage and could be overdesigned leading to degraded performance.

Modern systems require parallel LDO designs to meet more than just additional load current or spread the heat generated by the power dissipation of the LDOs. Methods to accurately design with more than two parallel LDO's needed to be developed as many engineers want to use 5-10 parallel LDO's to meet their load current requirements. The voltage at the load must be calculated to ensure it meets the system requirement. This technical white paper provides a new mathematical foundation to calculate the load current and load voltage for any number of parallel LDOs. From this, we can support a new generation of designs which may parallel any number of LDO's to meet the system load voltage and load current while optimizing the ballast resistance to include the parasitic PCB impedance for maximum performance.

2 Comprehensive Review of Error in LDO's

In a typical LDO, the voltage feedback amplifier (error amplifier) compares the sensed output voltage to the reference voltage and adjusts the feedback loop accordingly (Figure 2-1). The nonideal components of the error amplifier include the offset voltage (V_{OS}) and bias currents (I_{BIAS}). In an ideal LDO, there are no sources of error and the output voltage is configured using V_{REF}, R_1 and R_2.



(a) Basic structure including nonideal bias current and offset voltage of op-amps. (b) Reference voltage generated via a precision voltage. (c) Reference voltage generated via a precision current source and resistor.

Figure 2-1. Feedback and Error Amplifier of LDO's

$$V_{OUT\_IDEAL} = V_{REF}\left(\frac{R_1 + R_2}{R_2}\right) \quad (1)$$

The output voltage error sources include the reference voltage, error amplifier, feedback resistors, and pass element. Other sources of error on the output voltage include load regulation and line regulation. An LDOs line and load regulation measure how the voltage reference, error amplifier and pass element react to changes in line voltage and load current, respectively.

The source of load regulation inside an LDO is concentrated around the error amplifier and pass element. The reference voltage is minimally affected, if at all, to changes in load current. In contrast, the reference voltage, the error amplifier and pass fet are all affected by changes in line, which combined make up the line regulation of an LDO. Thus, the reference voltage can be thought of as dependent on the line voltage, while the offset voltage can be thought of as dependent on both the line voltage and load current.

We can write an equation to describe the error, V_E, on the output (Equation 2). The bias current flows into the resistor R_{FBx}. If I_{BIAS+} is flowing into the error amplifier input, $R_{FBx} = R_1$ and the term $I_{BIAS}R_{FBx}$ is positive. If I_{BIAS+} is flowing out of the error amplifier input, $R_{FBx} = R_2$ and the term $I_{BIAS}R_{FBx}$ is negative.

$$\Delta V_E = \left((\Delta V_{REF} + \Delta V_{OS}) \left(\frac{\Delta R_1 + \Delta R_2}{\Delta R_2} \right) - V_{OUT\_IDEAL} \right) + \Delta I_{BIAS} \Delta R_{FBx} \quad (2)$$

A special use case exists such that the feedback resistors are removed and the feedback pin is directly tied to V_{OUT}. In this case, Equation 2 can be modified to become Equation 3.

$$\Delta V_E = \Delta V_{REF} + \Delta V_{OS} \quad (3)$$

2.1 Commentary on Real World Error Voltage (V_E) in Single LDO's

The equations describing V_E can be simplified in most cases for real world LDO's based on what nodes are accessible to the designer. We will identify these error terms in modern data sheets and later discuss their impact on current sharing in parallel LDO's.

In the simplest design scenario, the LDO contains all of the Figure 2-1(a) elements inside the integrated circuit (with either Figure 2-1(b) or Figure 2-1(c) generating the voltage reference) and the only terminals accessible to the designer are V_{IN}, V_{OUT} and return (or ground). The data sheet will provide an output accuracy specification which can be used as V_E for the parallel converter.

In the most complex design scenario, the LDO is designed from discrete components. Here, the V_{OS} and I_{BIAS} terms must be known and will be located in the discrete op-amp's data sheet. Most designs will be somewhere in between these extreme cases, thus guidance for most designs can be generalized based on which node the designer has access to – the V_{REF} pin and / or the V_{FB} pin.

2.1.1 V_{REF} Pin

While the reference voltage is most often derived from a precision voltage source V_{REF}, in some voltage regulators, a precision current source I_{REF} flows into a resistor to set the V_{REF} voltage (Figure 2-1(c)). In converters where I_{REF} and / or V_{REF} is internal to the device, I_{BIAS} is included in the tolerance of I_{REF}, and V_{OS} is included in the tolerance of V_{REF}.

If the V_{REF} pin is accessible to the designer with the intent that V_{REF} is generated externally, V_{OS} of the internal error amplifier must be known and may be located in the LDO data sheet. Although the term (ΔV_{REF} + ΔV_{OS}) is rarely included in LDO's, when external resistors are used to program V_{OUT} this information is needed to complete (Equation 2). Texas Instruments has developed a new down-loadable software tool with this information included for some of our LDOs see reference [7]. In the event that a TI LDO does not have this information in the data sheet or the software tool, submit a request for the information on our E2E forum.

2.1.2 V_{FB} Pin

When the V_{FB} pin is accessible to the designer, the I_{BIAS} term is required only in designs where the error amplifier does not operate in unity gain. The I_{BIAS} term is located in the data sheet and is sometimes described as the adjust pin current, set pin current or the feedback pin current. In non-unity gain designs (where external resistors are used to program V_{OUT}), we must first identify the (ΔV_{REF} + ΔV_{OS}) term in (Equation 2) as discussed in Section 2.1.1. Then we must conduct a statistical analysis on Equation 2 to derive ΔV_E see reference [4].

3 Current Sharing and Load Voltage Analysis for *n* Parallel LDO's

A model of the parallel LDO's can be developed, and used to provide a universal equation for current sharing in *n* parallel converters (Figure 3-1). Using mesh current analysis, we can derive the output current for any *n* number of parallel LDO's:

$$I_{OUTn} = \frac{V_{OUTn} - V_{LOAD}}{R_{Bn}} + \frac{V_{En}}{R_{Bn}} \quad (4)$$

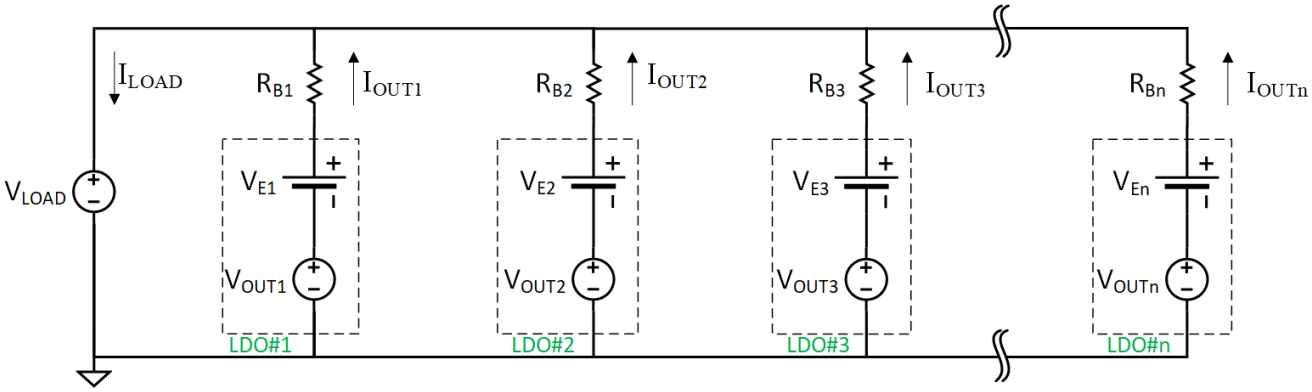


Figure 3-1. Equivalent Model for n Parallel LDO's Using Ballast Resistors.

The total load current is equal to the summation of current provided by each individual LDO. Thus:

$$I_{LOAD} = \sum_{n=1}^{n} \frac{V_{OUTn} - V_{LOAD} + V_{En}}{R_{Bn}} \quad (5)$$

In addition to deriving the current sharing of each LDO, we wish to compute the voltage on the load. Equation 5 can be rearranged to calculate V_{LOAD}.

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{Bn}}} \quad (6)$$

The universal equations for the current sharing and load voltage analysis are summarized in Equation 4, Equation 5 and Equation 6 for any *n* number of parallel LDO's using ballast resistors.

Equation 5 can be used to determine the maximum current provided by any LDO in a parallel system. This occurs when the error term for one LDO is the most positive while the error terms for the other LDO's are the most negative. In this worst-case scenario, I_{OUTn} raises to its maximum possible value using Equation 4. This analysis provides the maximum current that each LDO must be designed to, and should be used in power dissipation analysis and thermal analysis for the parallel LDO's.

3.1 Commentary on Parallel LDO's in Real World Applications

Upon review of Equation 4 and Equation 5, there are no theoretical limitations on the number of LDO's that can be paralleled. Also, there is no assumption that all of the LDO's or output voltages must be the same. To simplify implementation, it may be advantageous to reduce variability by selecting the same LDO with the same nominal output voltage. The worst-case current sharing of each LDO can be obtained and is a function of the error voltage and ballast resistance chosen. As discussed in Section 2, the sources of variability for single LDO's are located on the V_{REF} node and V_{FB} node.

When the designer has access to the V_{REF} node, they can short all V_{REF} nodes together, providing an identical reference voltage for each device. The reference voltage is typically the dominant source of variability in steady state analysis, so connecting the reference voltage nodes together can make a significant improvement in the current sharing of each parallel LDO. With the references shorted we can simplify Equation 7 and Equation 8 for our current sharing analysis.

$$\Delta V_E = \left((V_{REF} + \Delta V_{OS})\left(\frac{\Delta R_1 + \Delta R_2}{\Delta R_2}\right) - V_{OUT\_IDEAL}\right) + \Delta I_{BIAS}\Delta R_{FBx} \quad (7)$$

$$\Delta V_E = \Delta V_{OS} \quad (8)$$

The feedback for each LDO must be before the ballast resistors and not directly on the load voltage V_{LOAD}. Thus, we cannot tie the V_{FB} nodes together to eliminate its contribution to V_E. When selecting parallel LDO's without unity gain feedback, it is desired to minimize ΔI_{BIAS} (listed in the LDO data sheet) or its effects on accuracy by choosing the proper feedback resistance.

4 Ballast Resistor Design and Analysis

4.1 Selecting the Ballast Resistor Value

A ballast resistor is an electrical component used to prevent current faults in a system. For parallel LDO designs it is placed between separate LDO outputs, and also between the LDO output and the load. This limits the current that a single LDO can provide to the load.

Equation 4 and Equation 5 have too many unknowns to be uniquely solvable. For simplicity, engineers will typically set V_{OUT} of each converter to be the same. Similarly all ballast resistors will be set to the same value. As shown in Equation 4 the remaining unique contributor to I_{OUTn} is V_{En}.

Traditionally the ballast resistance was chosen using Equation 9 to set the current imbalance I_{MAX} of the parallel LDO's. This formula ensures that the LDOs do not go into current limit but does not account for the required load voltage, V_{LOAD}, which is also a requirement for most modern power supplies designed with parallel LDO's. A down-loadable software tool has been developed to design R_B for commonly used LDO's given a set of system requirements (see references 6 and 7).

Use either Equation 9 or the software tool to calculate the ballast resistor. Then using Equation 4, Equation 5, and Equation 9 we can solve for I_{OUTn} in Equation 10. Calculate I_{OUTn} in accordance with Current Sharing and Load Voltage Analysis for *n* Parallel LDO's to verify that no LDO enters current limit after accounting for component tolerance. Use Equation 10 in designs with identical V_{OUT} and R_B values for each LDO, otherwise use Equation 4.

$$R_B = \frac{\underset{1<x<n}{max} V_{En} - \underset{1<x<n}{min} V_{En}}{\Delta I_{MAX}} \quad (9)$$

$$I_{OUTn} = \frac{I_{LOAD} - \left(\sum_{n=1}^{n} \frac{V_{En}}{R_B}\right)}{n} + \frac{V_{En}}{R_B} \quad (10)$$

4.2 PCB Ballast Resistor Design vs. Discrete Ballast Resistance

A ballast resistor can be a discrete component or the parasitic resistance of a PCB trace could be used when the ballast resistance is very small see reference [1]. In general, PCB trace resistors favor applications which are low cost and which operate in a narrow temperature range or experience very high temperatures. Discrete resistors favor applications which require maximum performance (where output voltage tolerance and transient responses are critical). Designing with a discrete ballast resistor becomes challenging when ambient temperatures exceed 125°C.

Formulas are provided in see reference [1] to determine the cross section in square mils and the PCB trace length. Here, *I* is the current in amperes, *A* is the cross section in square mils, ΔT is the change in temperature in Celsius, *k* is a constant such that it is 0.048 for outer layers or 0.024 for inner layers, *l* is the length of the trace, *R* is the resistance in ohms, α is the temperature coefficient of copper (3.9 x 10-3 (°C-1)), T_A is the ambient temperature, and *p* is the resistivity of copper (1.74 x 10-8 (Ω·m)). The cross-sectional area *A* is a function of copper trace height (or copper weight) and copper trace width.

$$A = \sqrt[0.725]{\frac{I}{k\Delta T^{0.44}}} \quad (11)$$

$$R = \frac{l \times \rho \times (1 + \alpha \times (T_A - 25°C))}{A} \quad (12)$$

$$l = \frac{R \times A}{\rho \times (1 + \alpha \times (T_A - 25°C))} \quad (13)$$

When designing a PCB trace resistor, limit ΔT to the maximum rise above the board temperature that the PCB can withstand. For instance, when the board material is FR4, the glass transition temperature T_G is 135°C for standard FR4 and at least 175°C for high T_G FR4. The board temperature as seen by the PCB ballast resistor should consider any thermal spreading of heat generated by the voltage regulator or surrounding circuitry. Thus, setting ΔT to 20°C is a common value where the LDO's can reach a junction temperature of 150°C and high T_G FR4 is used. Thus, setting ΔT to 20°C is a common value where the LDO's can reach a junction temperature of 150°C and high T_G FR4 is used.

Calculate Equation 11 from the allowable temperature rise, then determine the length of the PCB trace resistor from Equation 12 and the desired PCB trace resistance. The trace length should always be calculated at the coldest temperature the trace will experience as this provides the lowest ballast resistance (Figure 4-1). Once the PCB trace length is obtained, use Equation 13 to obtain the PCB trace resistance at the maximum operating temperature of the PCB trace. Thus, the minimum and maximum PCB trace resistance is now known. The parallel voltage regulator design must then be reviewed for both values of ballast resistance. Use Equation 4 or Equation 9 to ensure I_{OUTn} does not exceed the LDO internal current limit, and Equation 6 to assess for regulation band compliance. If the PCB trace resistance does not meet the system requirements a discrete ballast resistor can be used since they tend to vary much less across temperature (Figure 4-1).

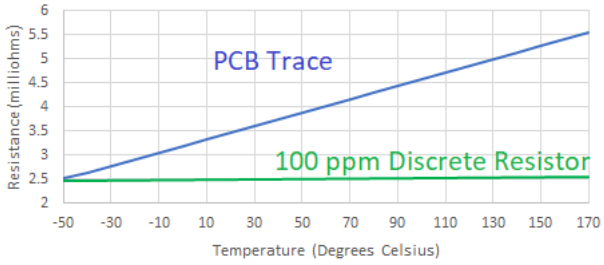


Figure 4-1. Tolerance Comparison of PCB Trace and a 100 ppm Discrete Resistor Over Temperature

Figure 4-2 compares discrete versus PCB trace ballast resistor techniques to show that as current increases, the PCB trace length is much larger than comparable discrete resistors. Parasitic inductance of the PCB trace may also hinder performance of the LDO during transient conditions.

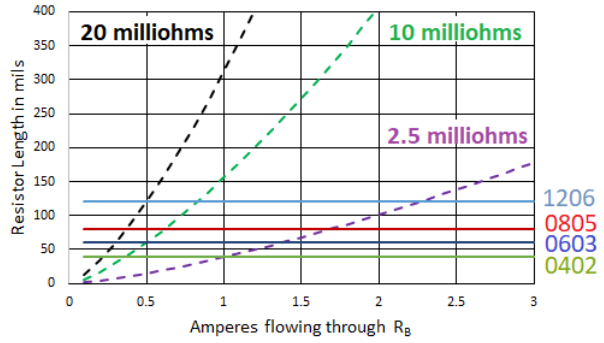


Figure 4-2. Length Comparison of PCB Trace Resistors (Dashed Lines) Versus Discrete Resistor Packages (Solid Lines) at Room Temperature for ΔT = 20°C

If a discrete resistor is chosen, the power derating curve must be reviewed if the resistor temperature exceeds 70°C (Figure 4-3). At high values of current, the power derating curve may push the resistor into a larger size package.

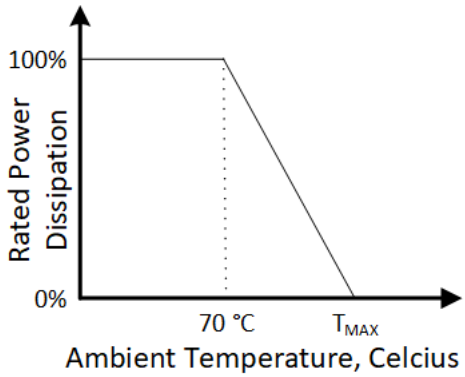


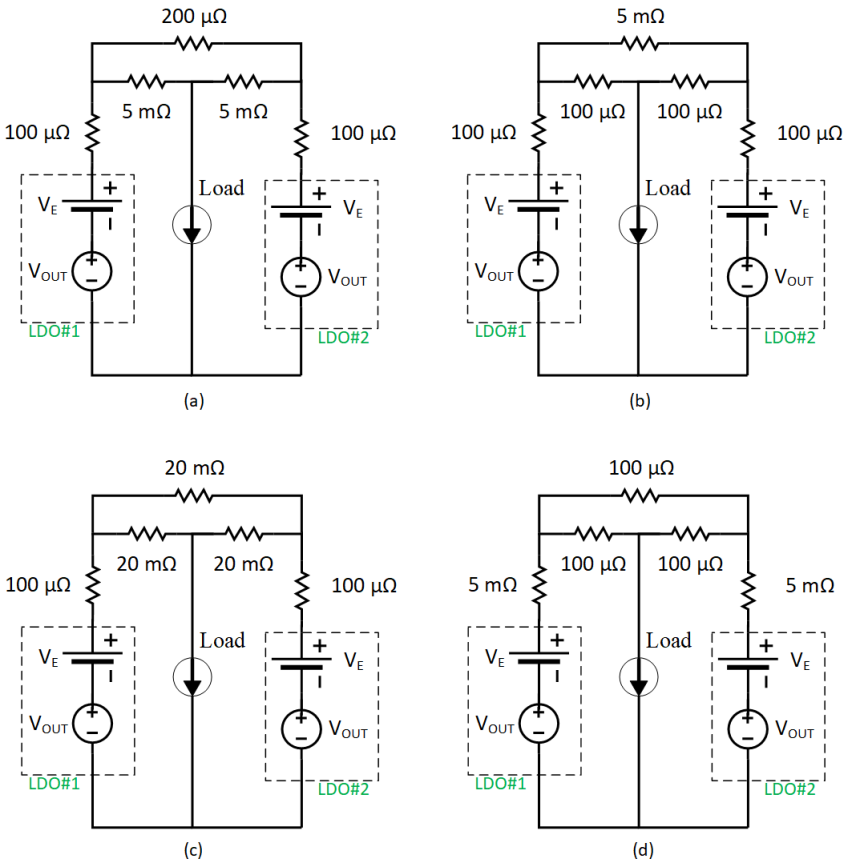
Figure 4-3. Typical Discrete Resistor Derating Curve Across Temperature

5 Impacts and Opportunities of PCB Parasitic Impedance

PCB parasitic impedance increases the effective ballast resistance. In designs with a large value discrete ballast resistor (such as greater than 50 mΩ), Equation 10 and Equation 6 provides good approximations of the load current and voltage. For small values of ballast resistance (such as less than 50 mΩ), the parasitic PCB impedance can impact the final current sharing analysis. To enable high performance use cases, R_B can be optimized by reviewing the PCB parasitic impedance and reducing the discrete ballast resistance for each LDO accordingly. A reduction of R_B will increase the current sharing mismatch between each LDO Equation 10 but will increase the load voltage Equation 6 which is usually a desired result.

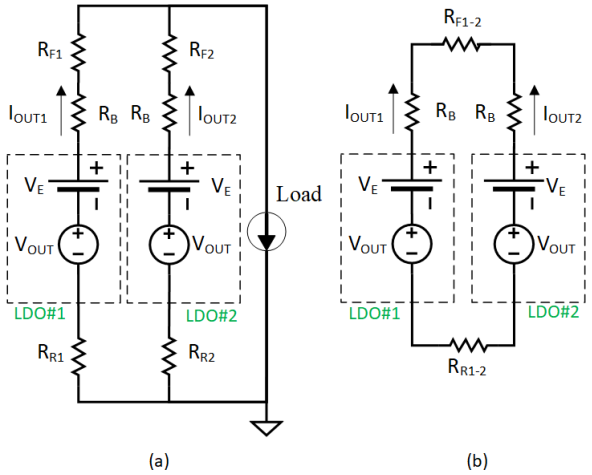
The interaction of the ballast resistance and PCB impedance is shown in Figure 5-1 assuming a minimum 5 mΩ ballast is needed. Here, we will limit the discussion to two parallel LDO's although we can extend this to any number of parallel LDO's. The PCB impedance is lumped into one equivalent resistor from each LDO to the load and also between the LDOs. Figure 5-1 then provides the four possible use cases of discrete ballast resistance and PCB impedance. Figure 5-1 (a) and Figure 5-1 (b) show insufficient ballast resistance between the LDOs or between the LDO and the load, which is incorrect and could lead to a current fault condition. Figure 5-1 (c) will current share but the load voltage specification may not be met due to the larger 20 m-ohm impedances. Figure 5-1 (d) is an example where the ballast resistance and PCB impedance has been optimized.

Thus, from Figure 5-1 (a) and (b) there are two sets of PCB impedance which must be reviewed in a system and are illustrated in Figure 5-2 for two parallel LDO's. From Figure 5-2a, R_{F1} and R_{F2} are the parasitic impedances from the output of each ballast resistor to the load, while R_{R1} and R_{R2} is the parasitic impedance from the load to the return pin of each LDO. From Figure 5-2b, R_{F1-2} is the parasitic impedance between the output side of the ballast resistors used for LDOs 1 and 2 and R_{R1-2} is the parasitic impedance between the LDO 1 and 2 return pins. Note that $R_{F1-2} \neq R_{F1} + R_{F2}$ and $R_{R1-2} \neq R_{R1} + R_{R2}$.



(a) The LDO outputs are connected before the ballast resistor (b) The load is connected before the ballast resistors. (c) The LDO's will current share but the load regulation may not meet the requirements. (d) Optimum configuration of ballast resistance and PCB impedance.

Figure 5-1. Nonideal PCB Impedance Examples



(a) Equivalent circuit from each voltage regulator to the load. (b) Equivalent circuit from one voltage regulator to another voltage regulator.

Figure 5-2. Impact of Nonideal PCB Impedance on Current Sharing of Two Parallel LDO's

The parasitic impedances R_{F1}, R_{F2}, R_{R1}, R_{R2}, R_{F1-2}, and R_{R1-2} can be simulated using a post route simulator, such as Altium PDN analysis. Note that when evaluating the parasitic return impedance, thermal pads should not be included in the post route simulation as the point of return for the simulated load. Thermal pads provide a low thermal resistance to dissipate heat, however they do not provide low electrical resistance from the die to ground. Thus, the simulation should be performed back to the ground pin of the LDO.

Upon review of Figure 5-2a, we wish to identify the minimum discrete ballast resistance $R_{Bn'}$ necessary to meet Equation 9 by accounting for R_{Fn} and R_{Rn}.

$$R_{Bn'} = \frac{\underset{1<x<n}{max} V_{En} - \underset{1<x<n}{min} V_{En}}{\Delta I_{MAX}} - \frac{1}{2}(R_{F1} + R_{F2} + R_{R1} + R_{R2}) \tag{14}$$

Upon review of Figure 5-2b, we wish to identify the minimum discrete ballast resistance $R_{B'}$ necessary to meet Equation 9 while accounting for R_{F1-2} and R_{R1-2}.

$$R_{B'} = \frac{\underset{1<x<n}{max} V_{En} - \underset{1<x<n}{min} V_{En}}{\Delta I_{MAX}} - \frac{1}{2}(R_{F1-2} + R_{R1-2}) \tag{15}$$

The new, optimized ballast resistor R_{B_OPT} chosen to account for the parasitic PCB impedance is the maximum value of $R_{Bn'}$ and $R_{B'}$ as shown in Equation 16. I_{OUTn} and V_{LOAD} can be modified as shown in Equation 17 and Equation 18, respectively. If both $R_{Bn'}$ and $R_{B'}$ provide negative values, then the PCB impedance is higher than the necessary ballast resistance for the desired worst-case current sharing. Thus, a discrete ballast resistor can be removed from the design as the parasitic impedances provide sufficient ballast resistance.

$$R_{B\_OPT} = \max(R_{Bn'}, R_{B'}, 0) \tag{16}$$

$$I_{OUTn} = \frac{I_{LOAD} - \left(\sum_{n=1}^{n} \frac{V_{En}}{R_{B\_OPT} + R_{Fn} + R_{Rn}}\right)}{n} + \frac{V_{En}}{R_{B\_OPT} + R_{Fn} + R_{Rn}} \tag{17}$$

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{B\_OPT} + R_{Fn} + R_{Rn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{B\_OPT} + R_{Fn} + R_{Rn}}} \tag{18}$$

If the voltage at the load must be increased, the PCB impedances can be reduced and / or V_{OUTn} can be increased to achieve a higher V_{LOAD}.

6 Design Examples

Two parallel LDO designs have been tested to validate the concepts developed in this white paper. The first LDO design uses three parallel TPS7A57 LDO's and the second LDO design uses three parallel TPS7A47xx LDO's.

6.1 TPS7A57

Three parallel TPS7A57 LDO's were configured for 0.75 VDC output voltage, supplying a combined 13.2 A load current, with a maximum current imbalance of 1 A (). The TPS7A57 reference voltage is generated using a precision current source and an external resistor see reference [2]. Thus, from Commentary on Parallel LDO's in Real World Applications we tie the individual reference voltage pins together to reduce the current sharing imbalance among the three LDO's. The remaining error voltage is a function of the line regulation, load regulation and offset voltage variation. Per the TPS7A57 data sheet, the line regulation is 10 nV/V, the load regulation is 175 µV/A and the offset voltage is ± 2 mV. The offset voltage dominates the total error voltage so we will set V_E = ± 2 mV in the analysis. From Equation 9, R_B = 4 mΩ. From Current Sharing and Load Voltage Analysis for *n* Parallel LDO's, the highest load current for one LDO is when V_E is positive for one and negative for the rest. From Equation 10 we conclude I_{OUT1} = 5.07 A and I_{OUT2} = I_{OUT3} = 4.07 A. We can determine the lowest load for an LDO by assuming one LDO has -V_E while the others have +V_E. From Equation 10 we conclude I_{OUT1} = 3.73 A and I_{OUT2} = I_{OUT3} = 4.73 A.

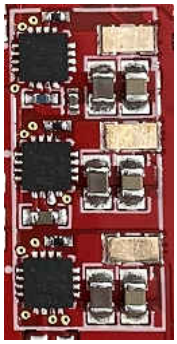


Figure 6-1. 3 Parallel TPS7A57 LDO's. The Parallel Circuitry is Boxed in White.

The parallel LDO's were implemented onto a PCB and a post route simulation was performed (Figure 6-2). The simulation assumed an ideal V_{OUT} = 0.75 V and R_B = 2.5 mΩ for each converter. The simulation results demonstrate the impact of PCB impedance mismatch from each LDO output to the load on the current sharing. Measurements versus simulation data in this configuration show strong correlation (Table 6-1) with the difference due to the slight variation of V_{OUT} and R_B in the fabricated design compared to the ideal values used in the simulation.

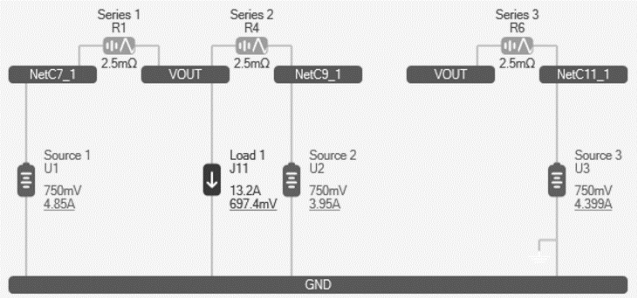


Figure 6-2. Post Route Simulation of the Parallel TPS7A57 Design

Table 6-1. Parallel TPS7A57 LDO Design Simulation vs. Measured Current

	PDN Simulation	Measurement	Error
I_{OUT1}	3.95 A	3.99 A	1%
I_{OUT2}	4.399 A	4.42 A	0.48%
I_{OUT3}	4.85 A	4.79 A	1.2%

6.2 TPS7A47xx

Three parallel TPS7A47 LDO's were configured for 12 VDC output voltage, supplying a combined 2.5 A load current, with a 60 mV maximum increase in load regulation (Figure 6-3). The TPS7A47 reference voltage is generated using a precision voltage source and is buffered with an internal unity gain amplifier see reference [3]. Thus, from Commentary on Parallel LDO's in Real World Applications we tie the individual reference voltage pins together to reduce the current sharing imbalance among the three LDO's. The remaining error voltage is a function of the line regulation, load regulation and offset voltage variation. For the TPS7A47, the offset voltage across line and load is ± 4 mV worst case. We will set V_E = ± 4 mV in the analysis and from see reference [6], R_B = 61 mΩ. From Current Sharing and Load Voltage Analysis for *n* Parallel LDO's, the highest load current for one LDO is when V_E is positive for one and negative for the rest. From Equation 10 we conclude I_{OUT1} = 928 mA and I_{OUT2} = I_{OUT3} = 797 mA. We can determine the lowest load for an LDO by assuming one LDO has -V_E while the others have +V_E. From Equation 10 we conclude I_{OUT1} = 753.5 mA and I_{OUT2} = I_{OUT3} = 885 mA.

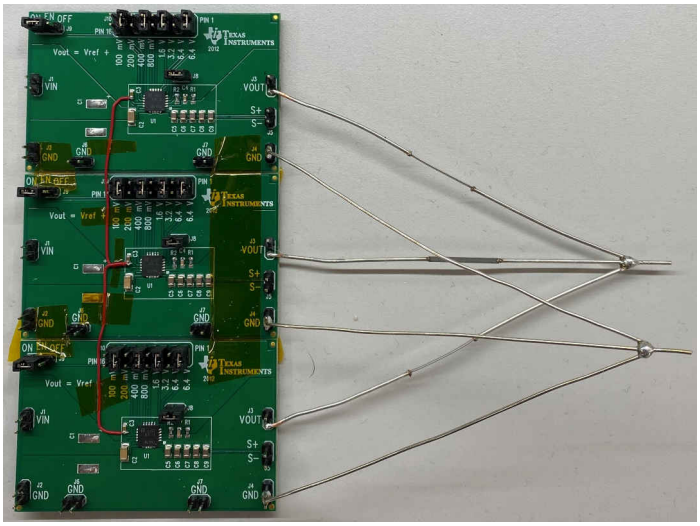


Figure 6-3. 3 Parallel TPS7A47 LDO's. Input Supplies and 2.5 A Load not Shown.

The parallel LDO's were implemented using EVM's and a post route simulation of the EVM identified 8.6 mΩ in the forward and return paths. Thus a 50 mΩ discrete ballast resistor was used for each LDO. Each output voltage was measured at V_{IN} = 15 V prior to connecting the EVM's together. Milliohm measurements were made of each ballast resistor (R4, R5 and R6) and the wire used to connect each EVM together (R7, R8 and R9), and these values were included in the spice simulation (Spice Simulation of the Parallel TPS7A47 LDOs.). Measurements versus simulation data in this configuration show strong correlation (Parallel TPS7A47xx LDO Design Simulation vs. Measured Current).

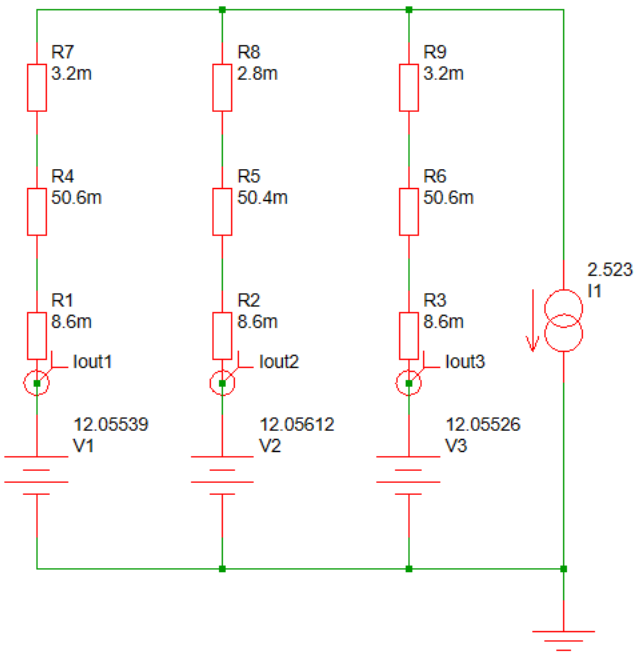


Figure 6-4. Spice Simulation of the Parallel TPS7A47 LDOs.

Table 6-2. Parallel TPS7A47xx LDO Design Simulation vs. Measured Current

	+/- 1 sigma Analysis, R_B = 61 mΩ	+/- 6 sigma Analysis, R_B = 61 mΩ	Spice Simulation	Measurement	Spice Simulation vs Measurement Error
I_{OUT1}	856 mA / 826 mA	928 mA / 753.5 mA	835 mA	835 mA	0%
I_{OUT2}	856 mA / 826 mA	928 mA / 753.5 mA	855 mA	853 mA	0.23%
I_{OUT3}	856 mA / 826 mA	928 mA / 753.5 mA	833 mA	835 mA	0.25%

7 Conclusion

A complete current sharing and load voltage analysis has been presented for parallel LDO's using ballast resistors. The equations developed for this analysis have no theoretical limitations on how many LDO's can be placed in parallel, enabling the user to decide what is feasible based on system requirements and components selection. A detailed discussion is provided on sources of error and how to minimize this error in the current sharing design. The salient features of current sharing in LDO's are provided by equations Equation 4, Equation 5 and Equation 6. When V_{OUT} and R_B are the same for each parallel voltage regulator, and R_B is large (typically at least 50 mΩ), the salient equations are modified to become Equation 6, Equation 9, and Equation 10. When V_{OUT} and R_B are the same for each parallel LDO, and when including the effects of parasitic PCB impedance, the analysis uses the modified equations Equation 14 through Equation 18.

An in-depth discussion on ballast resistor analysis and design was presented, including a methodical approach for PCB ballast resistor analysis and design. PCB ballast resistors are favored in applications with low cost, low current loading, or very high temperatures. Discrete ballast resistors are favored in applications requiring small form factor components for higher current loading. Discrete ballast resistors are also favored in applications with tight regulation bands or wide temperature operation.

System architecture development is addressed in reference [6] to provide the minimum number of parallel LDO's required to meet a list of system requirements. A down-loadable tool see reference [7] has been developed using worst case analysis to enable the user to quickly assess how many parallel LDO's are needed to meet their system requirements.

8 References

1. Generic Standard on Printed Board Design, IPC-2221B, 2012
2. Texas Instruments, *TPS7A57 5-A, Low-VIN (0.7 V), Low-Noise (2.1μV_{RMS}), High-Accuracy (1%), Ultra-Low Dropout (LDO) Voltage Regulator* data sheet
3. Texas Instruments, *TPS7A4701-EP 36-V, 1-A, 4 μV_{RMS}, RF LDO Voltage Regulator* data sheet
4. Texas Instruments, *AN-1378 Method for Calculating Output Voltage Tolerances in Adjustable Regulators* application note
5. Texas Instruments, Scalable, High-Current, Low-Noise Parallel LDO Reference Design
6. Texas Instruments, *Parallel LDO Architecture Design Using Ballast Resistors* white paper
7. Parallel Low-Dropout (LDO) Calculator

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