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LDO REGULATORS WITH PNP PASS ELEMENTS NEARLY OBSOLETED THE EARLY NPN LINEAR REGULATORS. CMOS TECHNOLOGY BROUGHT FURTHER GAINS VIA PMOS LDO REGULATORS. NOW, N-CHANNEL LDO DEVICES, WHICH USE BCDMOS TECHNOLOGY, OVERCOME THE PRIMARY LIMITATIONS OF EARLIER DEVICES.

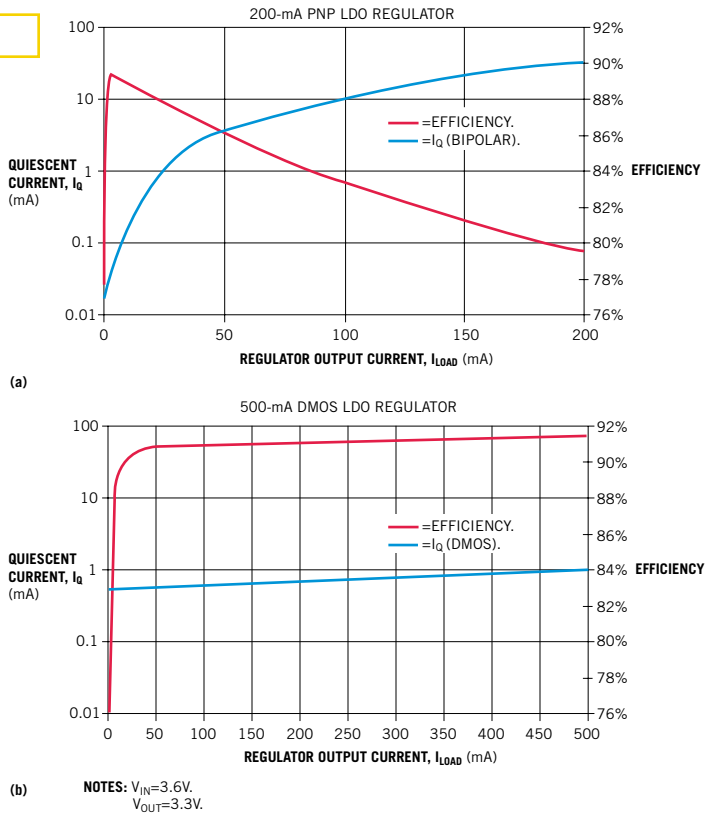
DMOS delivers dramatic performance gains to LDO regulators

THE HOT GROWTH IN PORTABLE applications has fueled the growth of the low-dropout (LDO)-regulator market and put extreme pressure on several key performance requirements, including low-dropout voltage, high efficiency (low ground-pin current), low-board-space usage, and stability. One of the most important LDO-regulator requirements is achieving lower dropout performance. When the market demanded that regulators waste less power, many systems went from pure linear regulation to two-stage regulation. The two-stage approach uses a highly efficient switch-mode converter followed by an LDO regulator, combining efficiency with low noise and fast transient response. Maximum efficiency requires the lowest possible voltage drop across the linear regulator, which results in even more pressure to reduce dropout voltage. Although the original conventional regulators had dropout voltages greater than 1V, the bar for newer LDO regulators is generally below 500 mV.

The requirement of high efficiency requires low quiescent, or ground-pin, current in the regulator. Ground-pin current represents waste current that the LDO regulator doesn't deliver to the load. Although many LDO-regulator vendors claim that their products have less-than-1-mA performance, most are far hungrier at their full-rated load or in dropout conditions. The performance target for new low-power LDO regulators has dropped to approximately 1 mA over full load and in dropout.

Standard LDO regulators typically require output capacitance of 2 to 10 µF. Although output capacitance does help transient response by providing in-

Figure 1



Even a so-called micropower regulator with a pnp pass element and a featured quiescent current of 20 µA can draw 30 mA, or 13% of its rated supply current, at its maximum rated load of 200 mA (a). A DMOS LDO regulator, the REG103, features a quiescent-current draw of 1 mA at the full-rated, 500-mA load (b).

stantaneous peak current, these capacitors have until now been necessary for a more fundamental reason: to keep the regulator stable. Unfortunately, the capacitor requirements are notoriously finicky, generally requiring a specified minimum and maximum capacitance as well as a minimum and maximum ESR to ensure stability. Therefore, LDO-regulator manufacturers have spent a great deal of effort attempting to develop a "capacitor-free" LDO regulator.

A process evolution has resulted in improved LDO performance. For example, the REG101/102/103 family of LDO regulators use a bipolar-CMOS-DMOS (BCDMOS) process and an n-channel double-diffused-MOS (DMOS) pass transistor in the emitter-follower configuration to achieve very low dropout and low ground-pin current while maintaining low noise and good transient performance. The topology of these regulators also eliminates the need for an output capacitor to maintain stability.

IN THE BEGINNING WAS THE NPN...

The first self-contained linear regulators of the early 1970s used npn pass elements. The pass element is the power device that the regulator uses to "pass" current from the input to the output. This type of regulator ruled the market for almost 15 years for many reasons.

One of the primary advantages of an npn pass device is a much higher current capability for a given die size or a much smaller die for a given current requirement. Because of the higher efficiency of silicon usage per unit area, npn elements are more cost-effective, especially for power applications. This advantage is due primarily to the carrier mobility of electrons, which is more than two times higher than the mobility of holes. An npn device usually has higher current gain, β; higher voltage gain, V_A; higher unity-gain bandwidth, f_T; and higher breakdown

ELIMINATE THE OUTPUT-CAPACITOR PROBLEM—AND THE OUTPUT CAPACITOR

One of the biggest drawbacks of pnp- and positive-channel-MOS (PMOS)-based regulators is their propensity to oscillate. These regulators not only require much larger values of output capacitance, but also are finicky about what type of output capacitor they have. Most manufacturers devote large sections of their data sheets to choosing an appropriate capacitor for a low-dropout (LDO) regulator. Application notes help you solve this common and vexing problem. The goal of most of these complicated maneuvers is getting a capacitor whose ESR falls neither too high nor too low to keep the regulator from oscillating. Often, the manufacturer specifies expensive or bulky output capacitors to target a precise combination of capacitance and ESR.

The basis of the problem is the gain configuration of the pass element itself. All pnp and PMOS LDO devices configure the pass element in the common-emitter, or common-source, configuration. This configuration has a high voltage gain of $A_V 5 g_m \cdot Z_D$, where g_m is the transconductance of the pass device, and Z_D is the impedance in the drain/collector leg. In an LDO regulator, Z_D is the load itself. Because load impedance varies widely from application to application and even over load changes in one application, most LDO-compensation schemes are critically load-dependent. The load forms both a pole and a zero that fall within the feedback loop, have low frequencies, and have inherently high variations.

All regulator-control loops contain a pole that the dominant pole of the error amplifier sets. The pass element itself introduces a second pole. And, if you use the pass element in a high-gain configuration, the load introduces a third pole. Because regulators operate at low gains, the load pole can introduce sufficient phase shift within the regulator's closed-loop response to make it unstable. (The specified output voltage is typically one to five times the bandgap-reference voltage for a gain of 0 to 14 dB.) Manufacturers are therefore forced to require complicated compensation schemes using pole-zero cancellation. The compensation circuits are notoriously fragile and susceptible to component variation.

Figure A illustrates the compensation nightmare of conventional P-type pass-element LDO regulators. LDO-regulator designers generally compensate the error amplifier to have a gain-bandwidth product of around 1 MHz, resulting in a well-controlled dominant pole of 100 Hz to 1 kHz, depending on the characteristics of the error amplifier. The impedance of the load determines the second pole, which occurs at $P_{LOAD} = 1/(2\pi \cdot R_{LOAD} \cdot C_{LOAD})$.

The example in **Figure A** assumes an R_{LOAD} of 33Ω (3.3V/100 mA) and a C_{LOAD} of 1 µF, resulting in a pole of approximately 5 kHz. This pole depends entirely on these two load parameters and varies in direct proportion to changes in either parameter. This result is startling and scary, implying that changes in load current, for example, modify the compensation loop.

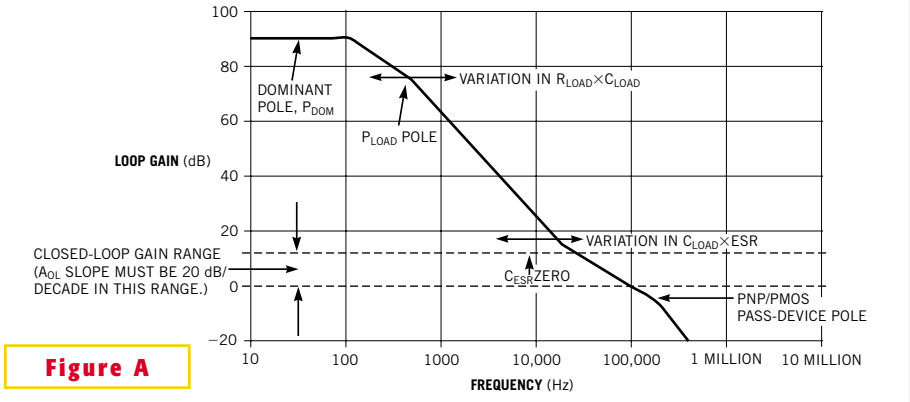


Figure A

The use of a pnp or PMOS pass element in the common-emitter/common-source configuration introduces an additional pole in the regulator's loop response and moves the zero down in frequency due to the loop gain.

voltage, $BV_{CEO,}$ than does a pnp device. These advantages carry over to MOS topologies, for which negative-channel MOS (NMOS) outperforms positive-channel MOS (PMOS).

A higher β makes the npn regulator's ground-pin current smaller than that of pnp regulators, given the same silicon area and thus the same cost. A more important advantage, however, is the configuration of the pass element in the regulator. An npn regulator configures the pass device as a high-side device with the emitter connected to the load. This configuration delivers the drive current, which is the base current of the pass element, to the load and doesn't flush the current down the ground pin, as is the case with a pnp pass element.

NPN REGULATORS ARE EASY TO COMPENSATE

One of the most significant advantages of the early npn linear regulators was their ease of use. They were easy to compensate; that is, they had a dominant-pole response, the load pole was not part of the regulator loop, and the size and ESR of the output capacitor was not critical. Therefore, designers could use just about any type or size of output capacitor or none at all. But smaller output capacitors were not a major issue during the early days of npn regulators because board space was much less constrained and battery/portable devices were nearly nonexistent. Therefore, this highly desirable feature took a back seat to the issue of low dropout.

The npn regulator may have continued to rule the market except for one major problem: high-dropout voltage. Most early npn regulators use the popular Darlington configuration for the pass element. Unfortunately, this configuration requires two V_{BE} drops between the input voltage (collector) and the output (emitter). When the input voltage drops below the required two V_{BE} drops, the Darling-

The pass device itself causes the next pole that sneaks into the loop. The unity-gain bandwidth of any power device is much lower than a smaller version of the same transistor due to the much higher parasitic capacitance and transit times inherent in larger devices. However, designers using p-type pass elements have to pay an additional high price, because the unity-gain bandwidth of pnp power elements is typically two to three times lower than that of npn elements. This example uses a typical pnp f_T of 400 kHz. This pole is also fairly easy to control.

The last major component of the LDO transfer equation is the zero introduced by the ESR of the output capacitor at a frequency given by: $Z_{ESR}=1/(2\pi \cdot ESR \cdot C_{LOAD})$.

Because a loop with three poles is an undesirable situation, this response zero is fortuitous and can help negate the effect of one of the low-frequency poles under certain conditions.

The requirement for the regulator to have sufficient phase margin to be unconditionally stable is as follows: The closed-loop gain line should intersect the open-loop response at a rate of closure of 20 dB/decade. Now, the picture becomes clear, and we can see the game the LDO-regulator user has to play to keep a p-type LDO device stable:

- The ESR must be high enough to lower the frequency of Z_{ESR} until it occurs at a gain above the closed-loop gain range. This method changes the open-loop 40- dB/decade slope to 20 dB/decade in the range where it will intersect the closed-loop gain.
- The ESR has to be low enough to keep the third pole from the pass device from rising above 0 dB, which would introduce enough phase shift to lead to oscillation.

Thus, the p-type-LDO-regulator user faces a tough challenge. The variation in both P_{LOAD} and Z_{ESR} makes the situation worse.

A transistor operating in the source/emitter "follower" configuration (the common drain/collector) has a voltage gain of approximately unity. Regulators that use a pass element configured as a follower can achieve a closed-loop frequency response that is nearly equal to f_T of the transistor itself. Now, you can set the dominant pole of the control loop so that the pass-element pole is below the closed-loop gain of the regulator (**Figure B**). This pole location makes the regulator unconditionally stable, and the value of C_{OUT} becomes nearly irrelevant. An additional side benefit is again due to the inherent superiority of n-type over p-type devices: Because the pole of the pass element limits the overall frequency response of the regulator-control loop, the natural higher frequency response of n-type devices allows superior transient response.

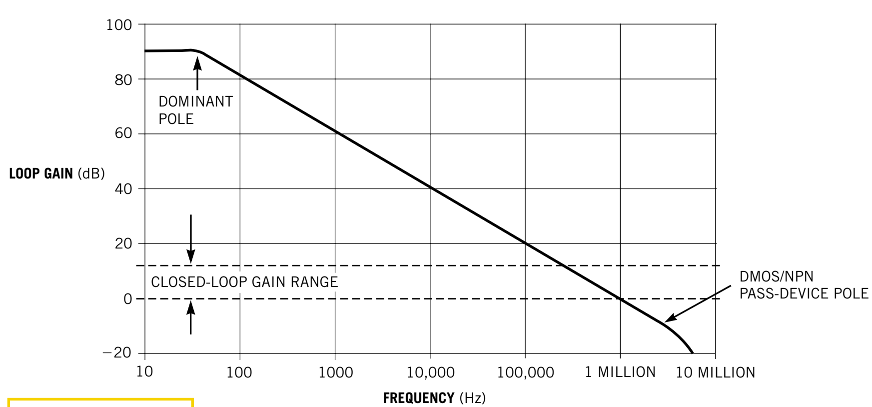
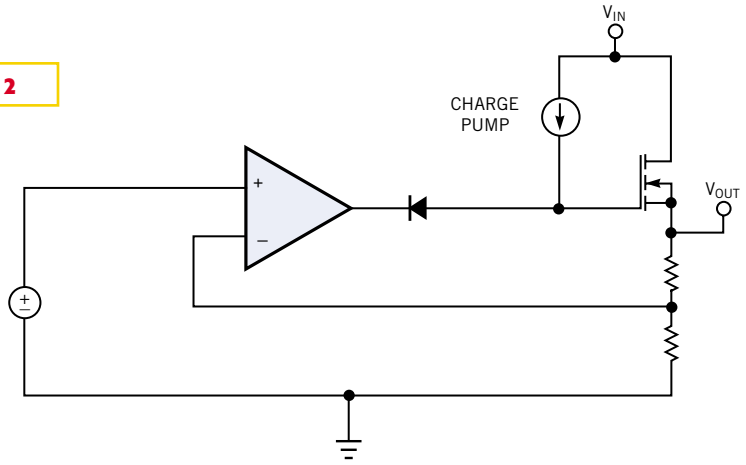


Figure B

Operating an n-type pass element in the emitter-follower/source-follower configuration results in a voltage gain of unity. Thus, the pole and zero from the load do not move down into the bandwidth of the control loop.

ton enters saturation, and the regulator rapidly loses the ability to regulate; in other words, it "drops out." Even with a so-called composite npn regulator, for which a pnp drives the npn base, dropout voltage approaches 1V. In the mid 1980s, this problem forced the development of low-dropout-voltage regulators.

Figure 2



A previous approach to driving an n-type-DMOS pass element uses a charge pump to directly drive the gate, which leads to high noise and limited positive slew rate.

THE BIRTH OF THE LDO REGULATOR

As the market demanded lower power consumption and as switching regulators appeared on the scene, a pressing need for lower dropout voltage resulted in the first LDO regulators. Additionally, a common use for linear regulators was in postregulation, which can suppress both switching noise and ESR transients. The common element of all early LDO regulators is a pnp pass element.

Early lateral-pnp regulators offered much worse performance than their vertical-npn brethren. However, they had one overriding advantage: You can connect them in the common-emitter (CE) configuration, which allows you to drive the pass element deep into saturation as the input voltage drops. Therefore, the dropout voltage is a function not of V_{BE}, as in npn regulators, but of the $V_{CE(SAT)}$ of the pnp, which is a much lower voltage. For early pnp regulators, dropout voltages of 500 to 800 mV were common. As linear processes became more sophisticated, vertical-pnp designs could stake out territory in the less-than-500-mV area, at least at light loads. Despite the many warts of pnp pass elements, pnp LDO regulators have maintained their hold on the regulator market because of this critical advantage over npn designs.

However, the disadvantages of pnp pass elements in LDO regulators' are significant. The poor frequency response of the pnp coupled with the CE configuration gives pnp LDO regulators a low-frequency pole in the regulators' control loop (see **sidebar** "Eliminate the output-capacitor problem—and the output capacitor"). Compensating for this second pole requires a large output capacitor with a specific ESR. For early, lateral-pnp-based regulators, a minimum C_{OUT} of 10 µF was common. Process improvements and the introduction of vertical power pnp structures have helped lower the minimum C_{OUT} to 1 to 2 µF. However, the "sweet spot" below 1 µF, where both capacitor case size and cost drop precipitously, is generally out of reach. Below the magic threshold of 1 µF, ceramic technology and multiple vendors drive a reduction in cost from 8 cents to 2 cents and in case size from EIA standard 3528 to 2012. The difference in case size means that switching from a 10- to a 1-µF ceramic capacitor reduces the pc-board area for the output capacitor by 75%. In addition, small capacitors provide insufficient peak currents to compensate for the pnp element's poor transient performance.

OUTPUT-CAPACITOR ESR

A transfer-function zero is necessary to offset the additional pole from the pnp, and the natural ESR of the output capacitor provides this zero. However, the ESR must fall within a carefully restricted range, or the LDO regulator will oscillate. Furthermore, the ESR must stay within the critical range over process and temperature variations. Capacitor manufacturers, which often list maximum ESR much higher than the actual typical value, further complicate the problem. The sensitivity of pnp LDO regulators to ESR and the high variability of ESR over temperature and frequency causes more regulators to oscillate than any other reason. A partial approach is to use bulky, more expensive tantalum capacitors to get the tolerance and ESR stability within range. The minimum ESR requirement naturally limits the transient performance of the regulator.

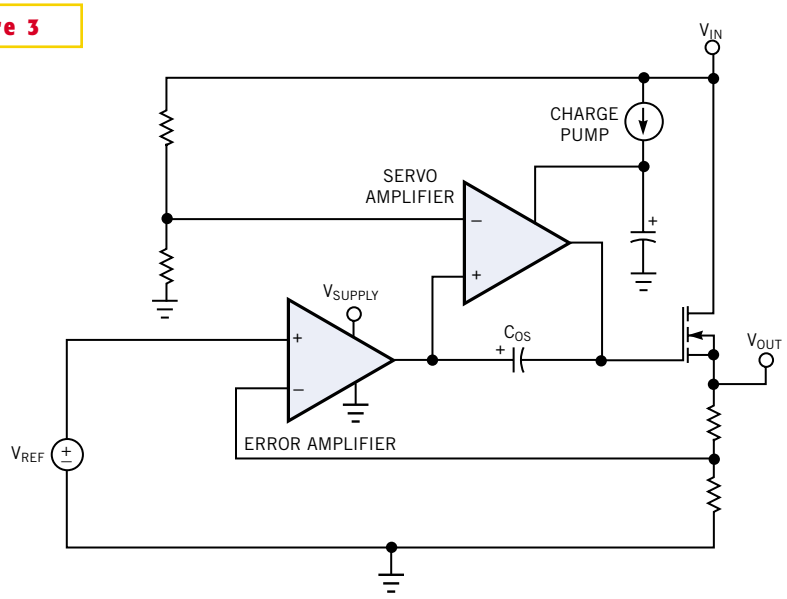
In pnp pass elements, the control current flows out the base of the transistor through the control circuit to ground, becoming part of ground-pin current, I_Q. This current is waste current and can become a significant portion of the insertion loss of an LDO regulator. The result is no small loss of efficiency. For a large power device, the current gain, β, of a standard bipolar process is often 20 to 50. Because β decreases as collector current increases above a certain level—fairly low for a pnp—the low β of the pass device further degrades, resulting in higher ground current. Process-technology improvements have improved current gain through innovations such as vertical-pnp structures (complementary-bipolar-process) and superbeta technology. However, operating (base) current is still a function of output current.

The situation worsens closer to dropout. When a bipolar transistor enters saturation, all of its performance characteristics, including β, rapidly degrade. As the regulator approaches its dropout voltage, that is as ΔV ($V_{IN}-V_{OUT}$) drops below approximately 500 mV, the pnp enters saturation. The ground-pin current can zoom from microamps to several milliamps or several percentage points of an LDO regulator's rated output current (**Figure 1a**).

Data sheets often bury the details of a pnp LDO regulator's insertion loss, and careful scrutiny is necessary to

gauge the true impact of this loss on the regulator's performance. For instance, data sheets often specify ground-pin current at low load currents or with input voltages significantly higher than the dropout voltage. This fact is the dirty little secret of pnp LDO regulators: Just when you most need to conserve battery power, their waste current is the highest.

Figure 3



A new topology uses a fast voltage-control amplifier to control the gate and a slow servo amplifier to maintain the proper offsetting voltage across a dc level-shift, or offsetting, capacitor, C_{OS}.

PMOS IMPROVES ON THE PNP

Low-cost CMOS foundries provided a new spin on the classical pnp device: PMOS LDO regulators. These devices use the pass element in the same gain configuration as does pnp LDO regulators but solves some of the more serious problems with pnp LDO designs. The most serious of these problems is quiescent current because of the increasing drive toward portability, battery operation, and "green" design. PMOS LDO devices solve the quiescent-current problems—a high I_Q that increases with increases in output current and with decreases in input voltage—of pnp LDO regulators. Because MOS devices are voltage-controlled, driving the pass device wastes no current, and the only ground-pin current that flows is the amount necessary to run the control circuit.

High-volume CMOS foundries have allowed manufacturers to offer PMOS LDO devices at more competitive prices than vertical-pnp based designs, which are generally higher mask-count processes. The advantages of PMOS do not come for free. Despite their cost advantage, PMOS designs still suffer from major drawbacks: They still require a large C_{OUT}, and the ESR of C_{OUT} must still fall within a critical range.

As with pnp devices, PMOS devices are also sensitive to the output capacitance for the same basic reasons. In addition, PMOS brings a new set of shortcomings to the LDO party, including a lack of drive voltage at low levels of V_{IN}, a restricted input-voltage range, and lower precision.

A PMOS LDO regulator controls the output current by pulling the gate below the source, which is the regulator's input. When an LDO regulator is in the "low-drop" region, the pass device is no longer pinched off and has entered its linear, or "triode," region. In this region, the amount of current that the device can deliver is directly proportional to the drive voltage, $V_{GS}-V_T$, or in the case of an LDO regulator, $V_{IN}-V_T$, where V_T is the MOS threshold, or turn-on, voltage. In addition, as V_{DS} decreases, an increasing drive voltage is necessary to keep the same output current. This situation forces the PMOS regulator into a corner. As input voltage drops, the control circuit forces the gate closer to ground, eventually running out of gas when the gate reaches ground. The device simply does not have the headroom to enhance the pass device, and the regulator loses regulation.

Although modern submicron CMOS processes can offer low on-resistance, both the MOS V_{DS} and the V_{GS} have limits of just a few volts. Therefore, CMOS regulators are generally limited to applications below 7V.

Another drawback is that regulators built on a CMOS process are generally less accurate than their bipolar counterparts, which is mostly due to the lower g_m of MOS devices. Most of the performance limitations arise in the error amplifier inside the control loop. MOS amplifiers have both higher V_{OS}, which makes it difficult to get high-output accuracy, and low gain, which makes it difficult to drive down the loop errors that line and load variation cause.

DMOS DEBUTS

Discrete DMOS has been around for 15 years and has been in volume production for more than a decade. The many strengths of this type of transistor have made it the power device of choice for applications in the 1 to 10A range, but new DMOS designs are pushing into the less-than-1A area.

The primary strength of DMOS is low $R_{DS(ON)}$, which in turn delivers very low-dropout performance. Currently, most DMOS devices are types of NMOS targeting low $R_{DS(ON)}$ in power applications. The DMOS structure uses a diffused junction rather than photolithography to form the MOS channel. This structure can be efficient and can result in extremely low $R_{DS(ON)}$. Modern discrete-DMOS processes can produce $R_{DS(ON)}$ levels that approach the theoretical limit of silicon. Of course, one of the most important requirements for an LDO regulator is low dropout. In the case of a MOS pass element, this requirement translates to low $R_{DS(ON)}$. Basically, the $R_{DS(ON)}$ of the DMOS becomes the V_{DO} of the LDO device, as long as the drive and control circuitry can maintain control

when the input voltage approaches the output.

Thus, the DMOS process shines for LDO designs, because it turns in the lowest dropout performance per unit area and drive voltage of any transistor available to regulator designers. This feature allows DMOS-based LDO regulators to potentially turn in dropout performance superior to the best pnp-based designs. DMOS also allows for high efficiency and low quiescent current of 1 mA or less (**Figure 1b**).

TABLE 1–LDO-REGULATOR-ELEMENT COMPARISON

Technology	Pass element	V_{DO}	Minimum C_{OUT}	Quiescent current	Precision
BCDMOS	N-DMOS	Very low	0	Low	Good to very good
CMOS	PMOS	Low	1 µF	Low	Fair
BiCMOS/CBC	Vertical pnp	Low	0.5 µF	High in dropout	Very good
Bipolar	Laternal pnp	Medium	2 µF	High in dropout	Good
Bipolar	npn	High	Unknown	Medium	Good

Another advantage of DMOS is that it has no restrictions on C_{OUT}; thus, you can entirely eliminate C_{OUT}. Using an N-type pass device in the follower configuration vastly simplifies compensation and results in a regulator that does not depend on the type and size of output capacitor for stability. DMOS also meets or beats the strengths of previous generations of pass elements. **Table 1** lists various characteristics and shows how the DMOS pass element compares with the pass elements in previous generations of linear regulators.

PROBLEMS WITH DMOS LDO REGULATORS

Two significant obstacles have prevented designers from using DMOS in highly integrated ICs: DMOS has been a large-pitch, discrete process, and the gate drive requires a high system voltage.

Most DMOS processes make ultralow-$R_{DS(ON)}$ vertical DMOS. Although these processes can make discrete-DMOS power transistors with $R_{DS(ON)}$ levels approaching the theoretical minimum, these processes are not suited for higher levels of integration. One reason is that the vertical-MOS action means that current flows from the top of the wafer to the bottom, which makes the back of the wafer a dedicated DMOS terminal. In addition, most of these processes have insufficient layers to generate other useful analog components and have a pitch too large to generate useful logic density.

In recent years, manufacturers have used older MOS fabs without submicron capability to produce ICs that integrate lateral DMOS with greater-than-1-µm CMOS. This use is good for facilities that would otherwise not compete with the large submicron-CMOS fabrication facilities, and it provides a good approach for inexpensively combining DMOS power devices with adequate control circuitry. However, this approach permits only low levels of integration.

The other barrier to using n-channel DMOS in LDO regulators is the requirement for a gate voltage of 1V or more above the source (the LDO output). This requirement implies that an n-channel DMOS LDO regulator either needs an extra supply voltage that is higher than the regulated voltage or needs an on-chip charge pump. Although many applications have additional system voltages higher than the desired regulated voltage, a regulator that required this additional voltage would be severely restricted in utility and in its range of useful applications.

Although manufacturers can theoretically add a charge pump to an LDO regulator to supply the drive voltage for the DMOS gate, practical implementations have come up woefully short. Problems include additional size, chip complexity, and noise. For instance, adding a charge pump to a chip using an older technology CMOS can add as much area as the DMOS device itself, partially offsetting the previously mentioned area gains. To be practical, a modern fine-lithography process is necessary to get the charge-pump CMOS logic small enough to be competitive.

Also, many ICs with an onboard charge pump that use DMOS in the high-side driver configuration—the configuration of an n-type DMOS pass element in a positive-output LDO regulator—use the charge pump to directly drive the gate. Unfortunately, this configuration leads to an extreme amount of switching noise on the output.

Using the charge pump to directly drive the gate also leads to another severe performance limitation: The ability of the charge pump to change the gate voltage limits the transient response of the regulator to load-current increases. Power pass elements are fairly large devices with large amounts of gate capacitance, and this approach therefore severely limits the transient response.

BCDMOS OPENS NEW OPTIONS FOR DMOS

The modern BCDMOS process gives power-IC designers a powerful tool kit for dealing with all of these problems. The BCDMOS process integrates bipolar, CMOS, and DMOS devices in a single fine-lithography process. State-of-the-art BCDMOS processes include precision- and power-bipolar transistors, analog CMOS, logic CMOS, and a range of DMOS power devices tailored for specific voltages. Mature, 1-µm BCDMOS processes are in volume production, and submicron BCDMOS is ramping up. Pushing into the submicron area for power devices may seem to have few benefits for analog and power components, but CMOS-logic density and $R_{DS(ON)}$ improve with finer lithography.

Using this process, designers can fit all of the logic, switches, and capacitors for a low-current charge pump into an area the size of one or two bond pads. This size removes one of the primary traditional obstacles to DMOS LDO regulators.

The $R_{DS(ON)}$ of DMOS devices on BCDMOS processes still does not rival that of discrete devices, but state-of-the-art BCDMOS processes can begin to offer integrated DMOS with $R_{DS(ON)}$ values as low as 60 $m\Omega/mm^2$. These values are not only far superior to those of PMOS, but also are available in a smorgasbord of voltage options, simultaneously allowing both low-dropout and high-input voltage.

Two of the primary determinates of the accuracy of an LDO regulator are the accuracy of its internal bandgap-voltage reference and the offset voltage of the

regulator's error amplifier, which compares the sampled output voltage to the reference voltage. A direct correlation exists between the precision of a bandgap reference and the process's ability to make a precision bipolar device. Using a bipolar input stage improves the V_{OS} of the error amplifier because the improved offset of a bipolar input and higher loop gain can reduce errors. Bipolar precision gives BCDMOS a large advantage over the high-volume, fine-geometry CMOS processes that manufacturers use to build PMOS regulators. These processes' bipolar capability is usually limited to diodes or committed-collector pnps.

REMOVING CHARGE-PUMP PROBLEMS

Even if an IC designer has access to a modern submicron process with integrated DMOS, the addition of a charge pump does not solve all of the design's problems. The amount of charge that the chip can store is limited, but driving the gate capacitance of a large DMOS device requires large currents during load transients. Thus, a large charge pump, which comes with concomitant switching noise, is necessary.

Figure 2 shows the most common topology of the few high-current DMOS regulators on the market. The two biggest problems with this topology are charge-pump noise, which usually translates directly to V_{OUT}, and a limited response to positive-load transients.

Charge pumps by nature tend to be noisy. Although clever design techniques can mitigate the amount of noise that a charge pump generates, most topologies for driving high-side DMOS use the large DMOS gate capacitance as part or all of the charge pump's output-storage capacitance. The few DMOS regulators that have appeared on the market rely on this technique of charging the gate capacitance directly from the charge pump. The problem with this approach is that directly pumping the gate translates the charge-pump noise to the output of the regulator with a gain of 1 because of the DMOS source-follower configuration. Also, to move the gate in response to a load change requires a large amount of charge during each cycle and thus a large charge pump, which makes the problem worse.

The gate capacitance, C_G, sets the amount of gate current, I_G, necessary to produce a change in gate voltage in a specified time, dV_G/dt; that is: $I_G = C_G \cdot dV_G/dt$, where C_G is total gate capacitance, primarily comprising C_{GS} and C_{GD}.

EVEN IF AN IC DESIGNER HAS ACCESS TO A MODERN SUBMICRON PROCESS WITH INTEGRATED DMOS, THE ADDITION OF A CHARGE PUMP DOES NOT SOLVE ALL OF THE DESIGN'S PROBLEMS.

Moving a DMOS gate with 100-pF gate capacitance by 5V in 0.5 µsec, which is a typical situation for a zero-output to full-scale-output current change, requires 1 mA of current. This amount is huge for an on-chip charge pump, and a charge pump beefy enough to supply 1 mA generates a large amount of noise. If you downsize the charge pump so that it can supply 10 µA, for example, a full-scale load change results in a severe loss of regulation. For several microseconds, the output voltage pulls down out of regulation by as much as several volts and requires more than 50 µsec to regain regulation. Because the regulator cannot supply this transient-load current, large amounts of output capacitance would still be necessary, which negates one of the prime advantages of DMOS.

OFFLOAD GATE DRIVE

The patent-pending topology of the REG101/102/103 family of LDO regulators use the error amplifier to drive the gate through a capacitor that serves as a dc-blocking, or offsetting, capacitor. A separate servo amplifier maintains the proper dc voltage across the offsetting capacitor (**Figure 3**).

In this topology, the error amplifier supplies the current necessary to move the gate through the offsetting capacitor, C_{OS}. Another way to view this action is to look at the error amplifier as a voltage-control amplifier and at C_{OS} as a charge storage/delivery device. The introduction of C_{OS} allows the amplifier to operate from a different voltage source from the one that the charge pump operates from, which further reduces the charge pump's output-current requirements. The new source is generally V_{IN} or a subregulated voltage. Now the charge pump services only the servoamplifier.

The servoamplifier's function is to keep the control-amplifier loop happy. That is, after a major load transition occurs, the control amplifier moves the gate to its new voltage but may have to move its output voltage to one of its supply rails. The servoamplifier slowly restores the control amplifier to the middle of its operating range by increasing or decreasing gate charge. The servoamp changes the gate charge by injecting or removing a small current at the node between C_{OS} and the DMOS gate. The servoamp causes loop-voltage changes that are orders of magnitude slower than changes in the primary loop, so the servoamp does not disrupt loop stability.

Because the servoamp is now the only load on the charge pump, the charge pump can be small, which translates directly to its being quieter. The amount of charge that transfers in each cycle using this topology is nearly two orders of magnitude lower than that of the traditional approach. Also, the power-supply rejection ratio of the servoamplifier rejects all remaining charge-pump-generated noise. The combination of smaller charge-pump current and servoamp power-supply rejection ratio knocks the noise down by nearly two orders of magnitude. Using good layout techniques, you can make the charge-pump noise at the regulator's output lower than the amount of noise that a good, low-noise bandgap reference generates.□

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