General Guideline: CDC7005 as a Clock Synthesizer and Jitter Cleaner

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ABSTRACT

This application report is a general guide for using the CDC7005 clock synchronizer/synthesizer and jitter cleaner from Texas Instruments. This report explains the basic functionality and methods for using the device efficiently, along with the results of evaluations. It also describes the clock termination method, decoupling the power supply, and the general applications.

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1 INTRODUCTION

The CDC7005 is a high-performance, low-phase noise and low skew clock synchronizer/synthesizer and jitter cleaner that synchronize the voltage controlled crystal oscillator (VCXO) frequency to the reference clock. The programmable predividers (M and N) give a high flexibility to the frequency ratio of the reference clock to output clock that operates up to 800 MHz. Through the selection of external VCXO and loop filter components, the PLL loop bandwidth and damping factor can be adjust to meet different system requirements. Each of the five differential LVPECL outputs is programmable by serial peripheral interface (SPI). The SPI allows individually control of frequency and enable/disable state of each output. The device operates for 3.3 V. The built in Latches ensure that all outputs are synchronized.

The CDC7005 is characterized for operation from –40°C to 85°C.

2 Functional Descriptions

2.1 Clock Synchronizer

The CDC7005 has an internal prescaler, phase frequency detector, charge pump, operational amplifier, and a LVPECL clock buffer. Along with an external VCXO and loop filter, the device completes a phase locked loop (PLL). Through the PLL operation, the VCXO input clock synchronizes with the reference clock input and ultimately with all clock outputs. So, all LVPECL clock outputs are completely synchronized in terms of phase and frequency with the reference clock input.

2.2 Frequency Multiplication and Division

The device has an internal prescaler; the CDC7005 can perform frequency multiplications and divisions.

Through the SPI compatible interface, the predividers M and N can be set from 1 to 1024. Depending upon the integer values of these two dividers, the output frequency can be fixed in almost any integer or fractional numbers of the input frequency within the data sheet specified frequency range (the VCXO with the right frequency is required to generate the applications frequency). Choosing the values of M and N determines the reference and feedback frequency for the phase frequency detector (PFD) and these two frequencies must be same. The LVPECL outputs are directly related to VCXO input frequency and the output frequency can be scaled down by 1, 2, 4, 8, or 16. The bottom line is the multiplication or division factor between output to input frequency is wide, but the division factor of output to VCXO frequency is limited. See Figure 13 in the *Applications Example* section.

2.3 Jitter Cleaner

The advantage of having an external VCXO and loop filter is that a wide range of PLL loop bandwidths, as well as a low noise VCXO, can be chosen depending on the jitter requirements of the system. The jitter cleaning action depends on the PLL loop bandwidth. Up to the loop bandwidth, all noise (jitter) passes through and above the loop bandwidth, all signal noise is cleaned. The ideal loop bandwidth is chosen such that the reference clock source starts exceeding the VCXO noise floor. If the input has lot of jitter, then selecting a low loop bandwidth, jitter can be cleaned. For the CDC7005, a low loop (sub 10 Hz) bandwidth can be selected easily. The CDC7005 itself adds a low noise to its outputs. For jitter cleaning operation, the noise performance of VCXO is critical. So, with a proper loop bandwidth and applicable VCXO, the CDC7005 acts as a jitter cleaner.

2.4 Clock Distribution with Dividing Options

The CDC7005 has five LVPECL outputs. The frequencies of each output is directly related to VCXO input with /1, /2, /4, /8, and /16 options. Each output can be programmed individually by SPI. The device can be used as a simple 1:5 LVPECL buffer with dividing capabilities.

2.5 Phase Adjustment

The CDC7005 along with an external VCXO forces a PLL and ensures a zero delay operation from its input to output. However, the input-to-output phase can be shifted up to ±2.75 through SPI logic. This can be done through the SPI accurately with certain steps. The phase adjustment is critical to some applications. The output phase relation to input phase is programmable, but all outputs are adjusted together. For adjusting output phase, no external components are required.

3 PLL Loop Bandwidth Selection

Unlike other PLLs, the CDC7005's loop bandwidth is not fixed. It is possible to choose a loop bandwidth from sub 10 Hz to a few MHz.

3.1 Loop Bandwidth

The PLL loop bandwidth depends on the passive/active filter, charge pump current, VCO gain, and PFD update frequency. The pre/post dividers determine the update frequency of the phase frequency detector (PFD).
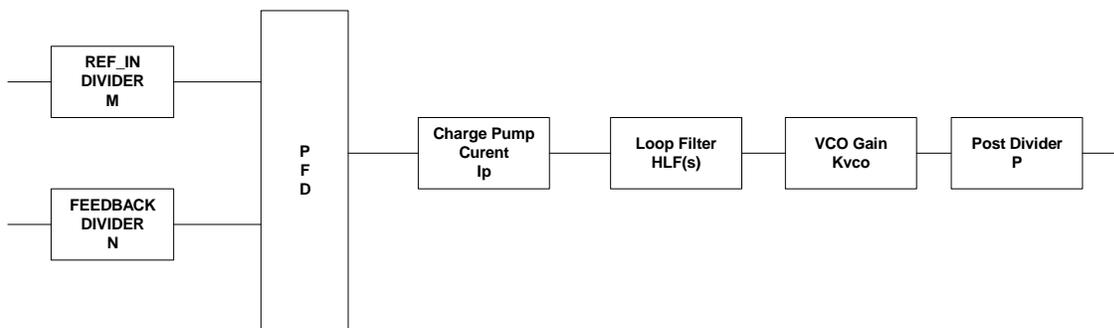

Figure 1. PLL Loop Bandwidth Parameter

3.2 Jitter Peaking

Around the loop bandwidth, the incoming jitter from the reference clock may be amplified. This phenomenon is called jitter peaking. For some applications, this has an adverse affect on jitter performance. Especially in systems with a series of PLLs, jitter peaking must be minimized. One-way to overcome jitter peaking is distributing the bandwidth of each PLL to a different frequency. In Figure 2, 2-dB jitter peaking has been observed around the PLL loop bandwidth frequency.
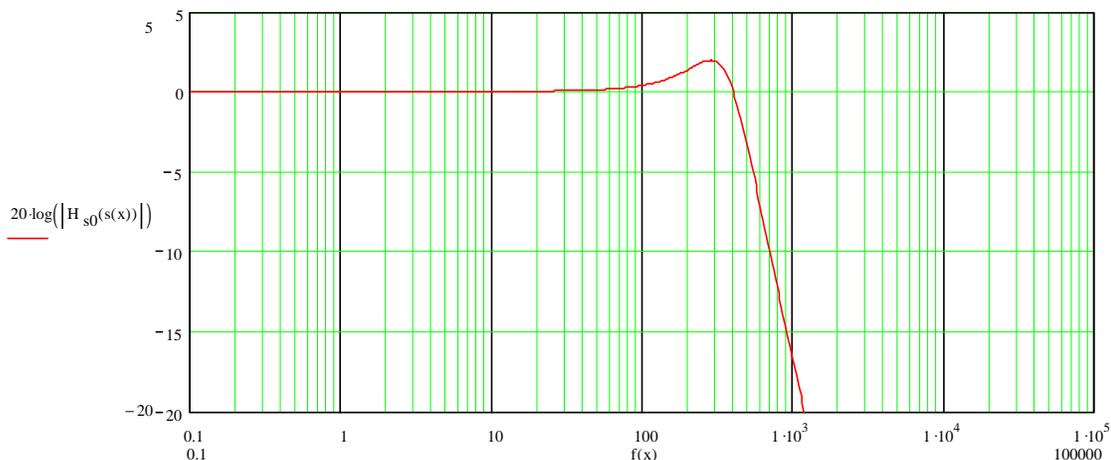

Figure 2.   Jitter Peaking Around Loop Bandwidth

3.3 Phase Margin

Phase margin is important for PLL stability and influences the PLL lock time. How fast the PLL's output is settled down, depends on the PLL loop's phase margin angle. A 55 to 80 degree phase margin is recommended for a stable clock operation.

4   Noise Performance With Different Types of Loop Filters

The CDC7005 can be configured with three types of loop filters. The device has an internal operational amplifier and can be used for an active loop filer. An external operational amplifier can also be used to form an active filter. An external RC passive filter is recommended for loop filters, as it does not add noise to the charge pump's output. If VCXO input impedance is low, an active loop filter is recommended, as it can handle a lower impedance by compensating leakage current.

4.1 Passive Loop Filter

The passive loop filter generates a complex pole and zero (R1, C1, C2). The zero is required for the overall loop stability and the generated pole is the dominant pole of the system. A second pole is introduced by the R2 and C3.

![Texas Instruments logo]
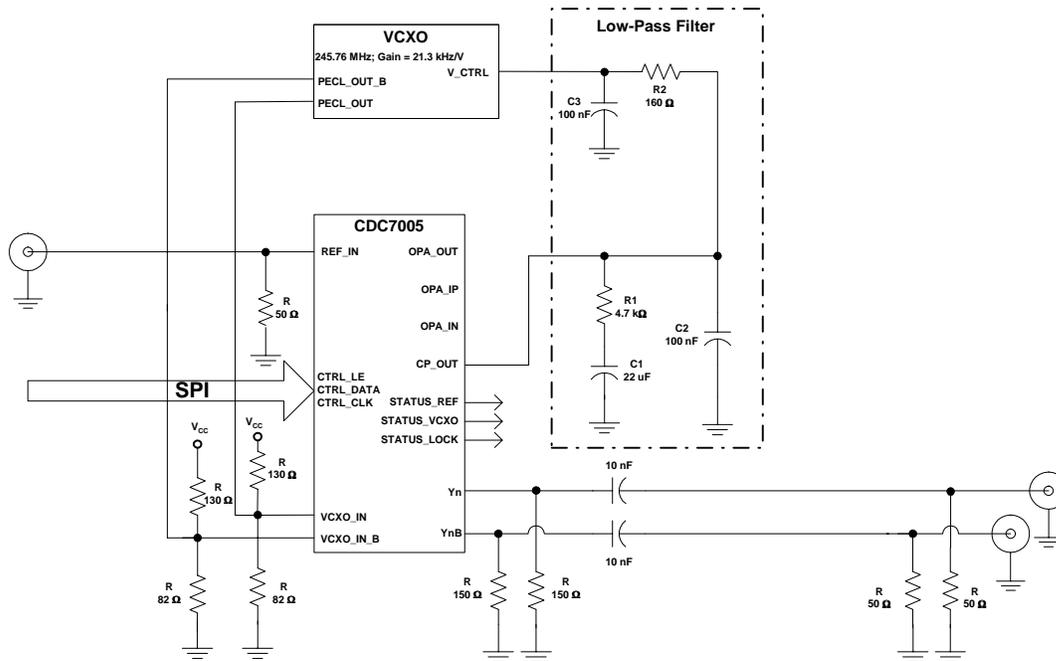
Figure 3.   CDC7005 With Passive Loop Filter

4.1.1 Loop Parameter Values

Phase noise on the EVM board with a 245.76-MHz VCXO and 30.72-MHz reference input clock from Agilent E8257C.

Power supply: HP E3631A

Ref divider: 128

FB divider: 128

Pre-divider: 8

VCXO frequency: 245.76 MHz

PECL out frequency: 30.72 MHz

Icp : 2 mA

VCXO gain: 21.3 kHz/V

Passive filter: R1 = 4.7 kΩ, C1 = 22 μF, C2 = 100 nF, R3 = 160 Ω, C3 = 100 nF

Loop Bandwidth = 25 Hz

4.1.2 Measured Noise Performance

Figure 4.   Phase Noise Performance With a Passive Filter

4.2   Active Loop Filter With Internal OPA

The operational amplifier needs external resistors and capacitors to create poles and zero. R2 and C2 generate a zero. R1 and C1 generate one pole and R3 and C3 introduces the second pole.

Figure 5. CDC7005 With Active Loop Filter Using Internal OPA
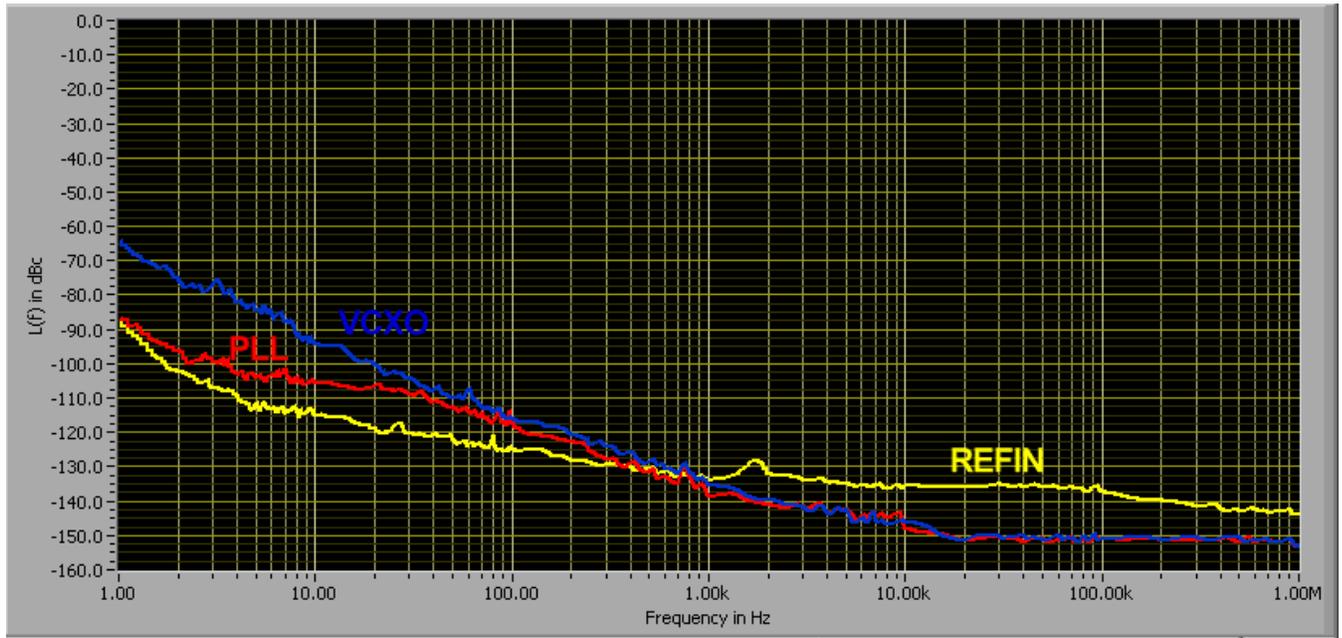
4.2.1 Loop Parameters Values

Phase noise on the EVM board with a 245.76-MHz VCXO and 30.72-MHz reference input clock from Agilent E8257C.

Power supply: HP E3631A

Ref divider: 128

FB divider: 128

Pre-divider: 8

VCXO frequency: 245.76 MHz

PECL out frequency: 30.72MHz

Icp: 2 mA

VCXO gain: 21.3 kHz/V

Active filter: R1 = 180 Ω, R2 = 4.7 kΩ, C2 = 10 μF, C3 = 100 nF, R3 = 10 kΩ, C4 = 100 nF, internal OPA

Loop bandwidth = 25 Hz

4.2.2 Measured Noise Performance

Figure 6. Phase Noise Performance With Internal OPA

4.3 Active Loop Filter with External OPA

An external operational amplifier with resistors and capacitors can be used for a low-pass active filter.
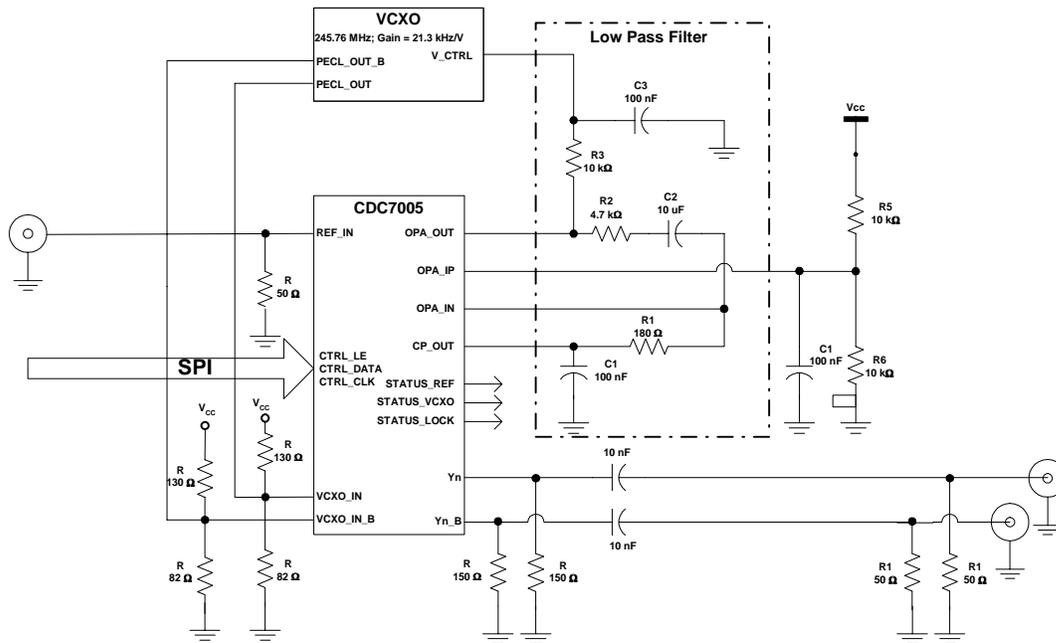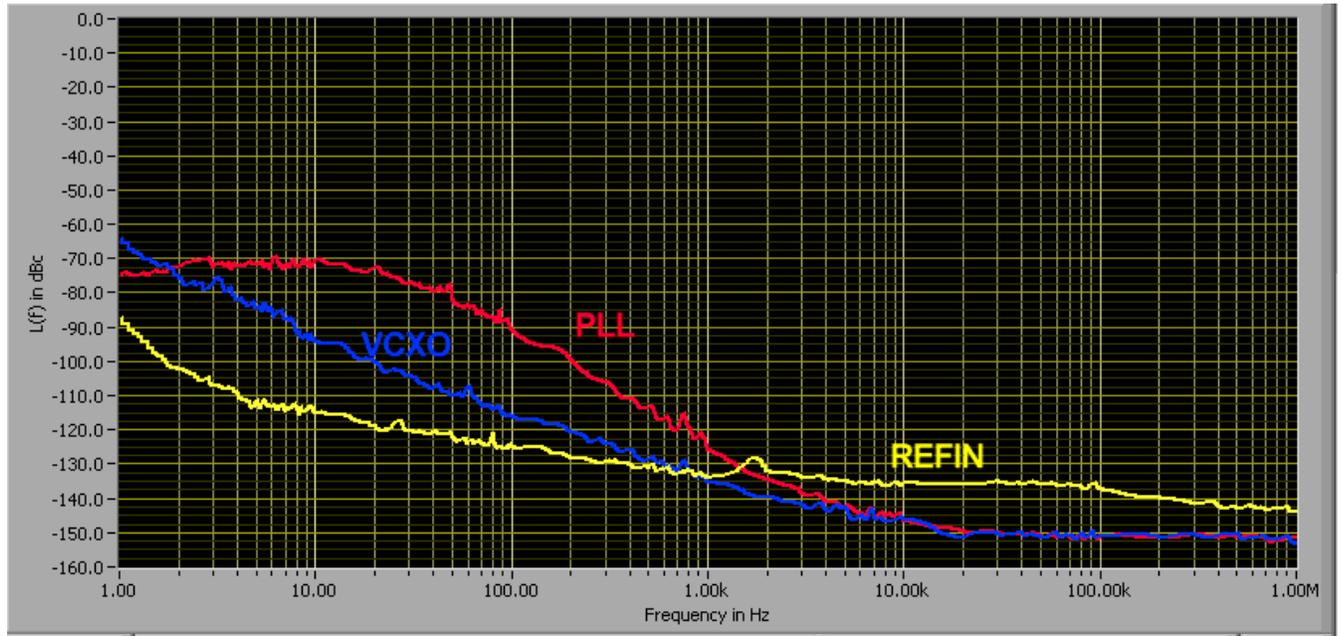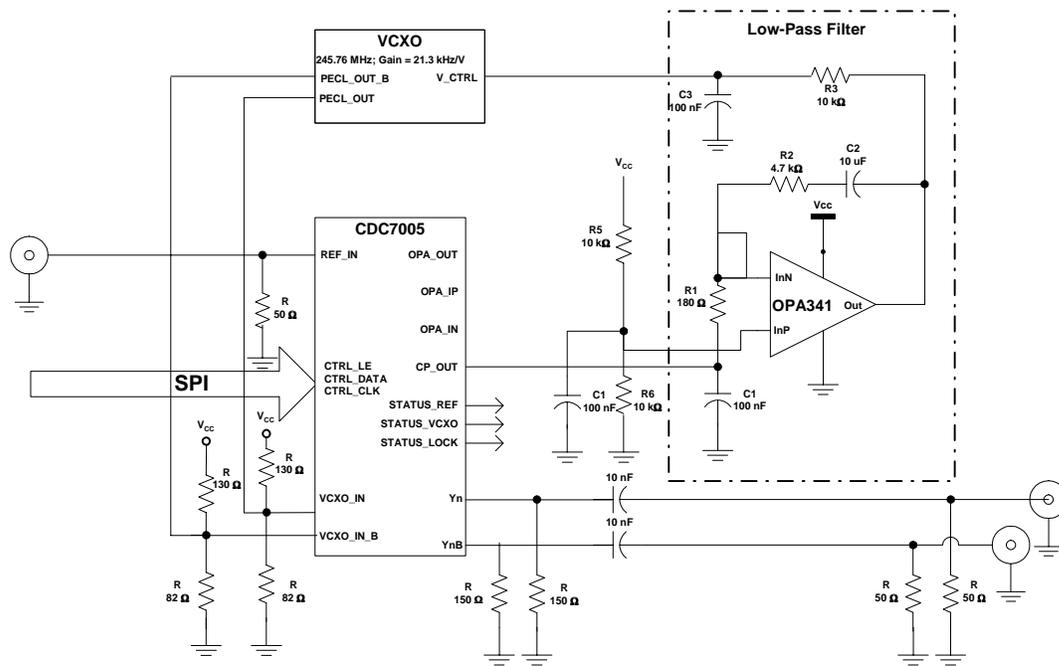
Figure 7. CDC7005 With Active Loop Filter Using External OPA

4.3.1 Loop Parameters Values

Phase noise on the EVM board with a 245.76-MHz VCXO and 30.72-MHz reference input clock from Agilent E8257C.

Power supply: HP E3631A

Ref divider: 128

FB divider: 128

Pre-divider: 8

VCXO frequency: 245.76 MHz

PECL out frequency: 30.72 MHz

Icp: 2 mA

VCXO gain: 21.3 kΩ

Active filter: R1 = 180 Ω, R2 = 4.7 kΩ, C2 = 10 μF, C3 = 100 nF, R3 = 10 kΩ, C4 = 100 nF, external TI341 OPA

Loop bandwidth = 25 Hz

4.3.2 Phase Noise Performance

Figure 8. Phase Noise Performance With External OPA

5 CDC7005 With Single-Ended VCXO

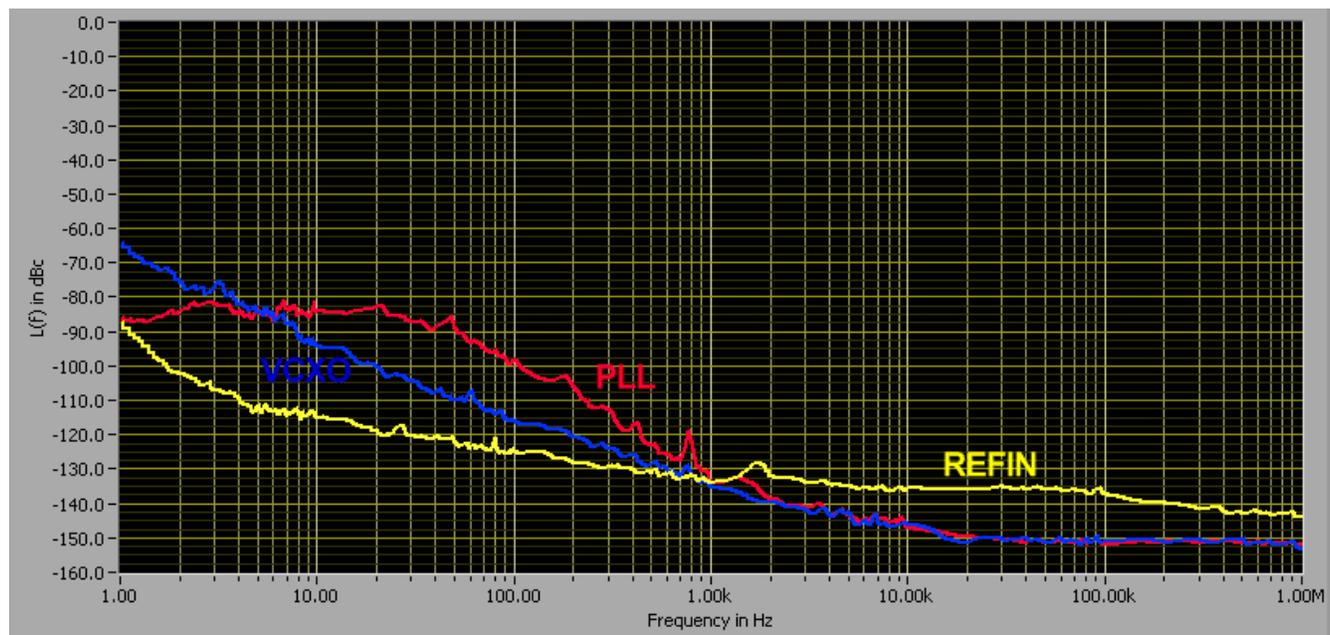Lower frequency LVPECL VCXO is rare and often expensive. The CDC7005 VCXO input requires minimum 500 mV to maintain the ac specifications. So, any signal with at least 500-mV swing can be easily used as the VCXO inputs for the CDC7005. The most common low frequency VCXO has the LVTTL/LVCMOS signaling level. But this signal swing is too high to drive the CDC7005 LVPECL input. If there is a signal with more than 1.32-V swing, it violates the requirements of V_{OH} and V_{OL} at 3.3-V power supply. So, it is required to reduce the voltage swing and to bias properly so that it can maintain the proper swing and common mode input voltage (V_{CC} – 2 V to V_{CC} – 0.4 V). That is why the recommendation is to use a divider circuitry to reduce the signal swing and a biasing circuitry which can set the right common-mode voltage. The trace also needs to be terminated properly.

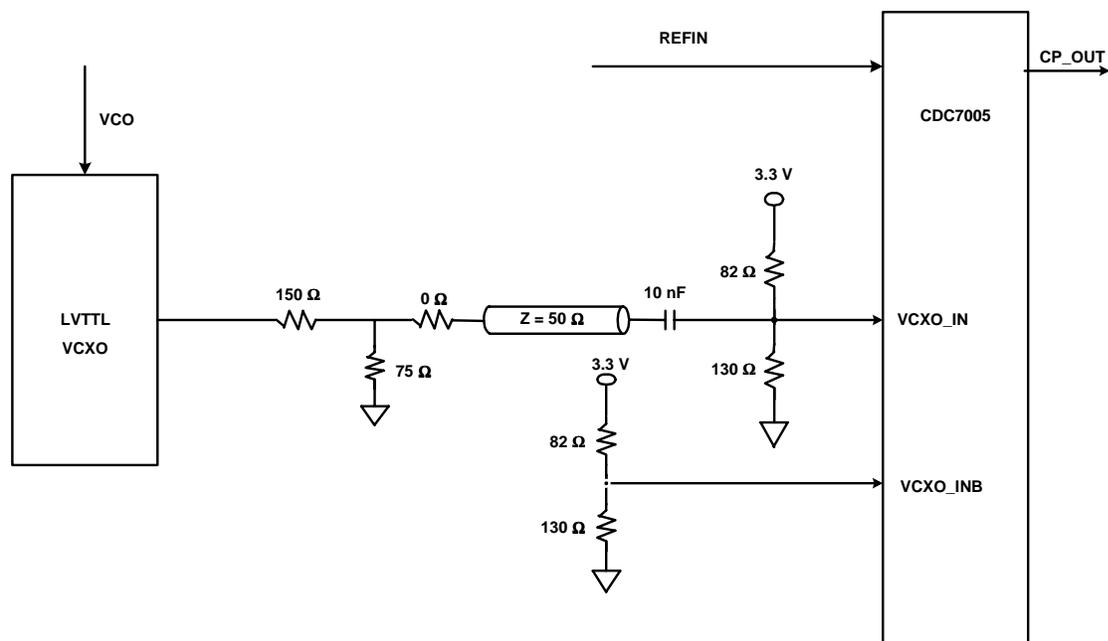Here is an example how single ended VCXO can be interfaced with CDC7005.

Figure 9.   CDC7005 With a Single-Ended VCXO

6   LVPECL Termination

The CDC7005 is a 3.3-V LVPECL clock driver with an open emitter. Therefore, proper biasing and termination is required to ensure the correct operation of the device and to minimize the signal integrity. The proper termination of the LVPECL output is 50 Ω to (V_{CC} − 2 V), but not popular in real applications as (V_{CC} − 2 V) supply is not always available in the board. There are many recommended termination circuits to solve the issue. Either the direct termination or termination with ac-coupled can be used to terminate the VCXO input and the CDC7005 outputs. It is recommended to place all resistive components close to either driver end or receiver end. If the supply voltage of driver and receiver are different (i.e., common mode voltage is different), ac-coupled termination is required.

6.1   Direct Coupled (DC) LVPECL Termination

In order eliminate the necessity of having an extra power supply (1.3 V for 3.3-V operation) on the board, a thevenin equivalent network composed of two resistors with 3.3-V power supply replace the 50 Ω to (V_{CC} − 2 V) circuitry to ensure required biased and termination. Figure 10 shows a termination circuit that is a general recommendation for dc termination.
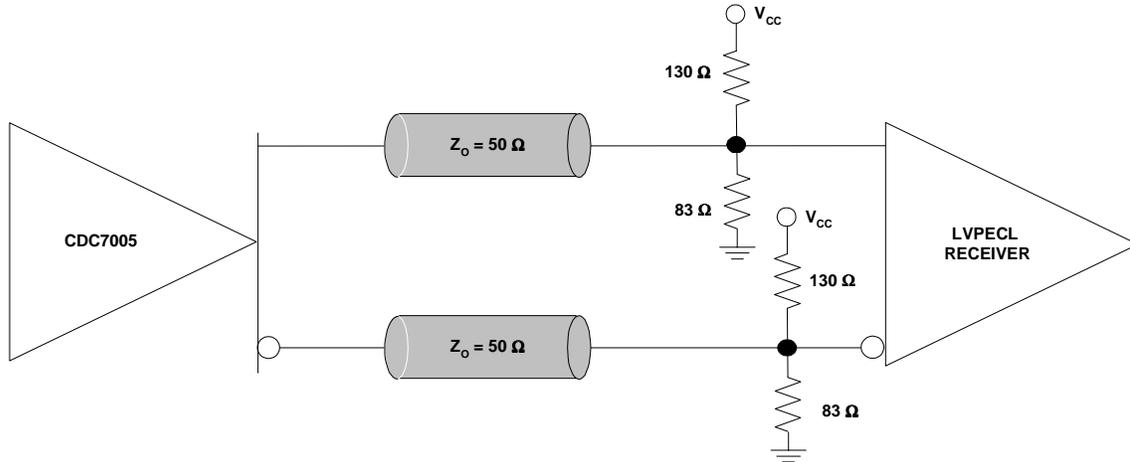
Figure 10.   DC Termination Circuit

6.2 AC-Coupled Termination

The ac-coupled termination can be used to drive LVPECL receivers from the CDC7005. Both input and output stages must be biased properly. The 150-Ω resistor close to the CDC7005 assures proper output biasing, while 1.3-kΩ / 2-kΩ resistors network bias the LVPECL receiver input stage. The termination circuit in Figure 11 is a general recommendation of an ac-coupled termination.
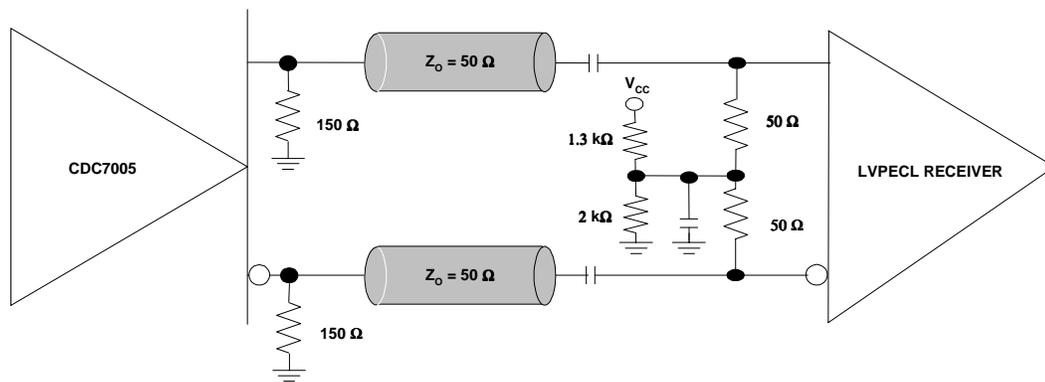
Figure 11.   AC-Coupled Termination Circuit

7   Decoupling Power Supply

The PLL based clock drivers and generators are very sensitive to noise on the power supply voltage. Noise on power supply can dramatically increase the jitter of the PLL. It is required to reduce noise from the system power supply especially when jitter/phase noise is very critical to applications. A PLL is practically sensible to noise at frequencies near and above the selected bandwidth of the PLL.

Filter capacitors are used to eliminate the low frequency noise from power supply, where as, the bypass capacitors provide the very low impedance path for high frequency noise and guard the power supply system against the induced fluctuations. Inserting a ferrite bead between the board power supply and analog V_{CC} isolates the high frequency switching noises generated by the clock driver, preventing them from interrupting the board supply. The digital power supply (V_{CC}) should be decoupled with a filter capacitor. Figure 12 shows a general recommendation for decoupling the analog power supply.
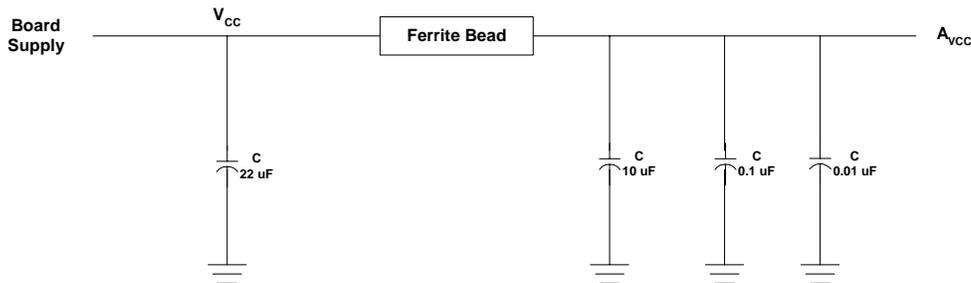

Figure 12. Analog Power Supply Decoupling

For decoupling, low-impedance ceramic-chip capacitors are recommended and for best performance, all components should be placed as close as possible to supply pins of the device.

8   Applications Example

8.1   Setting Example for Buffer Only with Dividing Options

The CDC7005 can be used a simple buffer with dividing options. In this situation, the PLL operation is inactive and the charge pump output is in Hi-Z. Each output can be programmed individually to enable or disable.
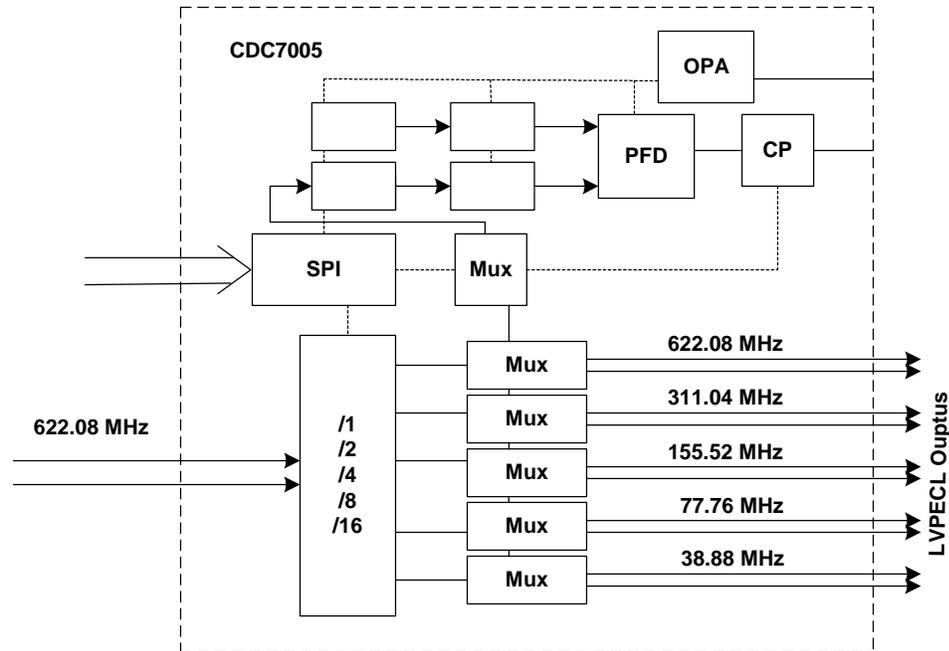
Figure 13.   Setting Example for Buffer Only with Dividing Options

8.2   Setting Example for Multiplication and Division

The CDC7005 can be used as a multiplier and a divider. The multiplying or dividing factor depends the post and predivider value. The predivider value can be chosen up to 1024, so the device has great flexibilities to fix the multiplying or dividing factor.
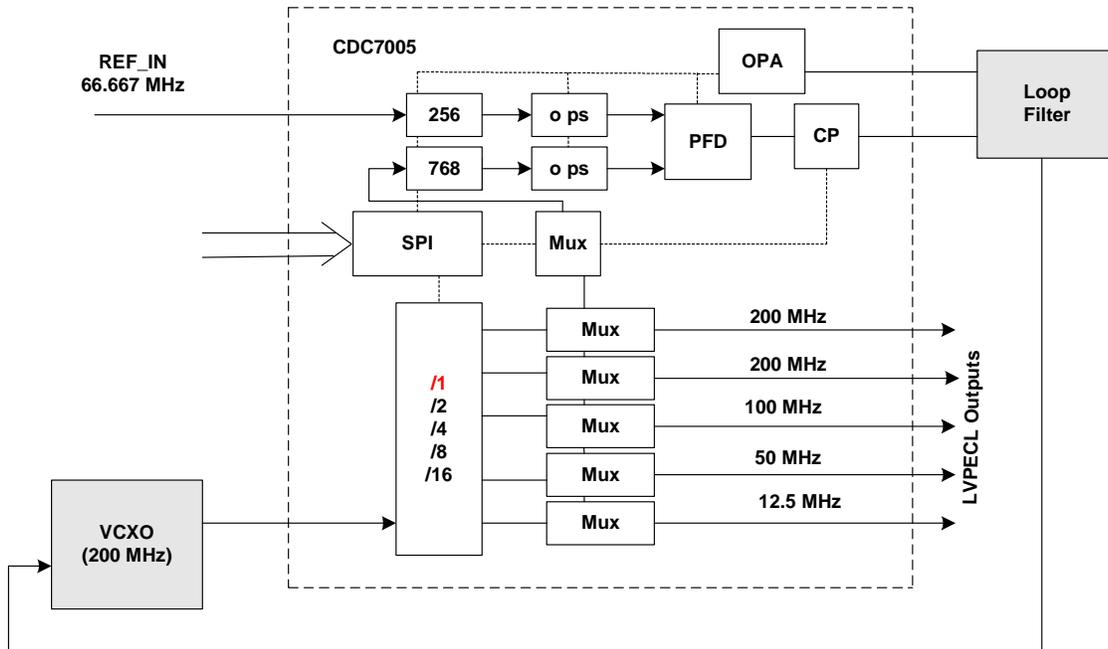
Figure 14. Setting Example for Multiplication and Division

8.3 Providing Low Jitter Clock to SERDES

The serializer and de-serializer (SERDES) need clean clocks for the safest operation. The reference clock often requires to multiply up and to synchronize with the system clock. The CDC7005 is an excellent clock drive, which can multiply and ensure the low jitter clock outputs.
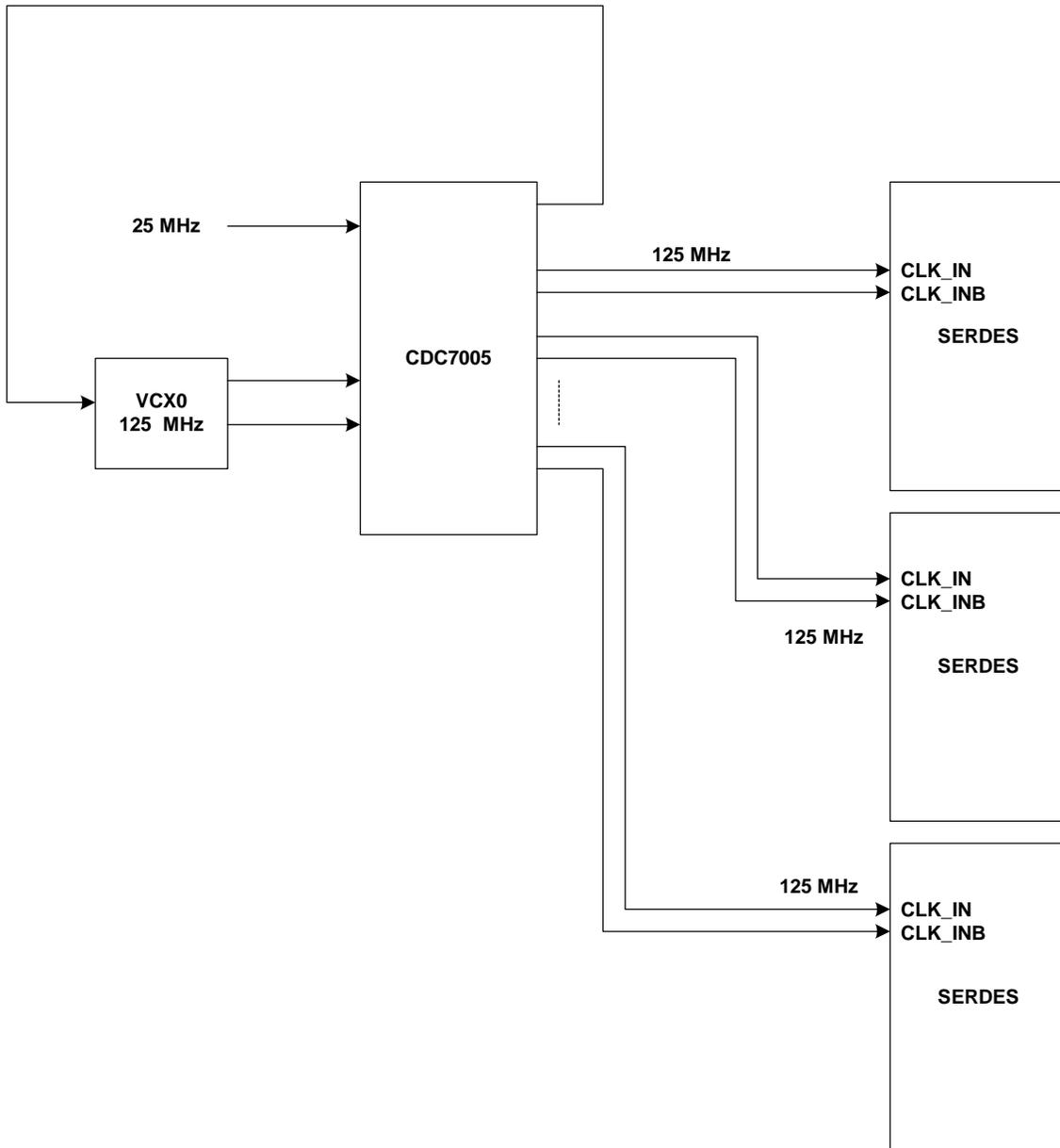
Figure 15. Providing Clean Clock to SERDES

8.4 Driving SERDES with FPGA

The clock generated by the FPGA is generally noisy and often does not meet the jitter requirement of SERDES. So, an external clean clock is required and data from FPGA and the clock must be synchronized at the SERDES end. This ensures optimal (low) bit error rates.
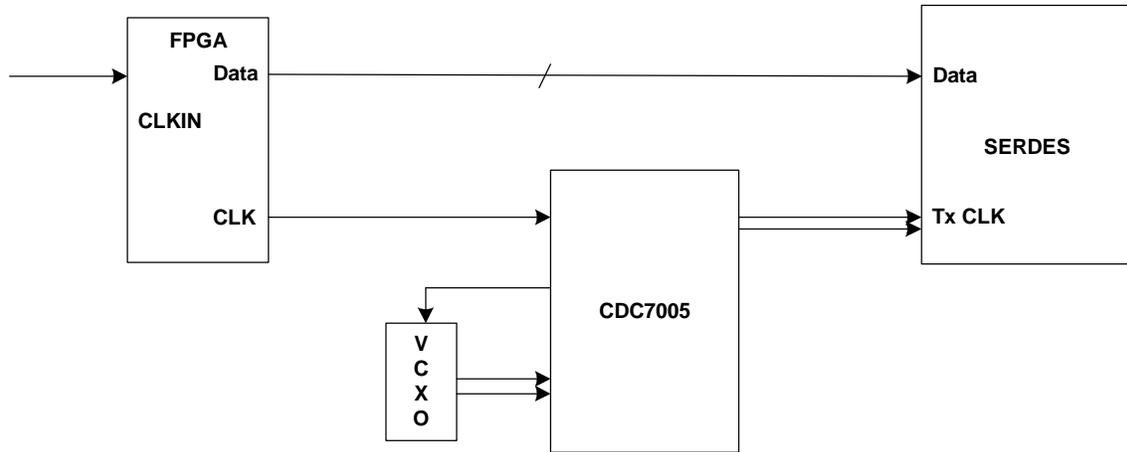
Figure 16. Driving SERDES with FPGA

8.5 Providing Low-Phase Noise Clock to DAC and ADCs

The digital-to-analog converter (DAC) and the analog-to-digital converter require low-noise clock signals to ensure high SNR. The CDC7005 can generate low-noise clock signals using an external VCXO and lower PLL loop bandwidth. The PLL itself adds less than 0.5-ps RMS (over 12-kHz to 20-MHz bandwidth) jitter to the clock output.
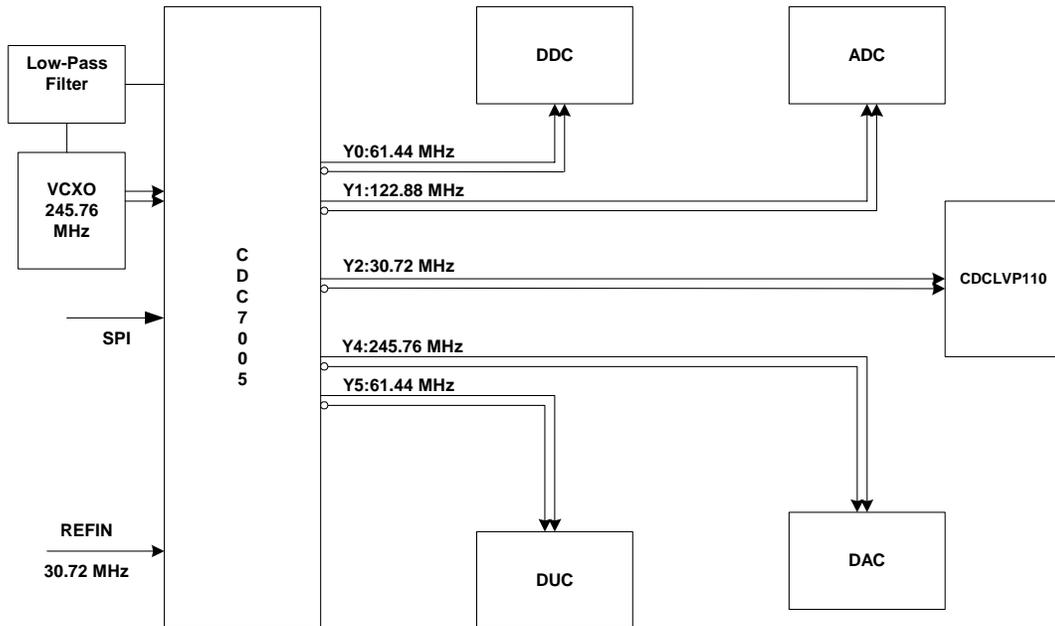

Figure 17. Driving DACs and ADCs

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