Application Note

TXE Series 16/24/48-bit SPI Controlled I/O Expander Fail-Safe Applications

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ABSTRACT

This application note illustrates two MCU fail-safe use cases that utilize the fail-safe I/O register set of the TXE series of automotive qualified I/O expanders. Example use cases range from maintaining a reliable state during a MCU reboot (firmware update) to holding the system into a known state when an MCU fails.

The TXE series of I/O expanders include TXE8116-Q1, TXE8124-Q1, and TXE8148-Q1.

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Trademarks

1 Introduction

The TXE81xx-Q1 SPI controlled I/O expander has unique fail-safe registers that puts the device in a known state if a failure mode is triggered externally. The $\overline{\text{RESET}}$ pin of this device can be configured as an active-low fail-safe input that puts the device into fail-safe mode when asserted low.

The diagram below shows a subset example automotive zone control system with a PMIC, MCU, high-side switch, and the TXE81xx-Q1 I/O expander. The SPI bus is routed from the MCU or processor to the TXE81xx-Q1, TPS2HCS08-Q1, and the TPS65386x-Q1. The PMIC has a watchdog flag that must be cleared on a periodic time interval by the MCU. If the MCU misses its regular clear of this watchdog event inside the PMIC, the MCU is considered to be in a failing state. Thus, the PMIC sends a $\overline{\text{SAFE\_OUT}}$ signal to the TPS2HCS08-Q1 and TXE81xx-Q1. The LHI (limp home input) pin of the high-side switch is driven high to cut current to the switch. The $\overline{\text{SAFE\_OUT}}$ signal also pulls the $\overline{\text{FAIL\_SAFE}}$ pin of the TXE81xx-Q1 low which puts the I/O expander in its pre-programmed fail-safe output state.

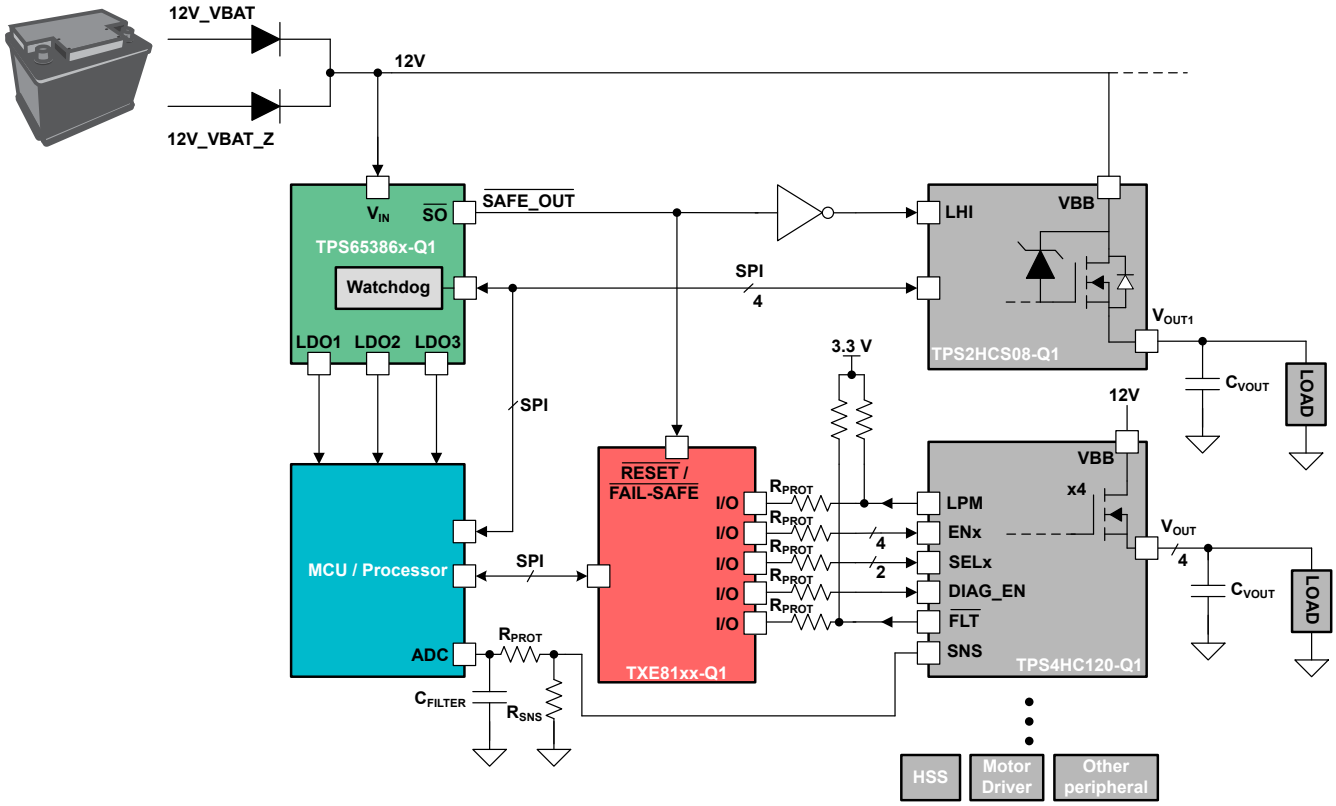


Figure 1-1. Example Block Diagram of TXE81xx-Q1 I/O Expander

It is important to note that if the MCU or processor powered up improperly, the TXE81xx-Q1 would have not been programmed to act in fail-safe mode. The $\overline{\text{SAFE\_OUT}}$ signal from the PMIC would result in a reset condition for the TXE81xx-Q1. The TXE reset or fail-safe pin acts as a reset pin by default until configured by writing to the fail-safe enable register. In the scenario that $\overline{\text{RESET}}$ = low, the I/O's of the TXE would become high impedance. An external deterministic factor like a pull-up or pull-down resistor would need to be used for the downstream high-side switch condition, otherwise ENx, SELx, DIAG_EN is left floating.

2 Overview of the Fail-Safe Register Set

The TXE81xx-Q1 series of I/O expanders implements fail-safe registers. A fault flag from an external device can be relayed to the TXE81xx-Q1 in order to put the I/O expander into a known state.

The fail-safe feature is configured through 4 registers, each of which has a copy for redundancy. This includes:

1. Fail-safe Enable Registers
2. Fail-safe Direction Configuration Registers
3. Fail-safe Output Registers
4. Fail-safe Redundancy Check Register

There are two identical registers (1 & 2) of each of the four types. For example, there exists "Fail-safe Output Register 1" and "Fail-safe Output Register 2." This is to verify software redundancy between fail-safe registers. If register 1 contains different data than register 2, then bit B1 of the fault status register will be set, alerting the user that there was a data write error.

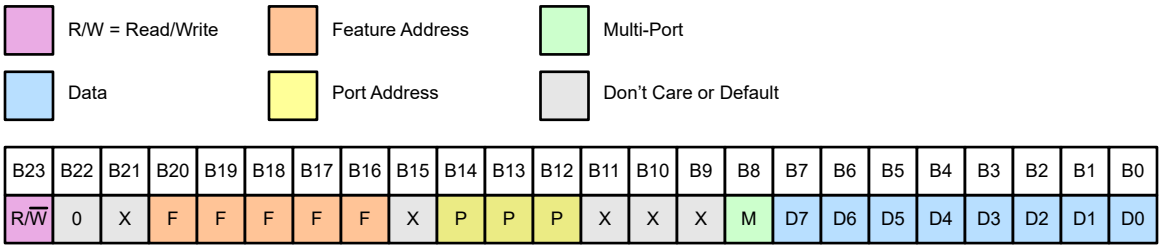
The fault status register is used to determine if there is a register mismatch which indicates one of the fail-safe registers is out of sync. The fault status register also indicates when the device fault status is active, or a power on reset has occurred. These flags are not cleared even if the fault condition goes away, but they are cleared only by a read operation.

Table 2-1. Fail-Safe Register Map and Fault Status Register

Register Name	Offset	Function
Fail-safe Enable Register-1	120h	Configures the $\overline{\text{RESET}}$ pin to a $\overline{\text{FAIL-SAFE}}$ pin.
Fail-safe Enable Register-2	130h	Configures the $\overline{\text{RESET}}$ pin to a $\overline{\text{FAIL-SAFE}}$ pin.
Fail-safe Direction Configuration Register-1	140h + (y * 1h) Where y = 0h to 2h	Configures the direction of each I/O Input = 0 Output = 1
Fail-safe Direction Configuration Register-2	150h + (y * 1h); Where y =0h to 2h	Configures the direction of each I/O Input = 0 Output = 1
Fail-safe Output Register-1	160h + (y * 1h) Where y = 0h to 2h	Configures the logic output of each I/O configured as an OUTPUT through the Fail-safe Direction Configuration Registers
Fail-safe Output Register-2	170h + (y * 1h); Where y = 0h to 2h	Configures the logic output of each I/O configured as an OUTPUT through the Fail-safe Direction Configuration Registers
Fail-safe Redundancy Check Register	180h	After writing all fail-safe registers (enable, configuration, output), enables redundancy checks on these registers. If fail-safe registers are mismatched, a flag will be set in the fault status register.
Fault Status Register	190h	Bit 0 - Power-on Reset Recovery Status Bit 1 - Fail-safe function cleared due to register mismatch Bit 2 - Fail-safe function is Active

3 How to Write to a Fail-Safe Register

TXE81xx-Q1 uses a 24-bit SPI word to program the device.



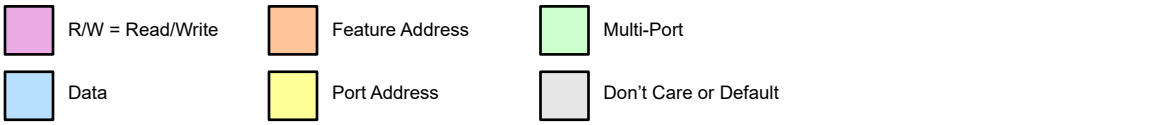
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R/$\overline{W}$	0	X	F	F	F	F	F	X	P	P	P	X	X	X	M	D7	D6	D5	D4	D3	D2	D1	D0

Figure 3-1. 24-Bit SPI Word for TXE81xx-Q1

Where:

- R/W = Read / Write
- X = don't care / default value
- F = Feature Address
- P = Port Address
- M = Multi-port bit
- D = data (MSB to LSB)

For example, write to the fail-safe output register 2 (0x17), on port 2, with P2.7 - P2.4 = HIGH, and P2.3 - P2.0 = LOW, multi-port disabled.



B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	X	1	0	1	1	1	X	0	1	0	X	X	X	0	1	1	1	1	0	0	0	0

Figure 3-2. Example Write Condition (B23 = 0) to Fail-Safe Output Register 2 (B20-B16 = 0b10111), Port 2 (B14-B12 = 0b010), Multi-port disabled (B8 = 0), Set P2.7-P2.4 HIGH (B7-B4 = 0b1111), Set P2.3-P2.0 LOW (B3-B0 = 0b0000)

4 Fail-Safe Use Case #1 - MCU Communication Loss- Limp Home Mode

An MCU may lose communication during system operation. A TXE81xx-Q1 I/O expander can be used to hold the vehicle in a "limp home mode" state. The TXE81xx-Q1 can step in to hold the critical states for the vehicle so that it can operate safely in a reduced function state (i.e. limp home mode).

For this example, the following code block is used to set the normal operating state of the TXE8124-Q1. Each Port is set to OUTPUT, with output logic for each port as follows. This is the state of the I/O expander when not in fail-safe.

Port 0 = 0x00

Port 1 = 0x55

Port 2 = 0x0F

```
//Configure IO's to OUTPUT on each port through the direction configuration register (0x04)
SPI_TRANSFER(0x04, Port_0, 0xFF);
SPI_TRANSFER(0x04, Port_1, 0xFF);
SPI_TRANSFER(0x04, Port_2, 0xFF);

//Set Output logic: Port_0 = 0x00, Port_1 = 0x55, Port_2 = 0x0F, through the output port register
(0x03)
SPI_TRANSFER(0x03, Port_0, 0x00);
SPI_TRANSFER(0x03, Port_1, 0x55);
SPI_TRANSFER(0x03, Port_2, 0x0F);
```

The next example code is written to the TXE8124-Q1 in order to program the fail-safe registers. First, write to the fail-safe enable registers 1 & 2 at offsets 120h and 130h. Then program the fail-safe direction configuration registers 1 & 2 at offsets 140h + (y * 1h) and 150h + (y * 1h). All of the I/O's are programmed to be outputs in this example. Program the logic of the outputs by writing to the fail-safe output registers 1 & 2 at offsets 160h + (y * 1h) and 170h + (y * 1h). 0xAA is used as an example in this coding use case. Then set the FSCHECKEN bit in the fail-safe redundancy check register at offset 180h.

```
//Configure the fail-safe registers

//Fail-safe enable register 1 (0x12), Fail-safe enable register 2 (0x13), set B0  = 1
SPI_TRANSFER(0x12, Port_0, 0x01);
SPI_TRANSFER(0x13, Port_0, 0x01);

//Fail-safe Direction Configuration Register 1 (0x14), set each port IO's to OUTPUT (0xFF)
SPI_TRANSFER(0x14, Port_0, 0xFF);
SPI_TRANSFER(0x14, Port_1, 0xFF);
SPI_TRANSFER(0x14, Port_2, 0xFF);

//Fail-safe Direction Configuration Register 2 (0x15), set each port IO's to OUTPUT (0xFF)
SPI_TRANSFER(0x15, Port_0, 0xFF);
SPI_TRANSFER(0x15, Port_1, 0xFF);
SPI_TRANSFER(0x15, Port_2, 0xFF);

//Fail-safe Output Register 1 (0x16), set the port output logic to 0xAA (high-low-high...)
SPI_TRANSFER(0x16, Port_0, 0xAA);
SPI_TRANSFER(0x16, Port_1, 0xAA);
SPI_TRANSFER(0x16, Port_2, 0xAA);

//Fail-safe Output Register 2 (0x17), set the port ouptut logic to 0xAA (high-low-high...)
SPI_TRANSFER(0x17, Port_0, 0xAA);
SPI_TRANSFER(0x17, Port_1, 0xAA);
SPI_TRANSFER(0x17, Port_2, 0xAA);

//Fail-safe Redundancy Check Register (0x18), set B0 = 1 to enable the fail-safe redundancy check
SPI_TRANSFER(0x18, Port_0, 0x01);
```

The block diagram of the example hardware setup is shown below. The MCU loses communication and can no longer clear the watchdog flag of the PMIC. A fault signal $\overline{\text{SAFE\_OUT}}$ is sent to the $\overline{\text{FAIL\_SAFE}}$ pin of the TXE8124-Q1 to trigger fail-safe mode. The TXE8124-Q1 will output the fail-safe logic as programmed above. The outputs will be 0xAA on all I/O ports, setting the functionality of the high-side switch and motor driver to a known output state while the MCU is inoperable. The value of 0xAA is completely arbitrary and is used only for

the purpose of the example. The exact value may differ in actual system application for a for a limp-home mode state.

A TPS4HC120-Q1 GPIO controlled high-side switch is used to drive LED's for visiual representation. In an automotive application, the high-side switch normally drives modules in lighting systems, motor control, various sensors and actuators, relays, e-fuses, and battery management systems. The use of LED's is for visual understanding to show when the high-side switch is disabled due to TXE8124-Q1 entering fail-safe mode.

A DRV8714H-Q1 motor driver is use to drive two small motors with fans for visual representation. When TXE8124-Q1 enters a fail-safe state, it is easy to see which motor is continuing to operate and which motor is disabled.

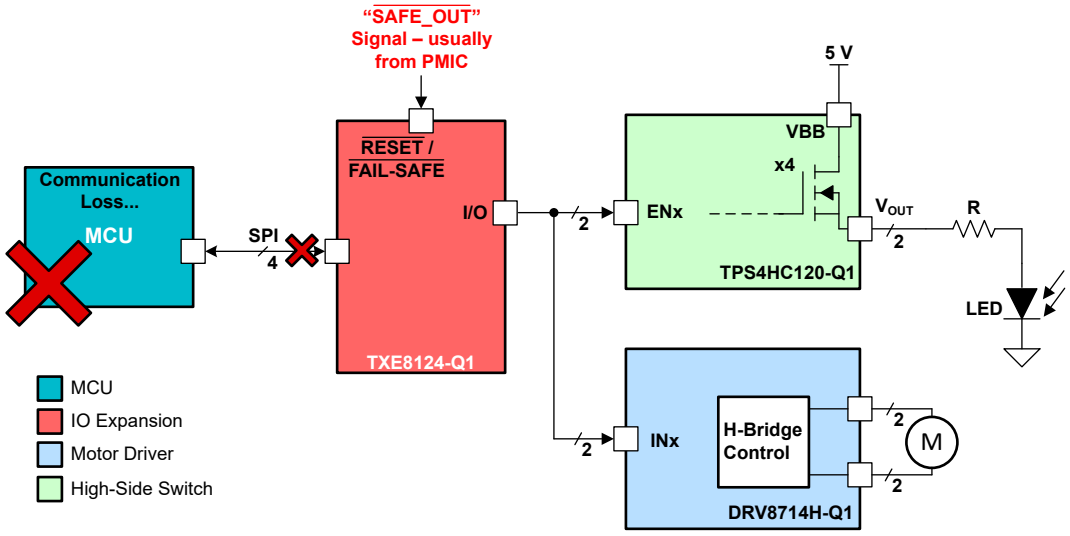


Figure 4-1. Use Case 1 - MCU Communication Loss - "Limp Home Mode"

Below is the TXE8124-Q1 operating in the normal state. Port 0 = 0x00, Port 1 = 0x55, Port 2 = 0x0F. These are arbitrary values selected for the output state. Port 2 controls the inputs to the TPS4HC120-EVM and DRV8714H-Q1EVM which enable both LED's and both motors in the system.

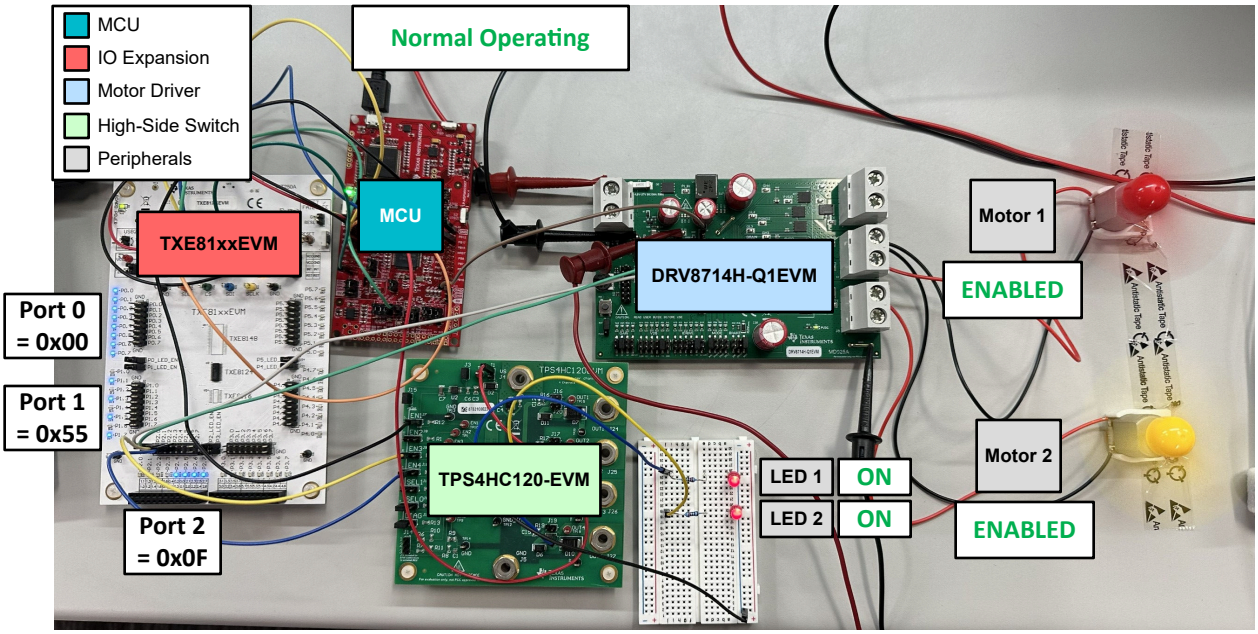


Figure 4-2. Normal Operation of TXE8124-Q1 on TXE81xxEVM

In the fail-safe state, the fail-safe pin of the TXE8124-Q1 is pulled low - indicating that the system is to enter a fail-safe state.

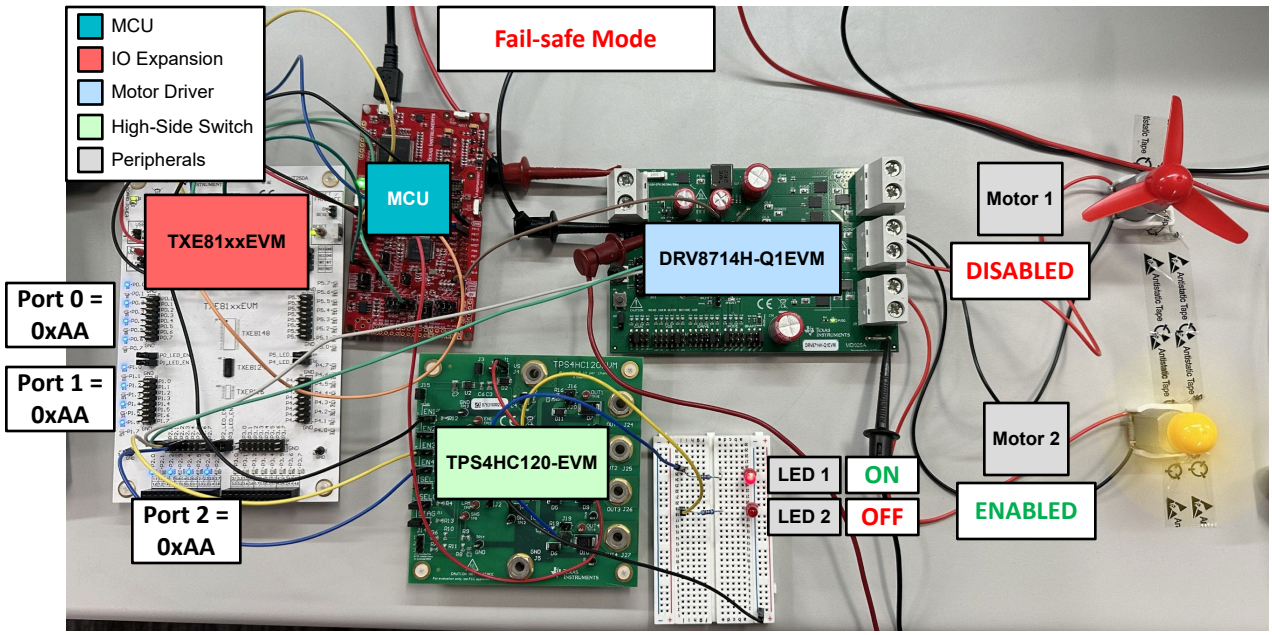


Figure 4-3. Fail-safe Mode - Output Ports set to 0xAA - This Disables Motor 1 and LED 2

Although this bench example is a representation of a true automtive zone control module, this demonstrates a clear example of a pre-configured fail-safe state that the TXE81xx-Q1 I/O expander can enter in the case that the MCU loses communication - limp home mode state.

5 Fail-Safe Use Case #2 - MCU Software Update / Reboot

A MCU may need to conduct an update or reboot procedure in a typical software defined vehicle application. While the MCU is in a reset state, the I/O's cannot be in an undetermined state. To keep the I/O's deterministic, an I/O expander like TXE81xx-Q1 can hold the necessary state while the MCU updates or reboots.

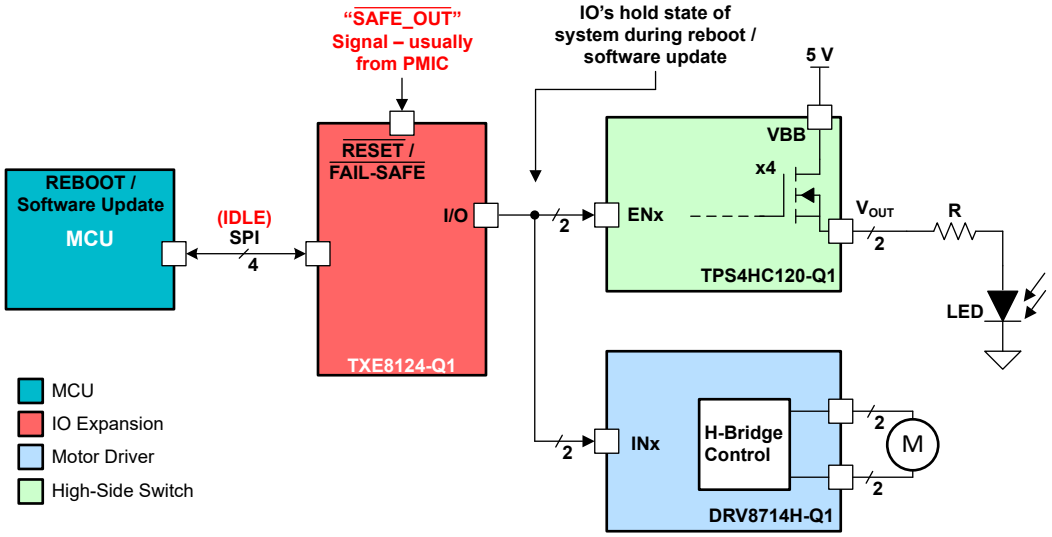


Figure 5-1. The MCU Enters a Reboot or Software Update State - The TXE81xx-Q1 can Hold Devices in the Zone to a Known State

6 Summary

The TXE81xx-Q1 SPI controlled I/O expander can be used in automotive zone control modules that require fail-safe states during a communication loss of an MCU or processor. TXE81xx-Q1 is versatile with its fail-safe register set, while also providing additional I/O's (16-bit, 24-bit, 48-bit) necessary for large zone control module platforms.

7 References

- Texas Instruments, *TXE81XX-Q1 Automotive 16-Bit and 24-Bit SPI Bus I/O Expander with Interrupt Output, Reset Input, and I/O Configuration Registers*, datasheet.
- Texas Instruments, *TXE81XX-Q1 Automotive 16-Bit and 24-Bit SPI Bus I/O Expander with Interrupt Output, Reset Input, and I/O Configuration Registers*, datasheet.
- Texas Instruments, *TXE8148-Q1 Datasheet*, datasheet.
- Texas Instruments, *TPS4HC120-Q1 120mΩ, 2A, Quad-Channel Automotive Smart High-Side Switch*, datasheet.
- Texas Instruments, *DRV871x-Q1 Automotive Multi-Channel Smart Half-Bridge Gate Drivers With Wide Common Mode Inline Current Sense Amplifiers*, datasheet.
- Texas Instruments, *TPS4HC120EVM Evaluation Module*, EVM user's guide.
- Texas Instruments, *DRV8714H-Q1EVM*, product page
- Texas Instruments, *TXE81xxEVM*, product page.
- Texas Instruments, *TXE8124-Q1 Functional Safety FIT Rate, FMD and Pin FMA*, functional safety pin FMA

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