Application Note

AM13E230x Hardware Design Guidelines

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ABSTRACT

The AM13E230x Hardware Design Guidelines is an essential document for hardware designers creating PCB systems based on the AM13E230x family of real-time control MCU devices. This document serves to integrate device-specific schematic and PCB layout recommendations by utilizing hardware design examples from the AM13E230x Evaluation Modules (EVMs) and reference designs. The AM13E230x hardware platforms include the following.

Table 1-1. AM13E230x Hardware Platforms

EVM Orderable Part Number	TI EVM Standard	Purpose
LP-AM13E230	LaunchPad	Low-cost, entry-level evaluation platform. Features the 64-pin QFP, 512KB AM13E23019GTPM MCU
AM13E230-SOM-EVM	controlSOM (System on Module)	Complex system evaluation with higher I/O requirements. Features the 128-pin QFP, 512KB AM13E23019GTPDT MCU

Additional collateral documents and tools can be found in *References*.

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1 Introduction

The AM13E230x real-time control microcontrollers are single-core ARM® Cortex®-M33 based devices intended for industrial motor control applications, including appliances, industrial automation, robotics, and building automation.

This guide must be referenced along with the other key AM13E230x collateral documents. See *References* for a complete list of supplementary documentation for the AM13E230x devices.

Table 1-1. Acronyms Used in This Document

Acronym	Description
EVM	Evaluation Module. Referencing TI PCB assemblies such as the AM13E230x LaunchPad (LP-AM13E230)
EMI	Electromagnetic Interference
BOM	Bill of Materials
SOM	System on Module
LP	LaunchPad

2 Schematic Design

2.1 Package and Device Selection

AM13E230x MCUs are available in a wide range of package sizes and memory configurations. Each package is pin-to-pin compatible with either STM32G4 or STM32H5 MCUs to enable drop-in migration at the hardware and system level. Full migration details can be found in the *STM32G474x to AM13E230x Migration Guide.* The package sizes and configurations are detailed in the following table.

Table 2-1. AM13E230x Device Package Sizes

Package	STM32 Compatibility	Package Size	Pitch	Pin Layout	Analog IO	Digital IO	Pin Count
LQFP128 (PDT) (1)	STM32G4	14x14mm^2	0.4mm	32x32	44	107	128
LQFP100_G (PZ)	STM32G4	14x14mm^2	0.5mm	25x25	44	86	100
LQFP100_H (PZ)	STM32H5	14x14mm^2	0.5mm	25x25	43	85	100
LQFP80 (PN)	STM32G4	12x12mm^2	0.5mm	20x20	39	66	80
LQFP64_G (PM)(2)	STM32G4	10x10mm^2	0.5mm	16x16	27	52	64
LQFP64_H (PM)	STM32H5	10x10mm^2	0.5mm	16x16	26	52	64
LQFP48 (PT)	STM32G4	9x9mm^2	0.5mm	12x12	21	38	48
QFN48 (RGZ)	STM32G4	7x7mm^2	0.5mm	12x12	22	42	48 + PWRPAD

(1) Used on AM13E230-SOM-EVM.
(2) Used on LP-AM13E230.

Package size should be selected based off of IO requirements and PCB size. The SysConfig tool can be helpful in experimenting with different device package sizes and IO counts to determine the appropriate selection.

AM13E230x MCUs come in three different configurations that determine the device flash and memory sizes. Each configuration is available in the package sizes listed in the following table.

Table 2-2. AM13E230x Configurations

Part Number	Flash Size	SRAM Size
AM13E23019(1)	512KB	128KB
AM13E23018	256KB	96KB
AM13E23017	128KB	32KB

(1) Used on both AM13E230x EVMs.

Configuration should be selected based on application size and needs.

2.2 Digital Peripherals

This section details the design guidelines to follow for the digital peripherals on the AM13E230x MCU.

2.2.1 GPIO

The AM13E230x microcontrollers contain varying numbers of general purpose I/O (GPIO) pins depending on the package size. All digital I/O pins on the device (i.e. pins not reserved for device power/ground) can be used as general purpose I/O when configured in mux mode 0.

The GPIO pins serve as the digital inputs and outputs of the device, and these GPIO-enabled pins can be configured to be used either as typical GPIOs or as peripheral I/O signals using the device PinMux. This design grants great flexibility when using the AM13E230x devices in different applications. Up to 15 independent digital peripheral signals are multiplexed on a single GPIO-enabled pin, and the same peripheral can be multiplexed onto multiple GPIO pins. Refer to *Multiplexed Peripherals* for additional details.

For each GPIO pin, the max drive strength (sink/source current) is 4 mA. The maximum toggling frequency and rise/fall time is dependent on the IO Structure (SDIO, HDIO, or HSIO), the drive strength, and the supply voltage. Refer to the *Digital IO* section in the device-specific data sheet for full specifications.

At reset, the GPIO pins are in a high-impedance state. Internal pull-up/pull-down resistors are selectively enabled or disabled through software. This means that any signals that require a defined state during power up should have external pull resistors, such as chip selects.

In addition to configuring the pin selection of the device, it is also essential to be aware of best practices when making use of the general purpose I/O (GPIO) resources on the device. AM13E230x devices integrate onboard analog peripherals, like ADCs, DACs, PGAs, and CMPSSs, which help to reduce system level cost. These additional peripherals, however, lead to reduced GPIO availability when optimizing a system to use the smallest MCU package possible. Thus, it is important to maximize GPIO usage when designing a custom system.

2.2.2 XBARs

As described in the GPIO section, each peripheral signal is multiplexed to many GPIO pins in order to ease the design and layout process of an AM13E230x system and allow for maximum flexibility in IO configuration.

To route the signals from a GPIO to any of the different peripheral blocks – such as ADCs, eCAPs, MCPWMs, and external interrupts, the device has an input crossbar (XBAR) system. The Input XBAR has access to every GPIO and can route each signal to any (or multiple) of the peripheral blocks. Input XBARs enable the ability to route the output of one peripheral to another.

AM13E230x MCUs also have a GPIO Output XBAR, which takes signals from inside the device and brings them out to any GPIO.

PWM XBARs are responsible for routing signals from any pin into the MCPWM module.

The XBARs can be configured using the SysConfig tool.

2.2.3 EPI

The External Peripheral Interface (EPI) is a high-speed parallel bus for external peripherals or memory devices. A variety of memories and peripherals can interface with the EPI module. The following table shows the various supported configurations with the maximum frequency.

Table 2-3. AM13E230x EPI Interface Options

Interface	Maximum Frequency
Single SDRAM	50MHz
Single SRAM	50MHz
Single PSRAM without iRDY signal use	50MHz
Single PSRAM with iRDY signal use	50MHz
FPGAs, CPLDs, others using general-purpose mode	50MHz
Memory configurations with 2 chip selects	50MHz
Memory configurations with 4 chip selects	50MHz

The *EPI* chapter in the Technical Reference Manual details how the AM13E230x EPI peripheral connects to each of these interfaces.

Design Guidelines to Follow:

- Place the target device (memory IC/FPGA) close to the MCU to keep trace lengths short
- Use 50Ω single-ended traces to control impedance
- Minimize reflections and crosstalk by routing signal groups on the same layer and minimize vias/layer transitions
- Match the following trace lengths to reduce timing skew:
  - Data bus: Match within +/-25mils
  - Address/Command signals: Match within +/-25mils
  - Control signals: Match within +/-25-50 mils
  - Clock signals: Match within +/-5-10mils to the longest data trace
- Route address/command signals in parallel
- Avoid stubs and keep routes as direct as possible
- Consider series termination resistors (22-33Ω) for data and clock lines, placed close to the transmitter

2.2.4 MCAN

Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN (Modular CAN) peripheral on AM13E230x MCUs supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices can coexist on the same network without any conflict, provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

In order to connect the AM13E230x MCU to a CAN network, a CAN transceiver must be implemented to serve as the physical layer between the CAN controller (AM13E230x MCU) and the CAN bus. At a high level, the MCAN_RX and MCAN_TX pins connect to the RX and TX pins on the transceiver, respectively. Additional signals may be required as control I/O for the CAN transceiver.

The AM13E230x LaunchPad implements the TCAN3414 transceiver for connecting the system to a CAN bus network. The TCAN3414 transceiver operates from a single 3.3V supply and can operate in CAN and CAN-FD networks up to 8Mbps. For more details on the TCAN3414, refer to the TCAN3414 Data Sheet.

A reference design circuit from the LaunchPad is shown in the following figure.

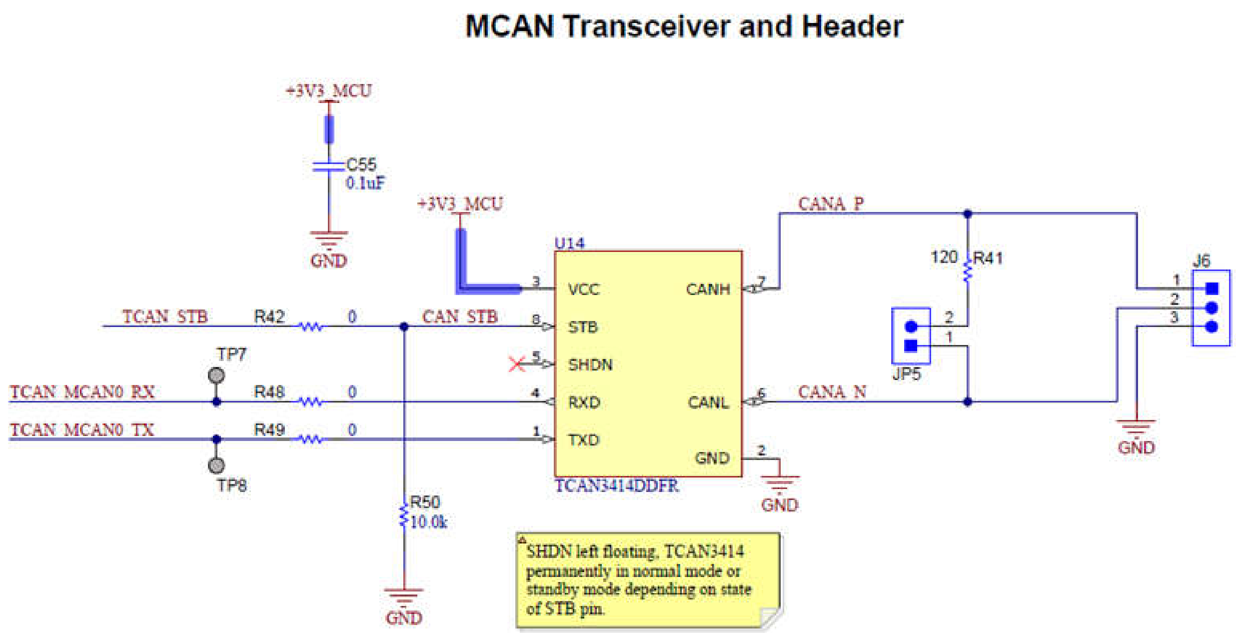


Figure 2-1. LP-AM13E230 MCAN Implementation

Any device GPIO can be used for the STB and SHDN pins. A pull resistor is recommended to keep the transceiver in a known state during power-on.

Transceiver-specific design requirements can be found in the device-specific data sheet.

When using MCAN, it is recommended to implement an external oscillator on the board (XTAL) to clock the AM13E230x device as opposed to using the internal oscillator (SYSOSC). Depending on the required CAN parameters like bit time settings, bit rate, bus length, and propagation delay, the accuracy of the on-chip oscillator may not meet the requirements of the CAN protocol.

2.2.5 UNICOMM

The UNICOMM module is a run-time configurable peripheral capable of supporting UART, I2C or SPI interfaces. Unlike typical MCUs that have separate peripheral blocks for these three communication peripherals, AM13E230x devices have six unified serial communication peripherals capable of operating in these different protocols.

Each UNICOMM instance can be configured to operate in one of the following modes:

- UART – Universal Asynchronous Receiver/Transmitter
- SPI – Serial Peripheral Interface
- I2CC – Inter Integrated Circuit Controller
- I2CT – Inter Integrated Circuit Target

UNICOMM instances are referred to using the abbreviation UCx (x being the instance number), followed by the signal types available on the specific interface.

Table 2-4. UNICOMM Signals by Peripheral Type

UNICOMM Signal Name	UART	I2C	SPI
UCx_RTS_POCI	RTS: Release To Send		POCI: Peripheral Out-Controller In
UCx_RX_SCL_SCLK	RX: Receive	SCL: Clock	SCLK: Clock
UCx_TX_SDA_PICO	TX: Transmit	SDA: Data	PICO: Peripheral In-Controller Out
UCx_CTS_CS0	CTS: Clear To Send		CS0: Chip Select 0

The six UNICOMM instances have different configuration options and peripheral types available depending on the instance. The details are shown in the following table.

Table 2-5. UNICOMM Configurations per Instance

UNICOMM Instance	Supported Serial Protocols	Available Peripheral Types1
UC0	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
UC1	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
UC2	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target
UC3	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
UC4	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
UC5	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target

The peripheral types are defined in each of the respective sections following this chapter.

The protocol selection for a given UNICOMM peripheral instance is done at a register level. Because of this low-level configuration, it is highly recommended that a designer implementing UNICOMM blocks in their application utilizes the SysConfig tool to configure each UNICOMM instance. This can help avoid configuring incorrect instance/peripheral combinations and ensure that the correct device pins are assigned to each instance.

For more information on configuring UNICOMM peripherals, refer to the UNICOMM Section in the *Technical Reference Manual.*

2.2.5.1 UART

UNICOMM instance selection must consider what features are desired on the peripheral. The table below compares the two UNICOMM UART types available on AM13E230x devices.

Table 2-6. UNICOMM UART Type Comparison

UNICOMM Instances	UART Type	Features
UC0, UC1, UC3, UC4	Basic UART	Includes additional support for ISO7816 Smart Card standard
UC2, UC5	Basic+ UART	Includes additional support for LIN (Local Interconnect Network)

If LIN functionality is required, UC2 or UC5 must be allocated for this peripheral assignment. If typical UART is acceptable for the application, any of the UCx instances can be used.

2.2.5.2 I2C

The UNICOMM I2C instances on the device can be configured as UNICOMM-I2CC (controller) or UNICOMM-I2CT (target). The controller/target configuration should be done using the SysConfig tool. The table below compares the two UNICOMM I2C types available on AM13E230x devices.

Table 2-7. I2C Comparisons

UNICOMM Instances	I2C Type	Controller Features	Target Features
UC0, UC1, UC3, UC4	Basic I2C	Digital glitch suppression	
UC2, UC5	Advanced I2C	• Analog glitch suppression • Burst mode • SMBus support (PEC, timeout detection)	• Analog glitch suppression • SMBus support (PEC, timeout detection, enhanced ACK features, default device/host/alert response addresses, target arbitration) • Secondary target address & mask

When configured as I2C, UNICOMM I2C signals SCL and SDA both require external pull-up resistors. The strength of the pull-ups is dependent on the I2C speed, however 2.2kΩ-4.7kΩ are typically acceptable for most implementations.

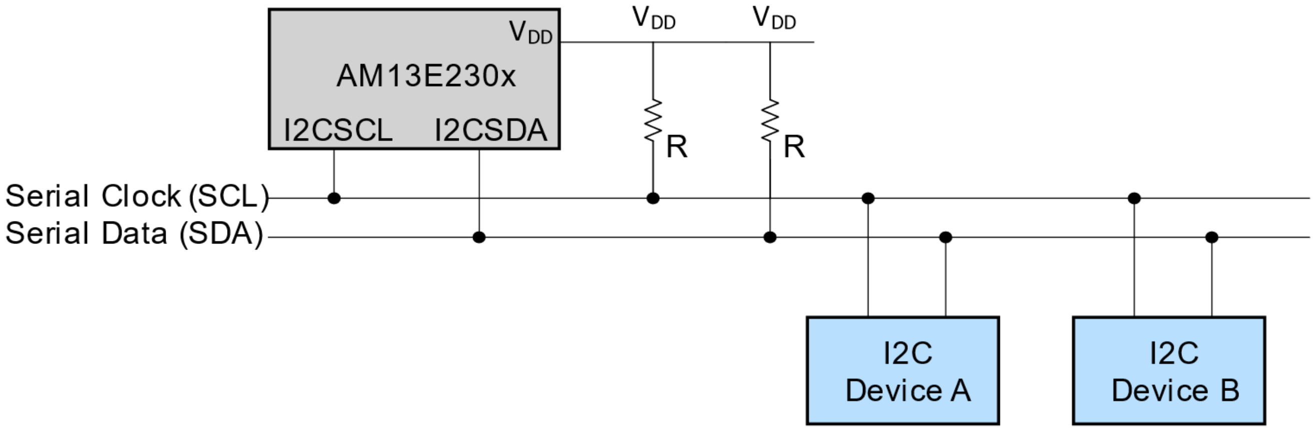


Figure 2-2. Typical I2C Bus Connection

2.2.5.3 SPI

AM13E230x UNICOMM SPI supports 3 or 4-wire configurations for connecting an external SPI device.

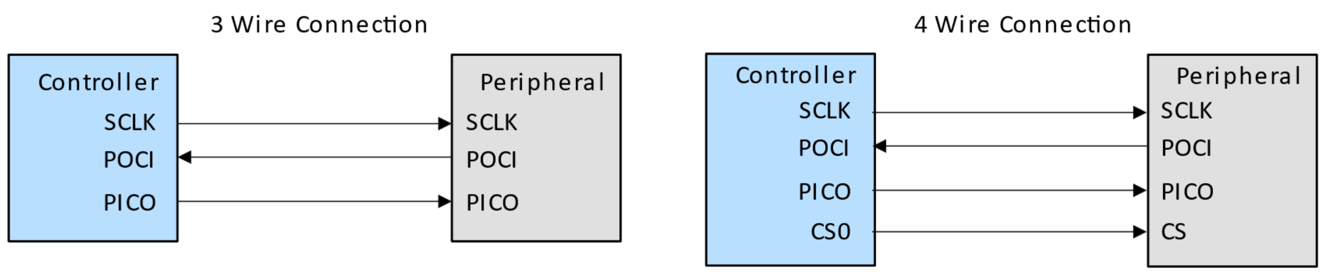


Figure 2-3. Typical SPI Connections

SPI can only be configured on UC0, UC1, UC3, or UC4.

A pull-up resistor is recommended on the Chip Select signal to keep the target device unselected until the AM13E230x drives this signal low.

2.3 Control Peripherals

The AM13E230x devices contain varying numbers of the following control peripherals:

- Enhanced Capture (eCAP)
- Multi-Channel Pulse Width Modulator (MCPWM)
- Enhanced Quadrature Encoder Pulse (eQEP)

For specific control peripherals, their performance can be greatly impacted by the design of the board. Be sure to follow the layout guidelines outlined in the Layout Section to reduce unwanted noise and maximize performance.

2.3.1 eQEP and eCAP

Both eQEP and eCAP do not have dedicated pinmux mode options to connect these types of signals for the device pins. Instead, any GPIO can be configured to supply the eQEP or eCAP inputs by taking advantage of the device's Input XBAR.

For more information on configuring these peripherals, refer to the following sections in the Technical Reference Manual:

- Configuring Device Pins (eQEP)
- Configuring Device Pins for the eCAP
- XBAR

2.3.2 Timers

The General-Purpose Timers (TIMG) on the AM13E230x devices are timer counting modules that can be used for a variety of functions, such as measuring the input signal edge and period of a signal or generating output waveforms. The two timer instances, TIMG4 and TIMG12 are general-purpose timer modules with slightly different features.

Table 2-8. Timers

Instance	Power Domain	Counter Resolution	Prescaler	CCP Channels	External PWM Channels	Shadow Load	Shadow CCs	QEI/Hall Input Mode
TIMG4	PD1	16-bit	8-bit	2	2	Yes	Yes	-
TIMG12	PD1	32-bit	-	2	2	-	Yes	-

Refer to the Technical Reference Manual for more details on TIMG features.

2.4 Analog Peripherals

This section describes the critical design choices when implementing analog peripherals on the device.

AM13E230x devices feature the following analog peripherals:

- Analog to Digital Converter (ADC)
- Programmable Gain Amplifier (PGA)
- Temperature Sensor
- Comparator Subsystem (CMPSS)
  – Each CMPSS contains 8bit Digital to Analog Converter (DAC) and 2 digital filters
  – Some CMPSS contain buffered DAC OUT

2.4.1 Choosing Analog Pins

Several IO pins on AM13E230x devices offer flexible pin usage that includes configuration for both digital **and analog** functionality. The IO pins that offer analog inputs (ADC, PGA, CMPSS) are multiplexed with digital peripherals – there are no dedicated analog IO pins on the AM13E230x device, allowing for a wide range of pin configurations for a user application.

When choosing analog pin connections, take into consideration the peripherals available on each pin. Analog inputs with comparators allow for those analog signals to be able to quickly trip PWMs (as a fault signal) or to detect zero-crossing. Because these devices contain multiple ADCs, also consider if sampling certain analog signals simultaneously is beneficial. In these situations, three simultaneous analog signals could be connected to A0, A1, and A2.

2.4.2 Analog Voltage Reference

The on-device ADCs use the VREFHI and VREFLO pins as voltage reference inputs. For most applications, the internal voltage references offer sufficient performance. The VREFHI pin voltage is driven by an internal bandgap voltage reference whose voltage can be selected as a 1.65V output (0V to 3.3V) or a 2.5V output (0V to 2.5V). The reference value is programmable. If a higher accuracy reference voltage is required for a system design, an external reference voltage can be used.

Regardless of whether the internal or external reference is selected, a series of decoupling capacitors is required to be placed between the VREFHI and VREFLO pins.

- Bulk capacitor of 2.2uF
- 2x 0.1uF capacitors at the device pins

Note

128-pin AM13E230x devices require 3x 0.1uF capacitors, as there are two external VREFHI pins on this package. The two pins are connected internally, and do not require separate supplies.

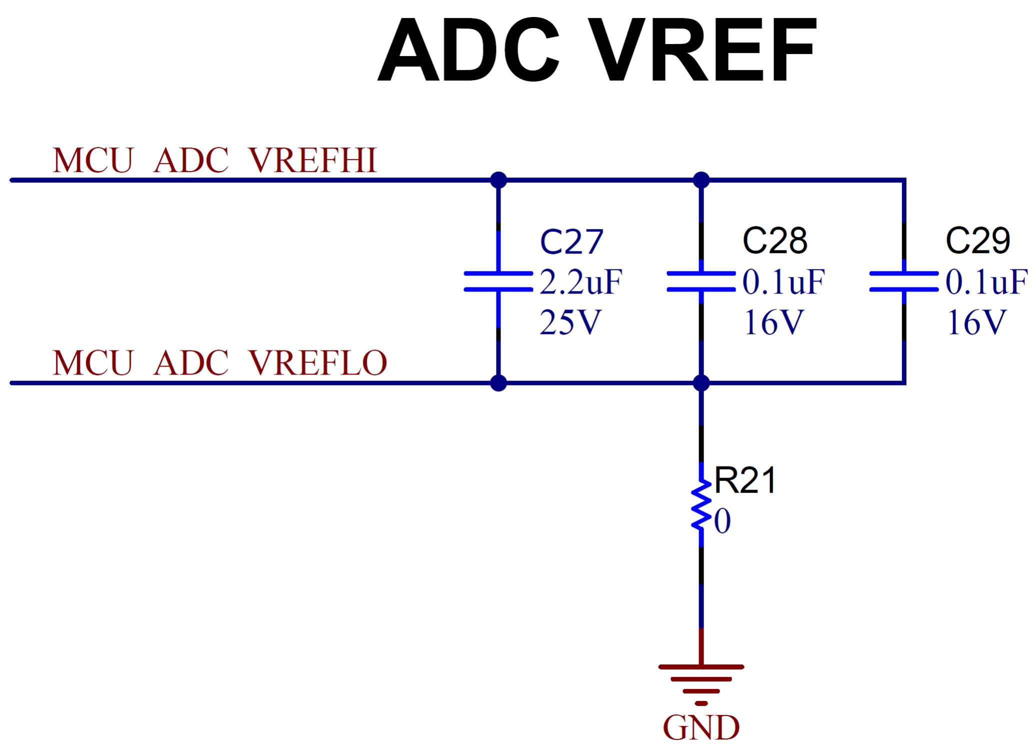


Figure 2-4. LP-AM13E230 VREF Decoupling

In most instances, VREFLO can be shorted to the system GND.

When using the internal reference mode, no additional voltage sources should be placed on the VREFHI pin as the voltage is driven onto this pin by the circuits on the device itself.

In external reference mode, drive the VREFHI pin using an external circuit or reference IC, such as REF3030 and a high-speed operational amplifier.

2.4.3 ADC Inputs

The ADCs should be properly designed and evaluated to ensure proper performance. The analog-to-digital converters have input impedance and bandwidth requirements which could lead to memory cross-talk and significant sample-and-hold (S+H) circuit settling errors.

The diagram below outlines the ADC Input Model, where Cp describes the parasitic input capacitance, Ron describes the sampling switch resistance, Ch describes the sampling capacitor, and Rs describes the nominal source impedance. The data sheet documents the ADC per-channel parasitic capacitances that can help in deciding which ADCs to use. Note that the acquisition window duration can be adjusted for each SOC by adjusting ACQPS or lowering the sampling frequency, or a combination of both. To evaluating the driving circuit, simulate it in TINA-TI to ensure correct performance and settling.

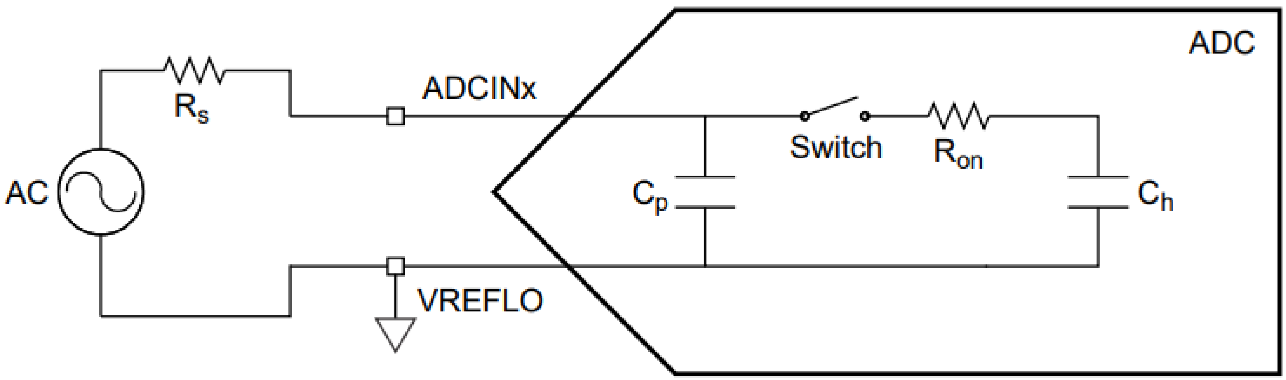


Figure 2-5. ADC Input Model

2.5 Multiplexed Peripherals

AM13E230x devices have a large number of multiplexed digital and analog I/O present on almost all of the MCU pins. For this reason, designers are highly recommended to make full use of the TI System Configuration tool (SysConfig) to experiment and plan different pin multiplexing scenarios before committing the design to hardware. The resulting SysConfig pin multiplexing configurations can be used for schematic capture and layout reference, as well as software driver development.

For more details, refer to the SysConfig tool page and *IOMUX* chapter in the Technical Reference Manual.

2.6 Power

AM13E230x MCUs have two main device power nets:

- VDD: 3.3V digital supply
- VDDA: 3.3V analog supply

VDD and VDDA are connected at the board level. When designing an AM13E230x system, it is expected that the same power supply being used for VDD is also connected to VDDA. The VDD and VDDA nets should be separated by a ferrite bead.

2.6.1 Discrete Power Solution

A single discrete 3.3V supply is recommended to provide the required power to the AM13E230x MCU.

Both the AM13E230x LaunchPad and controlSOM designs integrate a single LDO regulator for the 3.3V VDD/VDDA power rails. The TLV75733 1-A, low-IQ high-accuracy LDO is implemented in the EVM designs. This small-size regulator is recommended for powering the AM13E230x core, I/O, and peripherals as it has a small PCB footprint and can provide up to 1A. The TLV757P family of LDOs offers other options for current output, and can be explored if the PCB system has a smaller load requirement.

In practice, any 3.3V LDO can be used to power the AM13E230x as long as the following minimum requirements are fulfilled:

- Vout: 3.3V
- Iout: 300mA

Note

The AM13E230x MCU is expected to consume a maximum of 250mA. The additional 50mA allows for powering other on-board devices using the same LDO.

Many DC-DC regulators can be matched to fit these requirements and maximum power consumption. The TLV75733 implementation on the AM13E230x controlSOM is shown below:

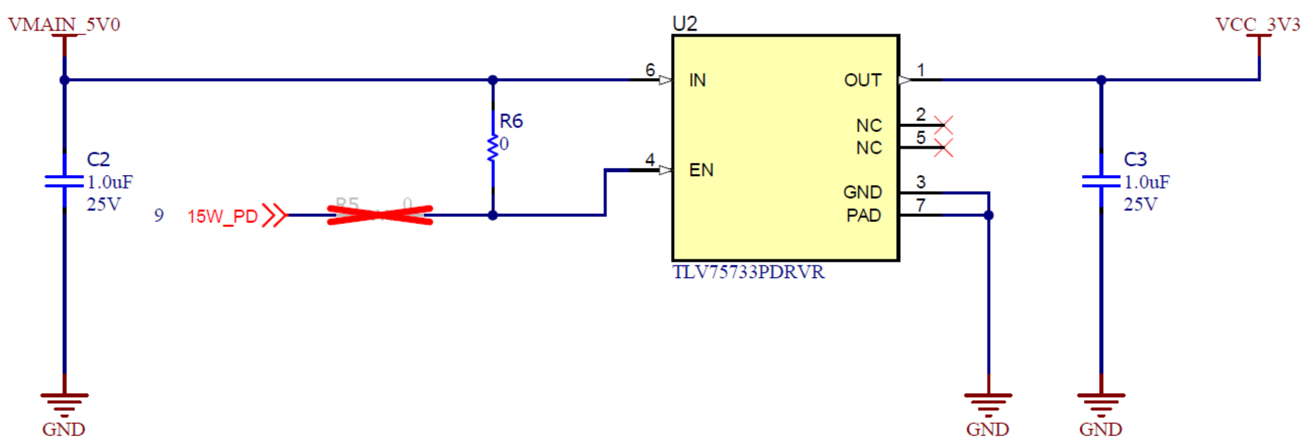


Figure 2-6. AM13E230x controlSOM LDO Implementation

The ENABLE pin can be driven by other system power sequencing requirements or power-good signals from upstream regulators. On the controlSOM, the output of a 15W power delivery handshake circuit can be used to enable the LDO.

2.6.2 Power Decoupling and Filtering

The following table describes the initial decoupling and power filtering required for each AM13E230x package.

Table 2-9. Power Filtering

MCU Supply	Quantity								Comment
	128 PDT	100_G PZ	100_H PZ	80PN	64_G PM	64_H PM	48 PT	48 RGZ	

Table 2-9. Power Filtering (continued)

VDD	1	1	1	1	1	1	1	1	2.2uF, 0402, X5R
	8	5	5	5	4	4	4	4	0.1uF, 0201, X7R
VDDA	1	1	1	1	1	1	1	1	2.2uF, 0402, X5R
	2	2	1	2	2	1	1	1	0.1uF, 0201, X7R
	1	1	1	1	1	1	1	1	Ferrite Bead

As a general rule, the power decoupling for any package of the AM13E230x MCU should follow these guidelines:

- 2.2uF bulk capacitor placed at the source of the power net
- 0.1uF capacitors placed as close as possible to each VDD/VDDA pin on the MCU
  - The number of 0.1uF capacitors required is dependent on the number of VDD/VDDA pins on the MCU package
- A ferrite bead is required to filter the VDDA net from the VDD net

The figures below show the decoupling placement and routing for the 64-pin PM package (LaunchPad).

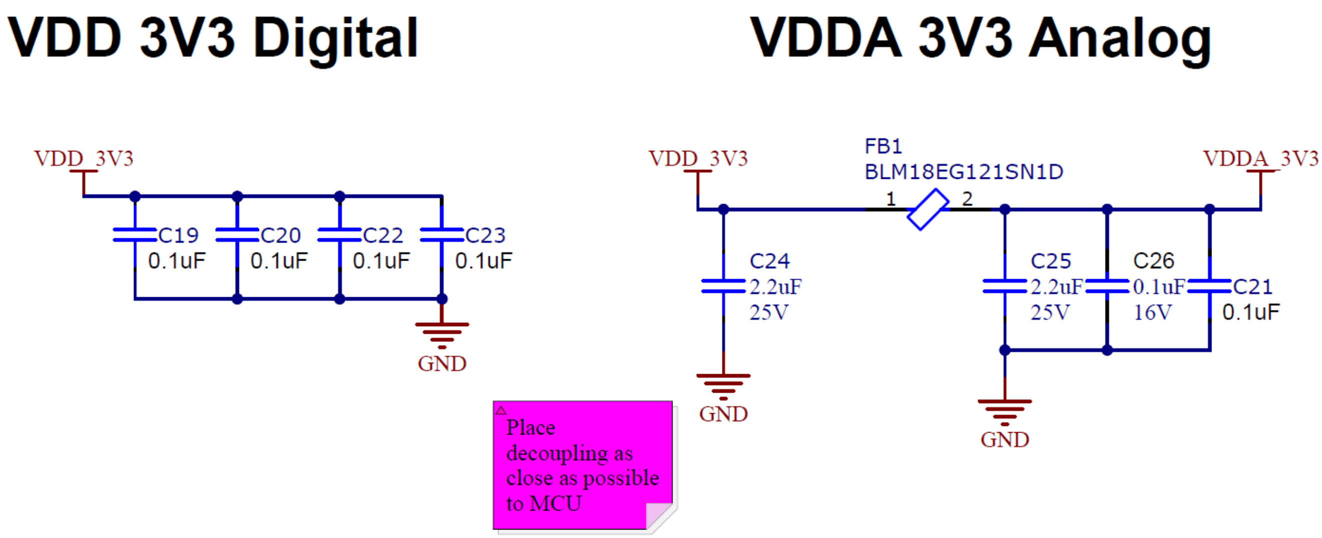


Figure 2-7. LP-AM13E230 Power Decoupling Schematic

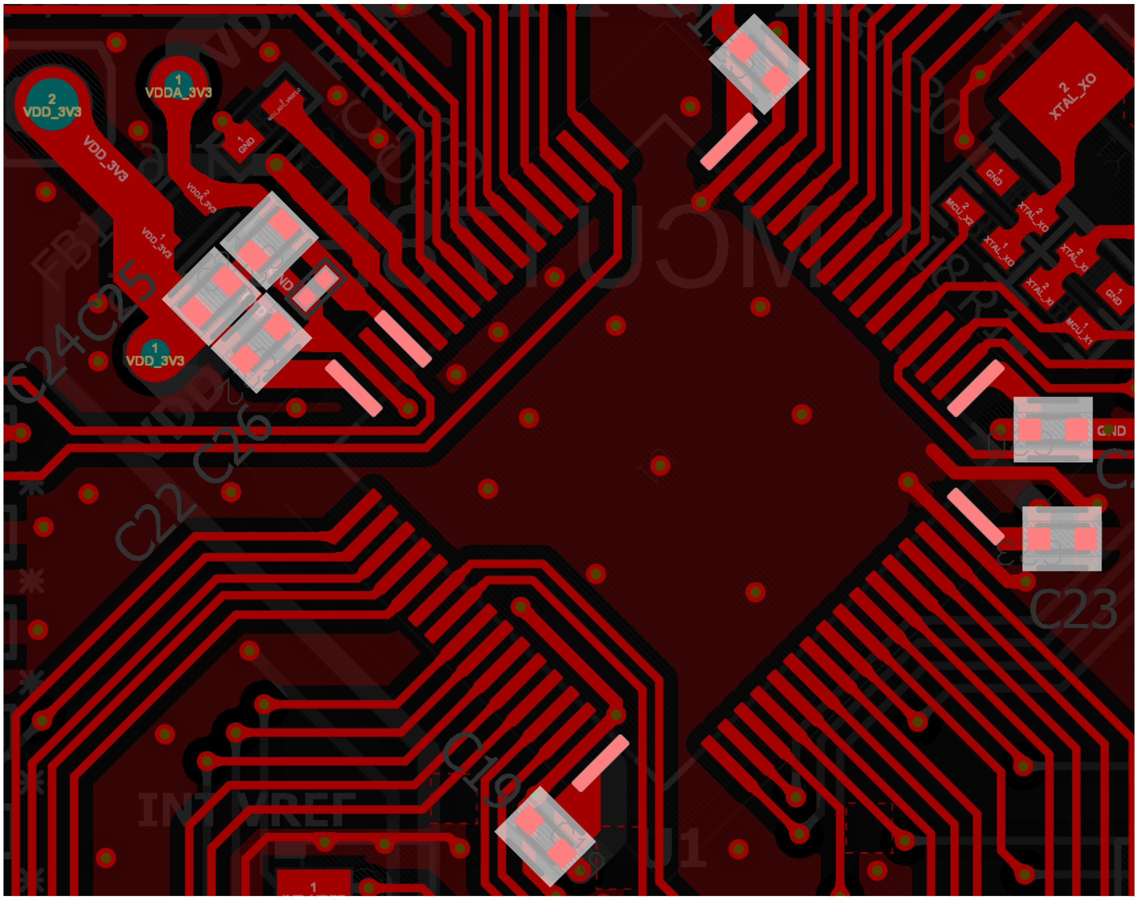


Figure 2-8. LP-AM13E230 Power Decoupling - Top Layer

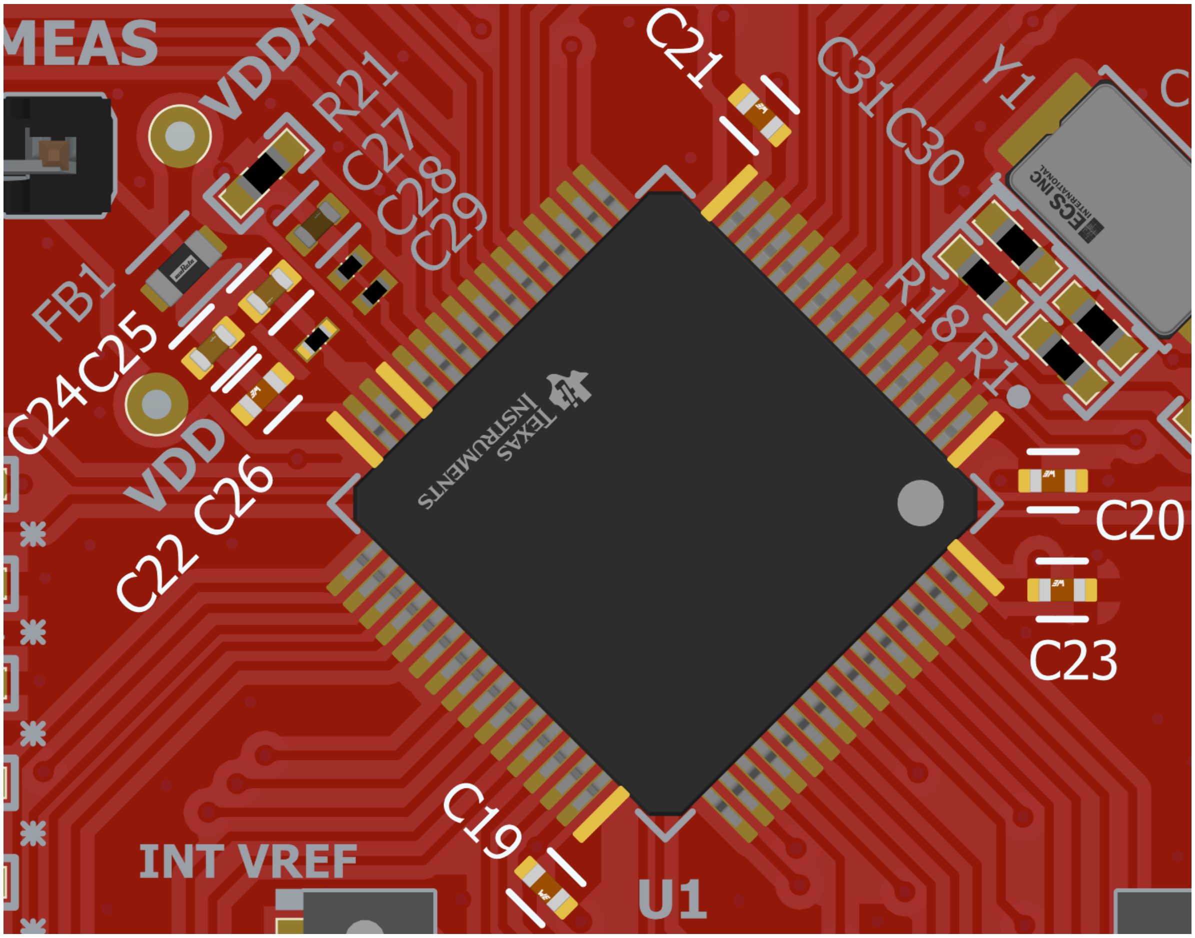


Figure 2-9. LP-AM13E230 Power Decoupling Placement – 3D View

2.6.3 Analog Voltage Reference

The AM13E230x MCU has dedicated pins for the ADC voltage HIGH (VREFHI) and LOW (VREFLO) reference inputs. VREFLO is to be shorted to GND.

There is additional decoupling required between these pins, regardless of whether the internally generated reference or external reference is implemented. To use the internally generated reference, simply connect the decoupling between the VREFHI and VREFLO nets. To apply an external reference, connect the supply to the VREFHI pin.

The following table describes the decoupling required for the device analog voltage reference nets per package.

Table 2-10. AM13E230x ADC VREF Decoupling

MCU Supply	Quantity								Comment
	128 PDT	100_G PZ	100_H PZ	80PN	64_G PM	64_H PM	48 PT	48 RGZ	
VREFHI	1	1	1	1	1	1	1	1	2.2uF, 0402, X5R
	3	2	3	2	2	2	2	2	0.1uF, 0201, X7R

Note

Some AM13E230x MCU packages have more than one VREFHI pin. These pins are internally connected and do not require a separate supply net.

The analog voltage reference decoupling must follow these guidelines:

- 2.2uF bulk capacitor
- 0.1uF capacitors placed as close as possible to each VREFHI pin on the MCU
  - The number of 0.1uF capacitors required is the number of VREFHI pins present on the device +1
- The decoupling network must be placed in order to minimize the loop and trace lengths between VREFHI and VREFLO
- VREFLO is to be shorted to GND in most cases

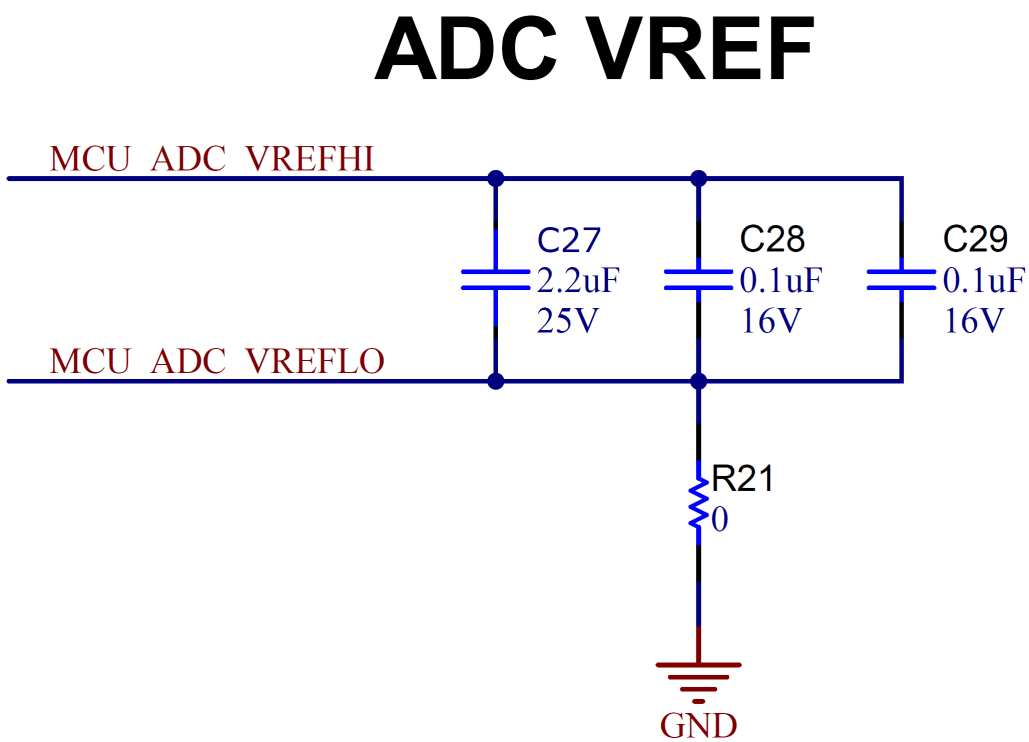


Figure 2-10. AM13E230x VREF Decoupling Schematic

The below figures show the decoupling placement and routing for the 64-pin (PM) package on the AM13E230x LaunchPad:

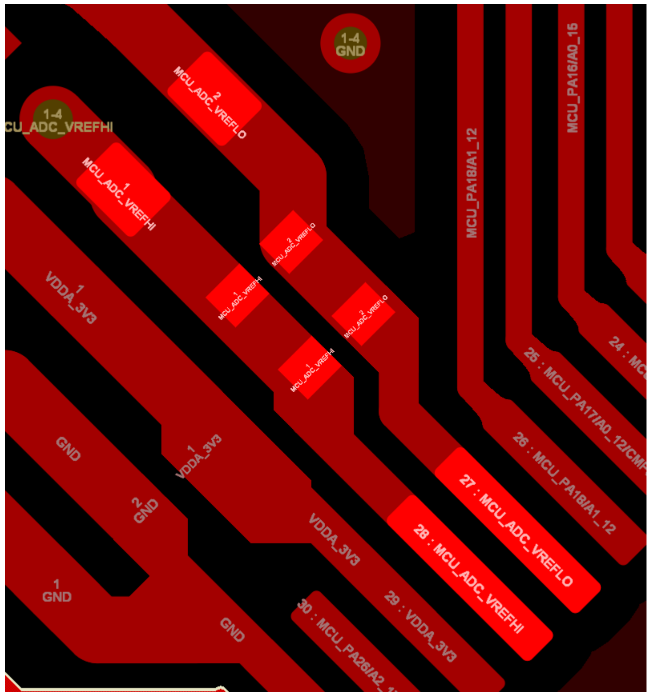


Figure 2-11. Analog VREF Decoupling – LP-AM13E230 Top Layer

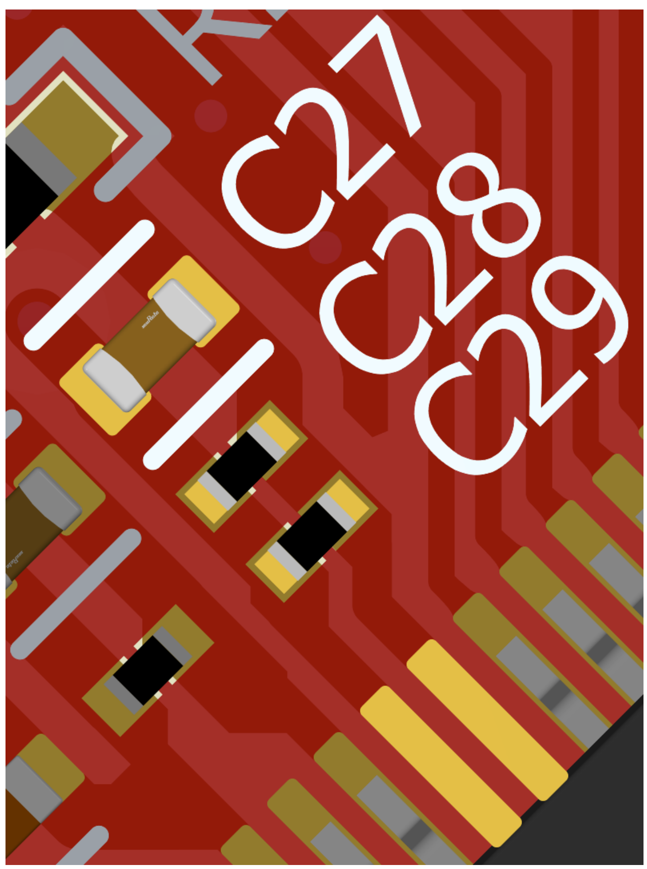


Figure 2-12. Analog VREF Decoupling – LP-AM13E230 3D View

2.6.4 VSS/VSSA

The VSS and VSSA pins on the AM13E230x MCU are to be shorted to GND. Vias to inner GND layers/planes are recommended to be placed as close as possible to the device VSS/VSSA pins.

2.6.5 Power Consumption

The estimates in the below table are based on initial power simulations of the device when operating at XX device temperature. For the latest characterized peak power values, reference the device-specific data sheet.

A use-case based Power Estimation Tool (PET) is provided for AM13E230x MCUs.This tool can help further bound the peak power based on specific peripheral utilization. The PET can be downloaded from the AM13E230x product page.

Table 2-11. Power Consumption

Device Supply Net	Peak Current (mA)	Supply Description
VDD	TBD	3.3V digital
VDDA	TBD	3.3V analog

2.7 Reset

There are several AM13E230x MCU pins associated with different types of reset activity.

For more information on device resets, see the *Resets and Device Initialization* section in the Technical Reference Manual.

2.7.1 nRST Pin

The nRST pin is the main interface for triggering a complete device reset. When designing an AM13E230x PCB system, the following design guidelines must be followed:

- The nRST pin must be HIGH for the device to boot successfully after powering up (cold start) as there is no internal pull-up on the nRST pin
- External circuitry, either a 10kΩ pull-up to VDD or a reset control circuit must actively pull nRST HIGH for the device to start

On the AM13E230x EVMs, this is accomplished simply by pulling the nRST net up to 3.3V using a 10kΩ resistor.

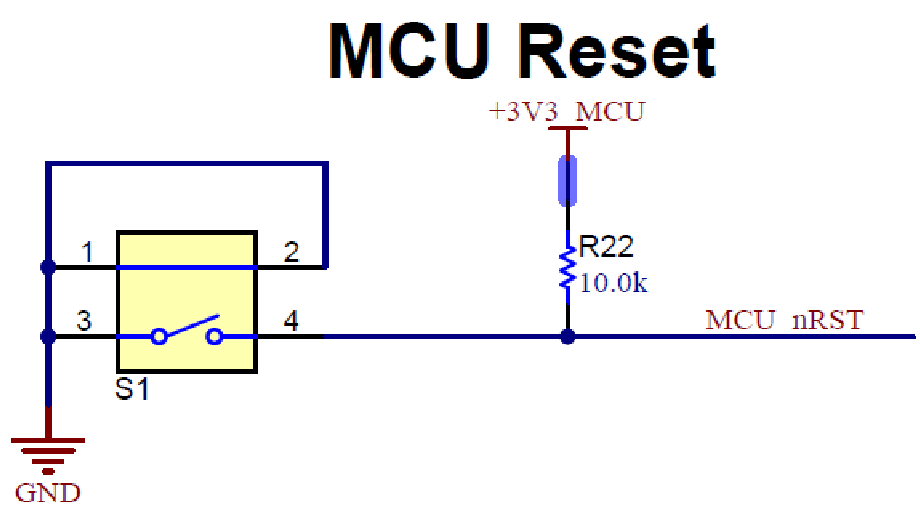


Figure 2-13. LP-AM13E230 nRST Circuit

The pushbutton S1 pulls the nRST line LOW when pressed, and triggers a different type of reset depending on how long the reset is asserted.

- A low pulse on nRST <1 second triggers a BOOTRST
- A low pulse on nRST >1 second triggers a POR

For more details on BOOTRST and POR, see the *Reset Levels* section in the Technical Reference Manual.

2.7.2 BSL Invoke Pin

The AM13E230x Bootloader can be invoked through a software application or through hardware using a GPIO pin. The device boot ROM configures pin PA6 by default for invoking the Bootstrap Loader (BSL) through hardware. If using this method to invoke the BSL, this signal needs to be pulled down with a 10kΩ resistor when the device comes out of reset. To invoke the BSL, this signal needs to be driven high.

On the AM13E230x LaunchPad, this is accomplished using a simple push button circuit:

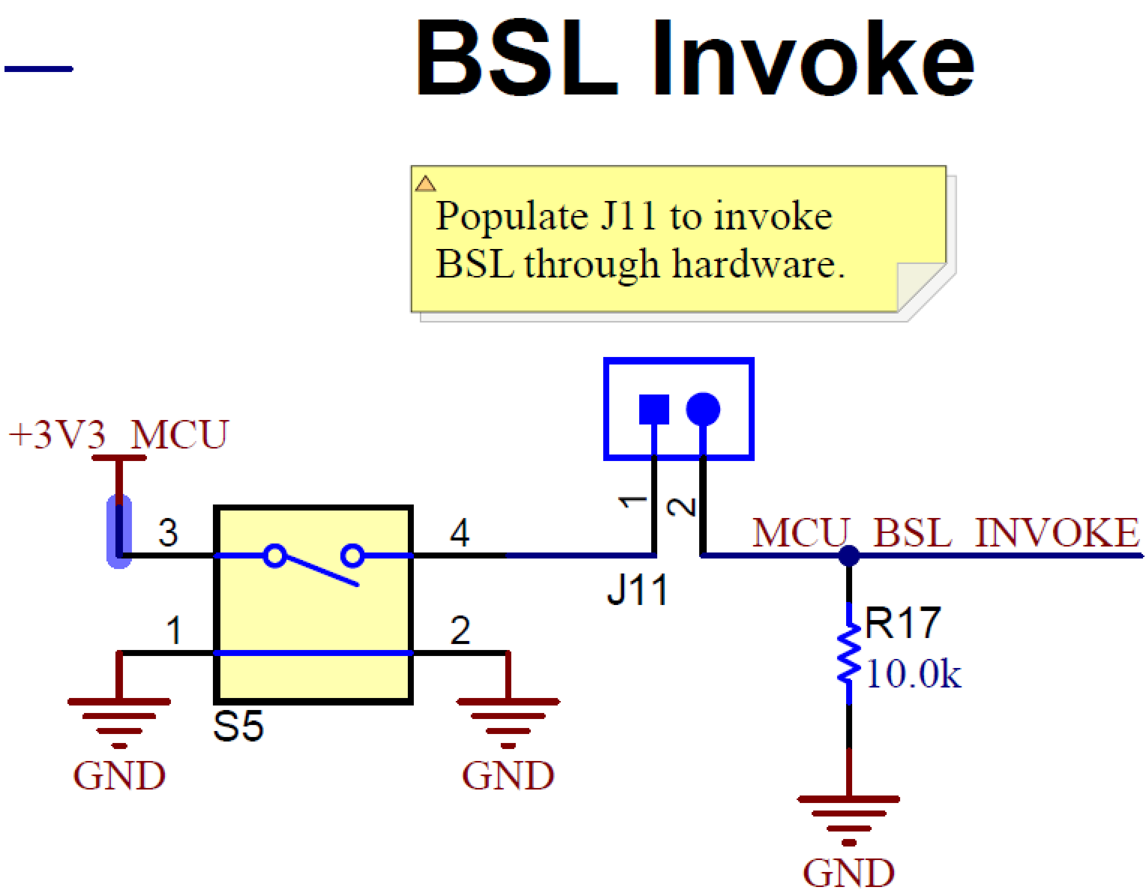


Figure 2-14. BSL Invoke Circuit

2.7.3 WAKE from LPM Pins

Waking the AM13E230x device from a Low Power Mode can be triggered from the rising or falling edge of an input signal to a GPIO pin. The GPIO pins that can be utilized for this purpose are dependent on which LPM the device is exiting and returning to RUN mode.

2.7.4 WAKE From STOP/STANDBY Modes

Waking the MCU from STOP or STANDBY modes can be done using any GPIO pin. The Fast Wake feature of the MCU allows the GPIO module to stay in a low-power state and detect interrupt events on the GPIO pins without requiring a high-speed clock. For more information on configuring GPIO Fast Wake from STOP or STANDBY modes, see the *GPIO Fast Wake* section in the Technical Reference Manual.

2.7.5 WAKE from SHUTDOWN Mode

A specific set of GPIO pins includes additional wakeup logic to wake the device from SHUTDOWN mode. In SHUTDOWN mode, the entire regulated core supply of the device is disabled, and the device can only wake from these wake-capable I/Os. For more information on configuring SHUTDOWN mode wakeup logic, see the *SHUTDOWN Mode Wakeup Logic* section in the Technical Reference Manual.

On the AM13E230x MCU, the following GPIOs are capable of waking the device from SHUTDOWN:

Table 2-12. SHUTDOWN Wake-Capable GPIOs

WAKEUP Pin #	GPIO #
WAKEUP0	GPIO0
WAKEUP1	GPIO45
WAKEUP2	GPIO70
WAKEUP3	GPIO2
WAKEUP4	GPIO37
WAKEUP5	GPIO33
WAKEUP6	GPIO50
WAKEUP7	GPIO51

For package-specific pin assignments, refer to the device-specific Data Sheet.

2.7.6 AM13E230x Hardware Platform Examples

WAKEUP GPIOs can be configured to trigger a WAKE event on a rising or falling edge. On the AM13E230x EVMs, the following GPIOs are assigned for WAKE functionality:

Table 2-13. WAKEUP GPIOs on AM13E230x EVMs

EVM	WAKEUP Pin #	GPIO #	Interface
AM13E230x LaunchPad	WAKEUP1	GPIO45	Pushbutton (active LOW)
AM13E230x controlSOM	WAKEUP5	GPIO33	Pushbutton (active LOW)
	WAKEUP2	GPIO70	High-density connector (configurable)

2.8 Clocking

The AM13E230x X1 and X2 clock input pins can be sourced from either an attached crystal oscillator or a single-ended oscillator output. The MCU can also operate without an external clock source, relying on only the internal oscillators to generate the device clocks.

2.8.1 Internal Oscillators

The AM13E230x MCU can operate without an external reference crystal or oscillator. In this mode, the internal System Oscillator (SYSOSC) provides a 32MHz clock source to the system.

Note

If peripherals with specific timing requirements such as MCAN are being used in a design, this mode of operation is not recommended. Using an external oscillator provides the highest level of accuracy when providing a source to the device clocks.

When the XTAL operating mode is set to ‘off,’ the X1 and X2 pins are not expecting a clock input and can be used as GPIO80 and GPIO81, respectively. See the *SYSOSC* section in the Technical Reference Manual for more information on using the SYSOSC to clock the device.

2.8.2 External Crystal Oscillator (XTAL)

An external crystal or resonator can be used to generate a stable reference clock for the system. The crystal or resonator must be populated between the X1 and X2 device pins. Three types of external sources are supported as input to the X1 and X2 pins:

- External crystal connected across X1 and X2 with load capacitors connected to GND (10-25MHz)
- External resonator connected across X1 and X2 (10-25MHz)
- Single-ended 3.3V external clock or crystal connected to X1 (4-48MHz). X2 may be used as GPIO

The AM13E230x EVMs utilize an external 25MHz crystal, which is the suggested method of clocking the device to enable all features at full-speed. Load capacitors to GND must be placed on both the X1 and X2 nets between the crystal and the MCU. The load capacitors must be sized according to the specifications of the crystal being used. Damping resistors may be required on the X1 and X2 nets in order to suppress unwanted oscillations and protect the crystal from excessive drive current.

The default reference clocking mode for the AM13E230x EVMs is crystal mode. Both the LaunchPad and controlSOM use a 25MHz crystal oscillator (ECS-250-12-30-GM) connected to the AM13E230x device X1 and X2 pins to clock the device. 18pF load capacitors and 0Ω damping resistors complete the crystal circuit on the EVMs.

The following examples from the AM13E230x EVMs show proper crystal circuit routing.

- XTAL_IN routes to the X1 pin (GPIO80)
- XTAL_OUT routes to the X2 pin (GPIO81)

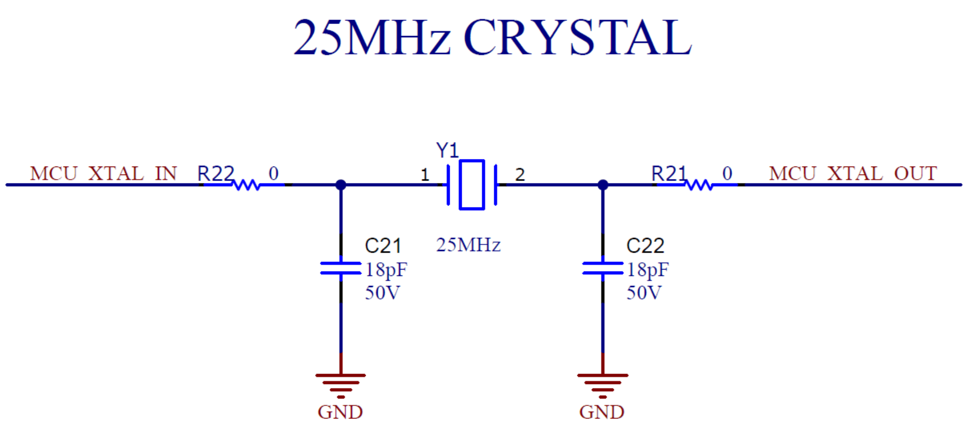


Figure 2-15. AM13E230x XTAL Circuit

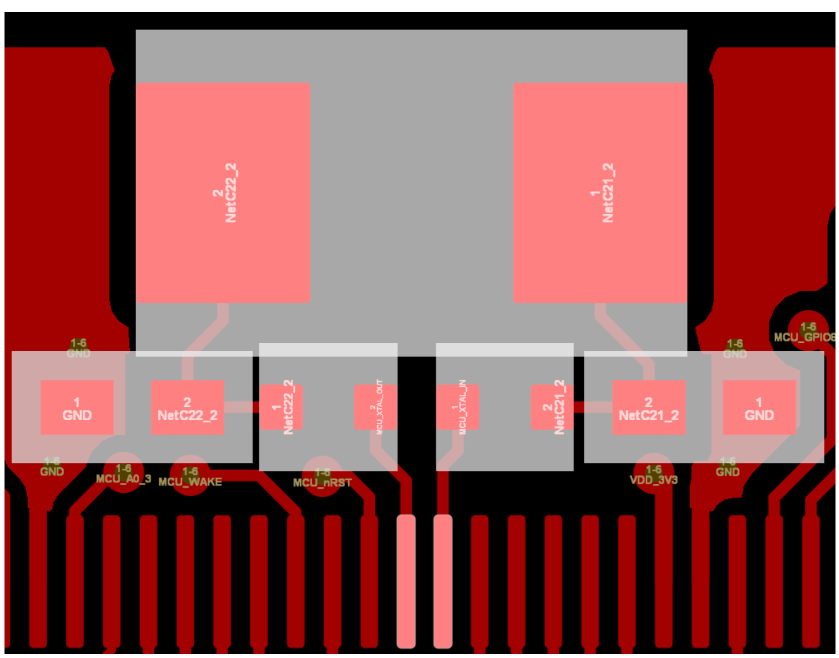


Figure 2-16. AM13E230x controlSOM Crystal Circuit - Top Layer

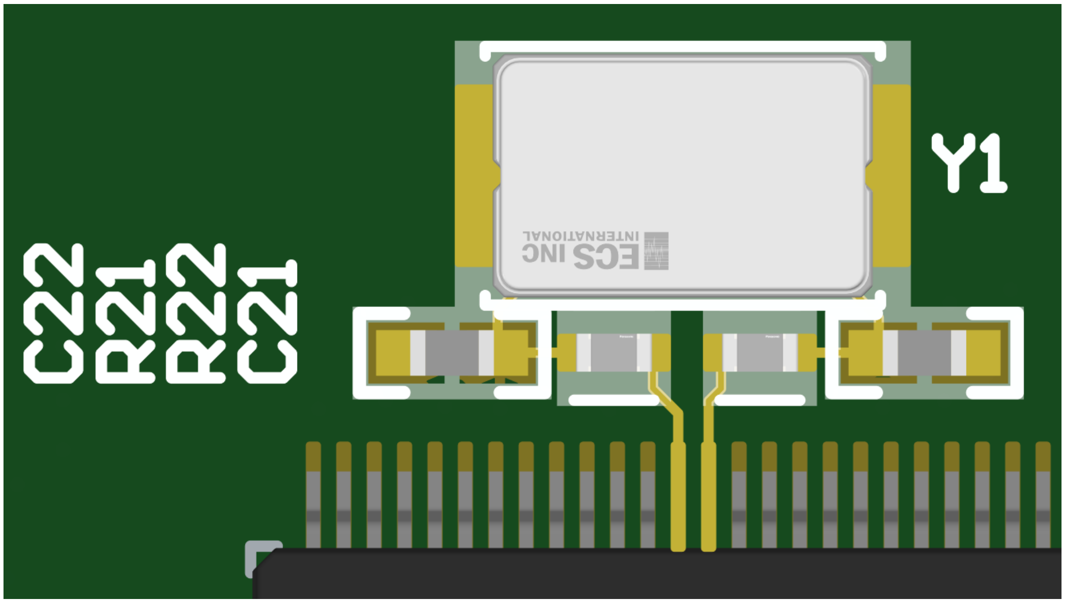


Figure 2-17. AM13E230x controlSOM Crystal Circuit - 3D View

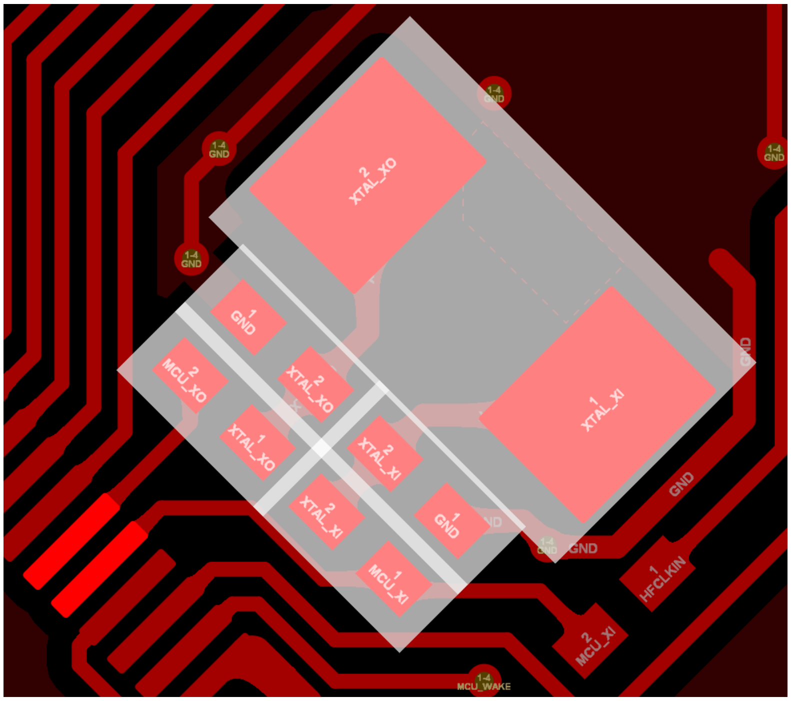


Figure 2-18. AM13E230x LaunchPad Crystal Circuit - Top Layer

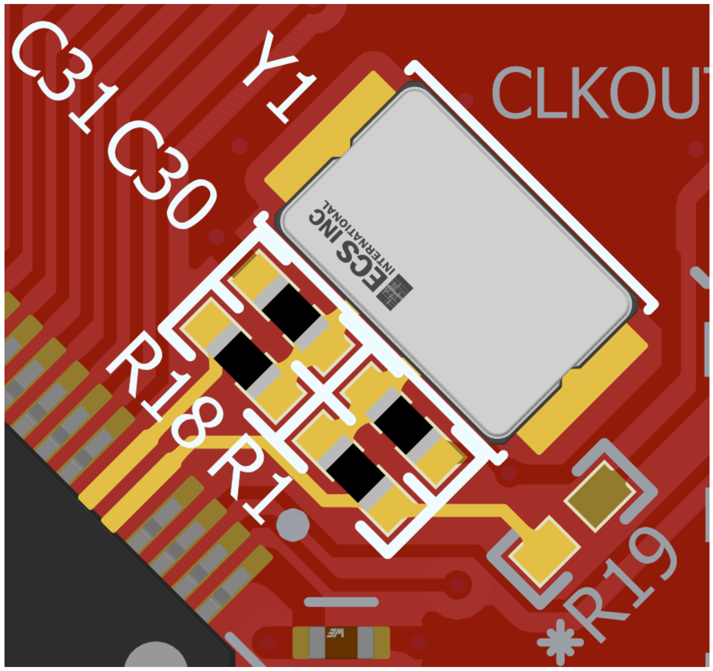


Figure 2-19. AM13E230x LaunchPad Crystal Circuit - 3D View

The following table details PCB routing guidelines when using a crystal oscillator.

Table 2-14. Crystal Routing Guidelines

Category	Guidelines
Placement	• Place the crystal as close as possible to the X1/X2 pins • Orient the crystal so that traces to the MCU are shortest and most direct • Keep the crystal away from high-speed signals, power supplies, and noisy digital signals • Place on the same layer as the MCU
Traces	• Keep traces as short as possible (ideally <10mm) • Traces to both crystal pins should be equal length • Use wider traces to reduce impedance • Avoid 90º angles, use 45º • Route on a single layer
Ground	• Place GND around the crystal circuit with multiple vias to a GND plane underneath the circuit
Load Capacitors	• Place load capacitors as close as possible to the crystal • Connect load capacitors directly to a solid GND plane with short traces
Isolation	• Do not route other signal traces directly under the crystal area • Do not route digital signals parallel to crystal traces

2.8.3 Digital Clock Input

A 4-48MHz digital clock signal can be used as the high-frequency clock source as an alternative to using a crystal oscillator. The AM13E230x IOMUX must be configured to enable the HFCLK_IN function on the appropriate device pin. For more information on configuring the device to use the HFCLK_IN function, see the *HFCLK_IN (Digital Clock)* section in the Technical Reference Manual.

HFCLK_IN is compatible with digital square wave CMOS clock inputs and should have a typical duty cycle of 50%. The AM13E230x LaunchPad includes an external header to connect a digital clock generator to evaluate this feature of the MCU.

Note

HFCLK_IN and XTAL are mutually exclusive and must not be enabled at the same time.

2.8.4 Output Clock Generation

The AM13E230x MCUs have a clock output unit (CLK_OUT) for sending digital clock signals from the device to external circuits or the device's Frequency Clock Counter (FCC). For more information on the FCC, see the *Frequency Clock Counter* section in the Technical Reference Manual.

Device pins configured to support the CLK_OUT function have a flexible set of sources to select and includes a programmable divider. For a full list of clock sources for CLK_OUT, see the *External Clock Output (CLK_OUT)* section in the Technical Reference Manual.

The AM13E230x LaunchPad includes an external header to connect an oscilloscope and measure an output clock signal.

2.9 Debugging and Emulation

The AM13E230x debug interfaces must be routed out to external headers for connecting an external debug probe to the device core, programming the device, and checking device health at platform bring-up.

AM13E230x MCUs support multiple classes of JTAG and Serial Wire Debug emulators. For out of box convenience, the AM13E230x LaunchPad design implements an on-board XDS110 emulator with JTAG and auxiliary UART-USB bridge implemented with a TI MSP432 MCU. The same XDS110 emulation scheme is interfaced with the AM13E230x controlSOM using the XDS110ISO-EVM debug probe. However, for custom, application-specific PCB systems, a simpler JTAG, SW-DP, or Trace debug header should be implemented in order to perform rapid prototyping and system programming while minimizing PCB footprint and additional on-board routing. This allows for external debug probes to be attached to the system as needed during development.

2.9.1 Debug Interfaces

2.9.1.1 JTAG and SW-DP

The JTAG and Serial Wire Debug Port (SW-DP) is a combined JTAG-DP and SW-DP that interfaces directly with a SWD or JTAG probe to connect to the device core. This interface, also referred to as SWJ-DP requires four pins to be routed out from the AM13E230x MCU:

- TDO (JTAG mode only)
- TDI (JTAG mode only)
- TMS/SWDIO (SWDIO for SWD mode, TMS for JTAG mode)
- TCK/SWCLK (SWCLK for SWD mode, TCK for JTAG mode)

For full JTAG signal definitions, see the *JTAG Debug Port (JTAG-DP)* section in the Technical Reference Manual.

For full SW-DP signal definitions, see the *Serial Wire Debug (SWD) Debug Port (SW-DP)* section in the Technical Reference Manual.

After the device powers on (cold start), the following pins are configured for JTAG/SWD mode to allow a debug connection to be established.

Table 2-15. JTAG/SWD Signal Pins

JTAG/SWD Signal	GPIO Pin Number	Pull-up/Pull-down
TDI	GPIO14	PU
TDO/SWD	GPIO15	PU
TMS/SWDIO	GPIO19	PU
TCK/SWCLK	GPIO13	PD

TI recommends the ARM Cortex 10-pin Debug Connector for interfacing an external debug probe with the AM13E230x MCU. This connector is compatible with most industry-standard debug probes and supports both JTAG and Serial Wire mode. For connector part number information, refer to the ARM Connector Documentation.

The AM13E230x LaunchPad includes this header (FTSH-105-01-L-DV-K) to connect an external debug probe.

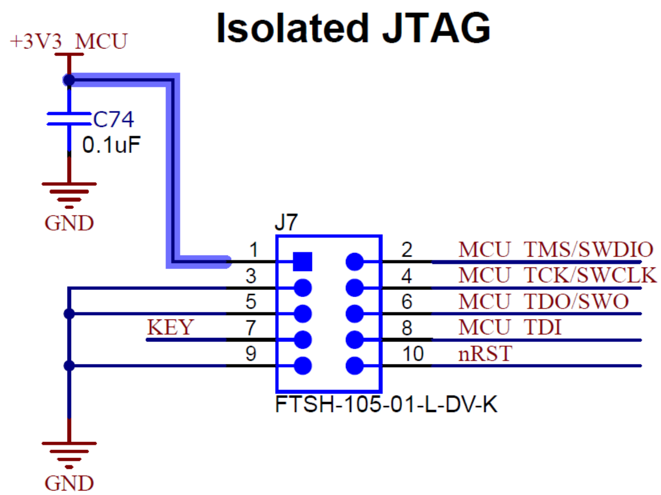


Figure 2-20. LP-AM13E230 Debug Header

When placing the JTAG header, the distance between the header and the MCU should be no longer than 6 inches. In instances where the MCU target and JTAG header are further than 6 inches apart or other devices are present on the JTAG chain, each JTAG signal should be buffered.

2.9.1.2 Trace

4-bit trace is supported on the 128 pin, 100G pin, and 100H pin packages of the AM13E230x MCU. The on-device Embedded Trace Macrocell (ETM) is used to stream a full-instruction program-counter trace with a 64-bit cycle-accurate timestamp counter. For more details on enabling the ETM, refer to the *External Trace (ETM)* section in the Technical Reference Manual.

TI recommends the ARM Cortex 20-pin Debug+ETM Connector for interfacing with the ETM signals. This connector also supports JTAG and SW-DP interfaces on separate pins. For part number information, refer to the ARM Connector Documentation.

The AM13E230x controlSOM includes this header (FTSH-110-01-L-DV-K) to connect an external probe.

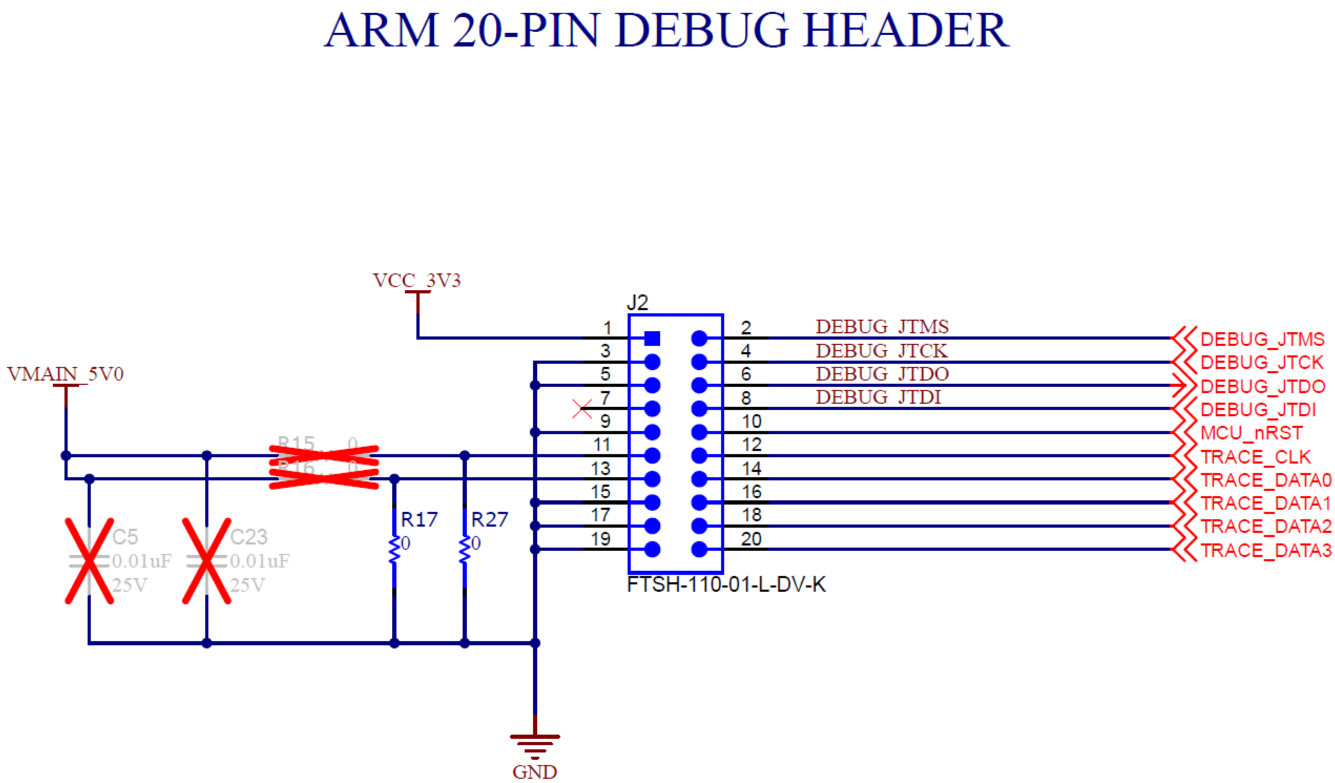


Figure 2-21. AM13E230x controlSOM Debug Header

2.9.2 Debug Probes

AM13E230x MCUs support several TI and industry-standard debug probes and Integrated Development Environments (IDEs). The following are recommended:

Table 2-16. Supported Debuggers and IDEs

Debug Probe	Description	Supported IDEs
TI XDS110	Preferred entry-level, low-cost debug probe from TI.	CCS, IAR
IAR I-JET	Fast debugging platform via JTAG and SWD/SWO. It can measure target power consumption with a high degree of accuracy and enables Power debugging in IAR Embedded Workbench.	IAR
KEIL ULink	Debugger for Cortex-M devices. Can control the processor, set breakpoints, and read/write memory contents, all while the processor is running at full speed.	Keil

2.10 Boot Interfaces

The AM13E230x bootloader can be programmed to the device through the following peripheral interfaces:

- UART
- I2C
- MCAN

For more information on the AM13E230x Bootloader, refer to the *AM13E230 Bootloader User's Guide.*

2.10.1 UART Bootloader

On AM13E230x devices, UART is configured by the device ROM code to the following default configurations:

Table 2-17. Default UART Pins

UART Signal	Device Signal Name	Pin Name	GPIO #	Mux Mode
UART RX	UC4_RX_SCL_SCLK	PA1	GPIO1	7

Table 2-17. Default UART Pins (continued)

UART Signal	Device Signal Name	Pin Name	GPIO #	Mux Mode
UART TX	UC4_TX_SDA_PICO	PA0	GPIO0	7

- Baud Rate: 9600

Having these signals available on a header can aid in debugging a prototype system and make sure that the device is booting properly at power-on. For these reasons, it is highly recommended that this UART interface is accessible on the PCB system.

2.10.2 I2C Bootloader

The following I2C pins are configured by the device ROM code for programming the bootloader:

Table 2-18. I2C Pins

I2C Signal	Device Signal Name	Pin Name	GPIO #	Mux Mode
I2C SCL	UC2_RX_SCL	PA23	GPIO23	4
I2C SDA	UC2_TX_SDA	PA22	GPIO22	4

Due to the open-drain nature of I2C, the SCL and SDA pins must be pulled up to VDD using a 4.7kΩ resistor.

2.10.3 MCAN Bootloader

The following MCAN pins are configured by the device ROM code for programming the bootloader:

Table 2-19. MCAN Pins

MCAN Signal	Device Signal Name	Pin Name	GPIO #	Mux Mode
MCAN RX	MCAN0_RX	PA11	GPIO11	10
MCAN TX	MCAN0_TX	PA12	GPIO12	10

For details regarding the hardware design requirements for MCAN, refer to the MCAN section of this document.

2.11 Unused Pins

Often times, applications and systems will not utilize the entire package pinout of the AM13E230x device. For unused pins, refer to the explicit requirements outlined in the Pin Connectivity Requirements section in the device-specific data sheet.

3 PCB Layout Design

After creating and validating that the system schematic is properly designed and meets all engineering specifications, the next step is to create the PCB layout in the preferred PCB design software. TI Evaluation Modules are designed using Altium Designer. Elements of the TI EVM designs can be re-purposed as they are well-validated examples of an AM13E230x MCU system.

3.1 Layout Design Overview

Proper layout practices must be implemented to ensure proper functionality and reliability of the PCB system. All aspects of the board – physical dimensions, PCB constraints, and key components should be considered thoroughly. While the schematic design portion of a system may indicate correct signal connections, the physical manifestations of the circuits must follow the guidelines and recommendations outlined in the following sections.

3.1.1 Recommended Layout Practices

AM13E230x real-time control systems typically include low-level analog, high-speed digital, and high-power (switching) circuits. It is recommended to section off each of these different types of signals and separate them on the PCB. Analog signals are most sensitive to the other two types of signals, as high current paths and high frequency signals can be disruptive to analog signals.

For this reason, it is important to take care when designing the pinout of the MCU, and is why utilization of the SysConfig tool is strongly encouraged when assigning MCU pins to signals. Not only does grouping these types of signals at the MCU pinout level make signal routing easier and more optimized, but it helps to guarantee that different signal types will be separate once fanned out from the MCU package.

3.1.2 Board Dimensions

PCB dimensions are largely dependent on the system and end equipment application. The PCB can range from a small board, like the AM13E230x controlSOM EVM that consists of a few devices to larger boards like the AM13E230x LaunchPad EVM that has additional on-board ICs and components. If possible, allot enough PCB area to simplify the design process and assist in routing traces/separating signals. If signals cannot be sufficiently separated on signal layers, additional PCB layers may be added to ensure proper isolation.

3.1.3 Layer Stackup

There are several considerations in planning the PCB layer stackup, both from an electrical design and practical standpoint. Number of connections, types of signal routing, top/bottom layer component utilization should be top priorities, whereas PCB manufacturing cost is often the key factor in determining layer count.

3.1.3.1 4-Layer Stackup

AM13E230x MCUs are offered in six package sizes, all of which can be reasonably routed on a 4-layer PCB. This layer count enables the designer to include a solid ground plane and split power plane on the interior layers, while utilizing the top and bottom layers for signal routing.

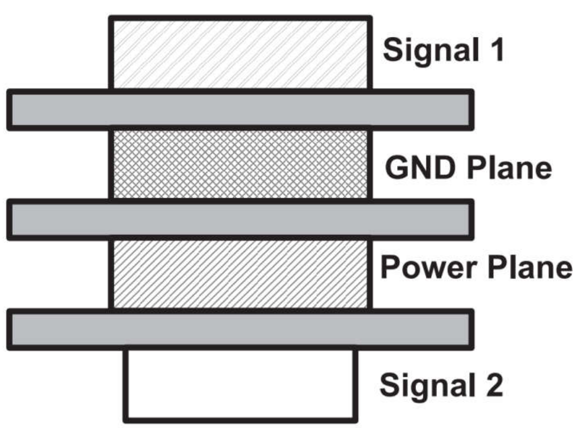


Figure 3-1. 4-Layer PCB Stack-Up

Table 3-1. 4-Layer PCB Stackup

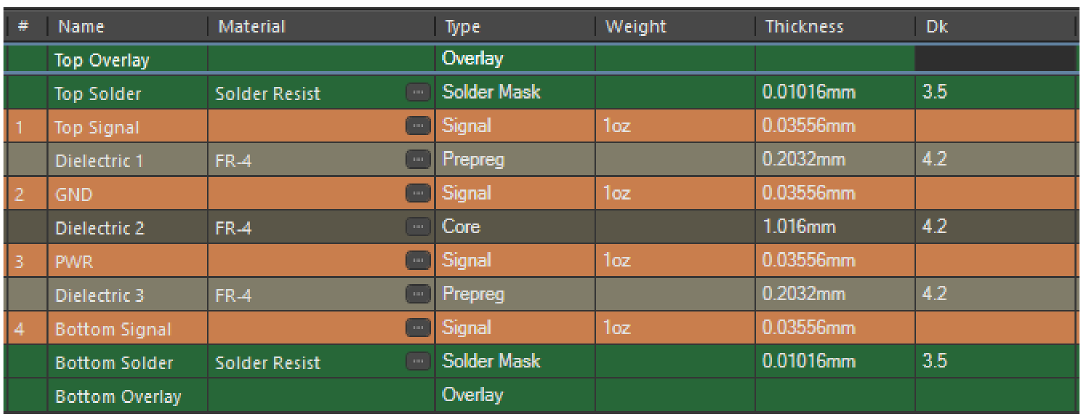
Layer	Utilization
Copper 1 (TOP)	Top layer mounting and signal routing
Copper 2	GND return plane
Copper 3	Power routing
Copper 4 (BOTTOM)	Bottom layer mounting and signal routing

The AM13E230x LaunchPad stackup represents the most optimized stackup example validated by TI for this family of MCU devices at this time.

Table 3-2. EVM Stackup Features

PCB Characteristic	64-pin QFP (LaunchPad)
Total Layers	4
PCB Thickness	62mil +/-10%
Signal/Power Layers have Adjacent GND Reference	YES
Core Center Layer Thickness	40mil

The AM13E230x LaunchPad routes the following on each PCB layer:



#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5
1	Top Signal		Signal	1oz	0.03556mm	
	Dielectric 1	FR-4	Prepreg		0.2032mm	4.2
2	GND		Signal	1oz	0.03556mm	
	Dielectric 2	FR-4	Core		1.016mm	4.2
3	PWR		Signal	1oz	0.03556mm	
	Dielectric 3	FR-4	Prepreg		0.2032mm	4.2
4	Bottom Signal		Signal	1oz	0.03556mm	
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5
	Bottom Overlay		Overlay			

Figure 3-2. 4-Layer AM13E230x PCB System Stackup

3.1.3.2 6-Layer Stackup

If all device I/O are being utilized, a 6-layer PCB may be required for designs using the 128-pin QFP, such as the AM13E230x controlSOM EVM.

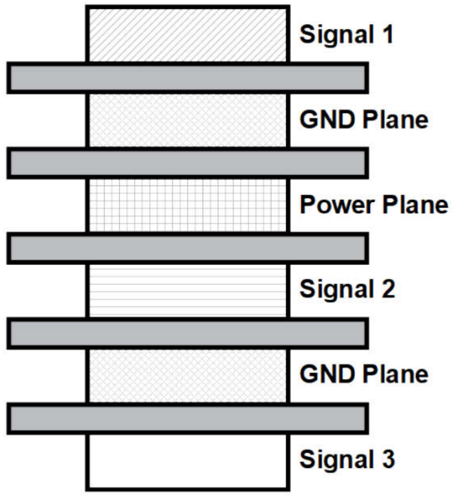


Figure 3-3. 6-Layer PCB Stackup

Table 3-3. 6-Layer PCB Stackup

Layer	Utilization
Copper 1 (TOP)	Top layer mounting and signal routing
Copper 2	GND return plane
Copper 3	Analog signal routing
Copper 4	Power routing
Copper 5	GND return plane
Copper 6 (BOTTOM)	Bottom layer mounting and signal routing

The AM13E230x controlSOM has 6 layers. Due to the higher pin count on the device, an inner signal routing layer is added in order to route and isolate sensitive analog signals from digital signal routing on layers 1 and 6. This has shown to improve analog performance on the routed peripherals.

Table 3-4. EVM Stackup Features

PCB Characteristic	128-pin QFP (controlSOM)
Total Layers	6
PCB Thickness	62mil +/-10%
Signal/Power Layers have Adjacent GND Reference	YES
Core Center Layer Thickness	28mil

The AM13E230x controlSOM routes the following on each PCB layer:

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		1mil	3.5
1	L01_Top Layer		Signal	1oz	2.087mil	
	Dielectric 1	IT180A Prepreg 2113...	Prepreg		3.511mil	4.13
2	L02_GND1		Signal	1oz	1.26mil	
	Dielectric 2	IT180A 4 mil core H/1	Prepreg		4mil	4.4
3	L03_SIG1		Signal	1oz	0.689mil	
	Dielectric 3	IT180A Prepreg 106...	Prepreg		1.909mil	3.79
	Dielectric 4	IT180A Prepreg 1080...	Prepreg		2.904mil	3.86
	Dielectric 5	IT180A 28 mil core H...	Prepreg		28mil	4.53
	Dielectric 6	IT180A Prepreg 1080...	Prepreg		2.904mil	3.86
	Dielectric 7	IT180A Prepreg 106...	Prepreg		1.909mil	3.79
4	L04_PWR1		Signal	1oz	0.689mil	
	Dielectric 8	IT180A 4 mil core H/1	Prepreg		4mil	4.4
5	L05_GND2		Signal	1oz	1.26mil	
	Dielectric 9	IT180A Prepreg 2113...	Prepreg		3.511mil	4.13
6	L06_Bottom Layer		Signal	1oz	2.087mil	
	Bottom Solder	Solder Resist	Solder Mask		1mil	3.5
	Bottom Overlay		Overlay			

Figure 3-4. 6-Layer AM13E230x PCB System Stackup

3.2 Vias

AM13E230x EVMs show different examples of via construction for the device fan-out and overall board routing. The EVMs make use of Plated Through-Hole (PTH) via construction.

Table 3-5. AM13E230x EVM Via Types

EVM	Via Type	Diameter (mils)	Via Drill (mils)	Misc
AM13E230x LaunchPad	PTH	18	10	Tented
AM13E230x controlSOM	PTH	18	8	Tented

In general, projects that are cost-sensitive should aim to use larger via drill sizes.

3.3 Recommended Board Layout

To ensure that the signals routed on the board do not experience any cross-talk or degraded performance, a good practice is to partition the board similar to that shown in <Figure>. As mentioned in <section>, the three types of signals (digital, analog, and high-current) should all be sectioned off from each other on the PCB.

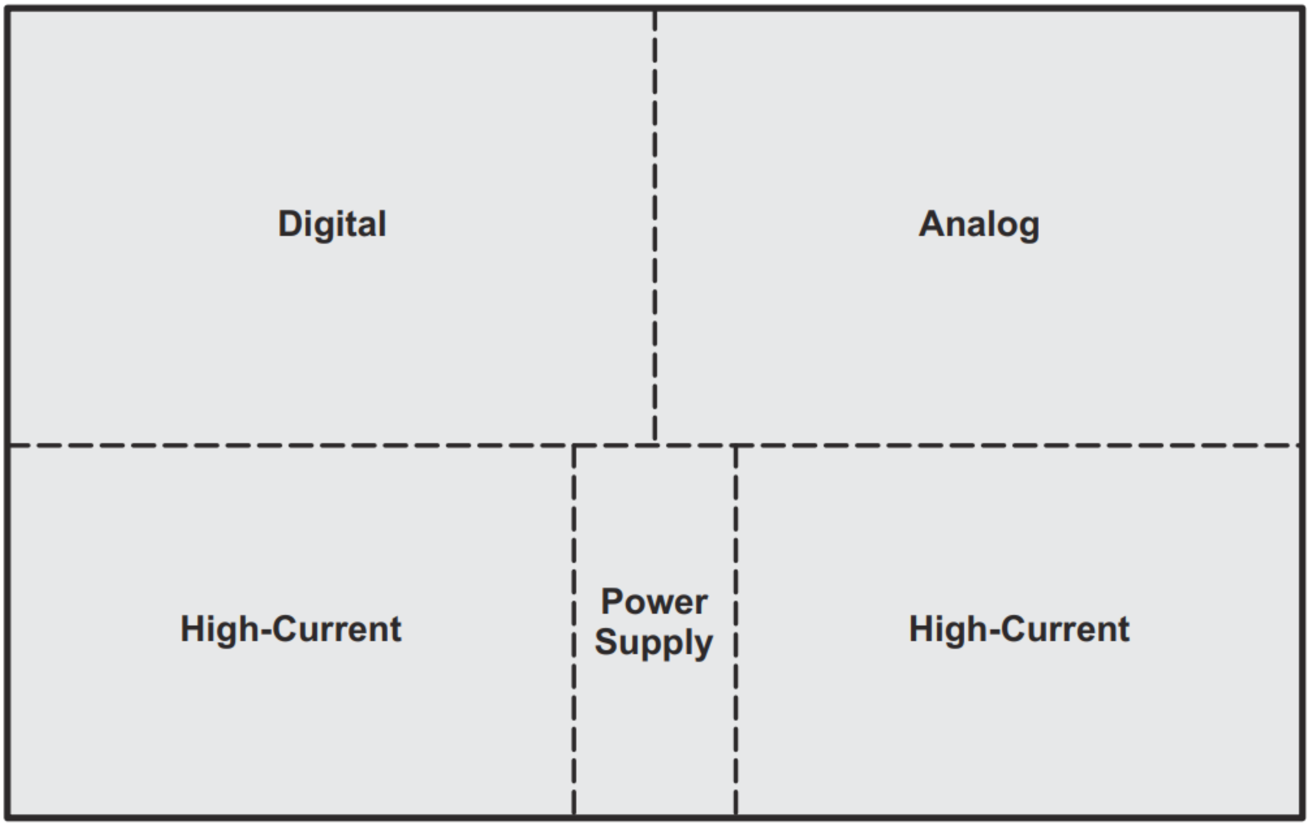


Figure 3-5. Ideal PCB Partitioning

3.4 Placing Components

Once the PCB floorplan is set, the first (and most consequential) step is to determine the position of the AM13E230x MCU. The package orientation should allow for optimized routing and ensure that traces can remain short and direct between the MCU and external connections. If convenient, the MCU device can be placed at a 45-degree angle such as on the AM13E230x LaunchPad to align the device pins with the signal trace connections.

After the MCU device is set, the next most critical component to place is the crystal/oscillator. For full implementation details with examples, reference the Section 2.8 section of this document.

Next, the decoupling capacitors for the device power pins should be placed. These capacitors must be placed as close as possible to their respective pins to reduce noise and ensure stability on the device power supply nets. Decoupling capacitors placed more than one inch away from a power pin offers poor performance. However, bulk capacitors can be placed relatively further away from the MCU without greatly impacting the performance. For full implementation details with examples, reference the Section 2.6.2 section of this document.

Following the power rail decoupling, debug header/circuits and reset logic should be placed and routed.

3.5 Ground Planes

Copper planes on a PCB are excellent high-frequency capacitors and can be utilized for high-frequency bypassing along with the recommend capacitors. Another benefit of solid planes are that they can act as a good heat sink to mitigate excess thermal levels. If the board has ample layers, a good practice is to place a ground place on the PCB. This ground plane not only assists in routing the ground signals on a board, but also helps in combating ground noise. Each signal on the board has a return current (via GND), and this ensures that the return path is through the path of least impedance. For boards with multiple ground planes on different layers, it is helpful to employ via stitching to connect these ground planes and further minimize impedance.

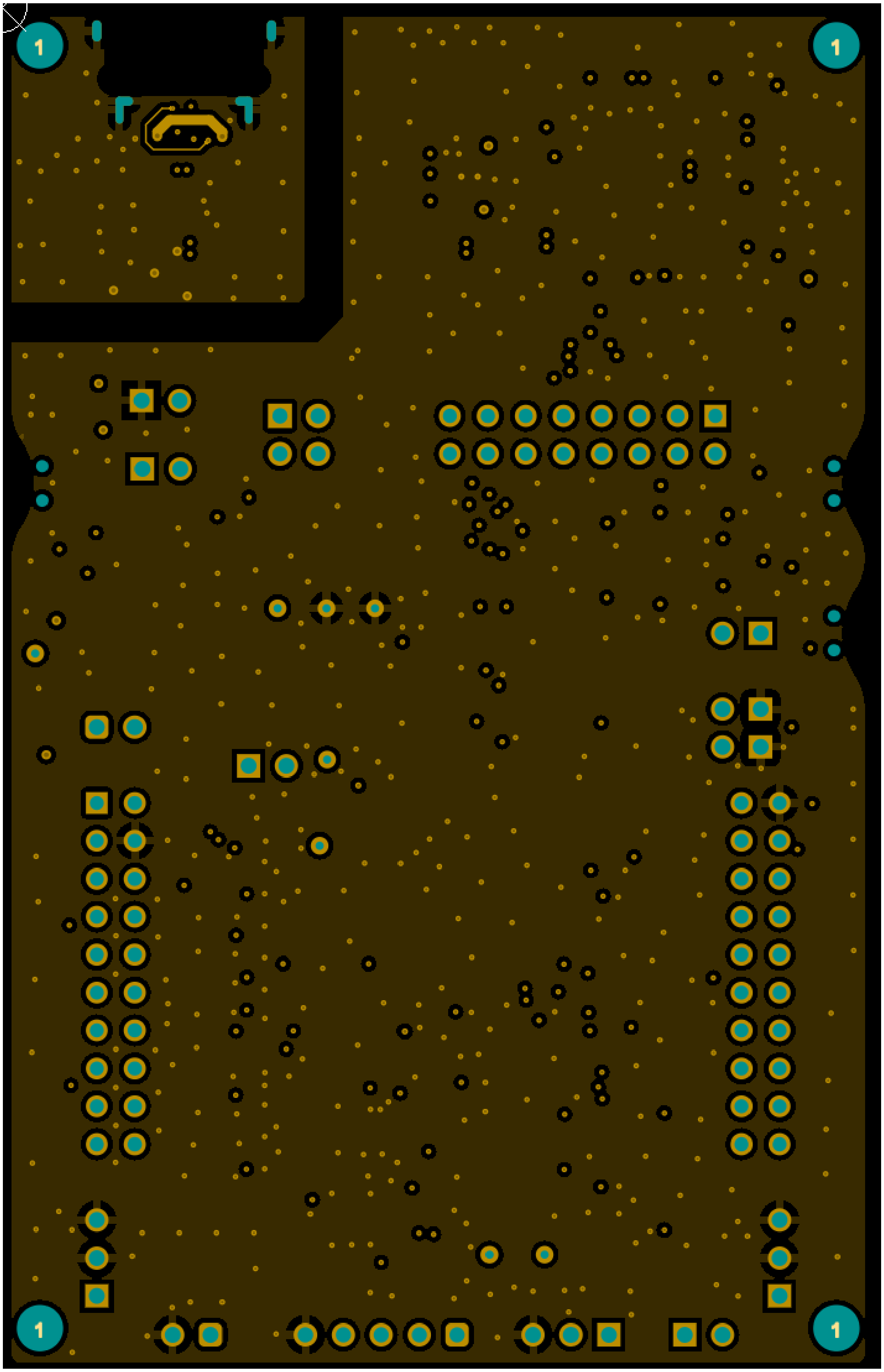


Figure 3-6. GND Plane on AM13E230x LaunchPad

The key to an effective ground plane is making sure that the plane remains intact and has good connections throughout the entire layer of the board. Onboard connections, such as vias and traces, can cut up the ground layer and reduce its effectiveness. Vias create a hole through multiple layers of the board and traces can sever the connection between different parts of the ground plane. In the left figure below, notice that the RGND vias only have a single connection to the ground plane and that the surrounding ground pore connections are very thin. Furthermore, in the Figure 4-8, notice that the top left of the pore is connected to the bottom left of the pour only through a thin sliver of copper. Both of these figures showcase undesirable ground planes. It would be helpful to rearrange the vias and traces to ensure that there are no thin ground plane connections or a severely cut-up ground pour.

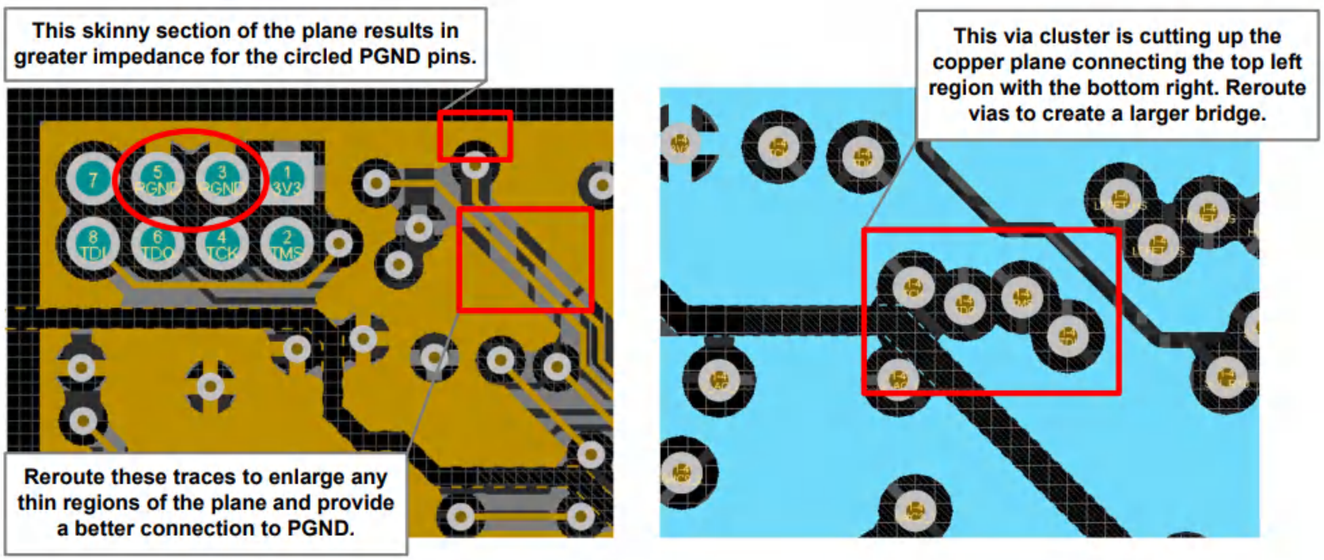


Figure 3-7. Cut-Up GND Plane Examples

When applying a ground plane to a layer, examine the plane to see if it has good connection throughout. Areas with missing planes or thin connections should be redesigned to maximize the ground plane area. Typically, this can be done by reducing the number of vias and by routing groups of traces closer to each other. In some cases, it may be helpful to modify the pinmux selection and schematic to improve routing. Sometimes these benefits may not be apparent until the layout routing process begins, but optimizing the pinmux can result in shorter trace lengths and reduced via usage, and thus a better ground plane.

3.6 Signal Routing Traces

Pull in from C2K guide.

3.7 Thermal Considerations

Systems and end products that exceed the AM13E230x data sheet's recommended maximum power dissipation may require additional thermal dissipation incorporated into the PCB design. The primary thermal consideration is the device junction temperature (TJ). This specification should be carefully tested to that it remains in the absolute and recommended limits, as outlined in the device data sheet. This ensures reliable and functional operation of the device over its entire lifetime. It is also important to consider the ambient temperature (TA) of the system, through this is dependent on the end application environment and product design.

To minimize TJ throughout the PCB system design, the board-to-ambient thermal resistance (ΘBA) must be kept as small as possible. The device ground and power pins are the primary sources of heat dissipation. Thus, if the device has a thermal pad pin (48-pin QFN package only), ensure that it is tied to a large copper area on the PCB. For all other AM13E230 QFP package types, ensure that all GND and power pins have good connection to a solid plane, and that any vias on these nets remain close to the AM13E230x device.

4 EOS, EMI/EMC, ESD Considerations

As with any electrical system, it is important to consider the possible effects of outside electromagnetic factors and to take steps to limit and mitigate any impacts. Insufficient care to do so may result in non-optimal performance, reduced reliability, and potential damage to the components.

4.1 Electrical Overstress

The AM13E230x data sheet provides great detail about the recommended and maximum conditions in which the device is expected to function properly and reliably. The following points detail the most important considerations to be aware of when using the AM13E230x devices:

- GPIO input voltages cannot be >VDD+0.3V nor <VSS-0.3V
- Analog input voltages cannot be >VDDA+0.3V nor <VSSA-0.3V
- For all digital and analog input pins, the input clamp current should not be >20mA or <-20mA.
- The continuous clamp current per pin is +/-2mA. However, do not operate in this condition continuously as VDD/VDDA voltage may internally rise and impact other electrical specifications.
- Any signals/IOs that may be powered prior to the AM13E230x being powered on and booting should be current limited and protected such that the signals do not exceed the specifications listed in the data sheet.
- Use of 3.3V powered operational amplifier (op amp), steering diodes, or series resistance, or any combination of the three, may be necessary to remove the risk of damage to the device.

4.2 EMI and EMC

Electromagnetic Compatibility (EMC) describes the ability of electronic components to function properly amidst interferences and disturbances from other systems. The most important to consider is Electromagnetic Interference (EMI) – radio frequency energy emitted by the MCU device and other nearby devices. This type of disturbance can propagate throughout a system and impact devices through conduction and radiation.

Reducing EMI effects to the system itself should be top priority when it comes to minimizing EMC risk, but it is also important to ensure that EMI emitted from the system in both radiation and conduction does not exceed the maximum allowed per local regulation standards. It is good practice to minimize radiated and conducted EMI to levels far below the limits for certification in order to avoid any project delays due to this easily mitigated component of design. Similarly, the PCB system should be designed with adequate shielding to function properly even while being in contact with radiated and conducted EMI energy from other systems around it.

The majority of system components, including the PCB, connectors, and cables serve as a source of EMI. PCB systems that make use of high frequencies and fast-switching currents & voltages require special care as all of the signal traces act as antennas which radiate electromagnetic energy well.

The five main sources of radiation that designers should look to minimize are:

1. Digital signals propagating on PCB traces
2. Current return loop areas
3. Inadequate power supply filtering or decoupling
4. Transmission line effects
5. Lack of power and ground planes

Power supplies are another major contributor to EMI, especially if they are switching or are being switched using PWM signal outputs from the MCU device. It is important to follow the recommended layout for each power supply found in the product’s data sheet.

To reduce unwanted EMI generated by the PCB system and its components, the following guidelines should be met throughout the schematic and PCB layout design process:

- Use decoupling capacitors on all power inputs to IC devices. Follow the recommended capacitor values as outlined in each IC data sheet. Be aware that every capacitor has a self-resonant frequency.
- Provide adequate filter capacitors on power supply sources. These capacitors should have low equivalent series inductance (ESL).
- Create ground planes in available spaces on the PCB routing layers. Connect these ground polygons to the main inner ground plane with vias. Creating a quarter-inch via grid across the PCB is ideal.

- Keep the current loops as small as possible. Add as many required decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Apply current return rules to connect the grounds together while isolating the ground plane for the analog portion. If the project does not use ADC and there are no analog circuits, do not isolate grounds.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes or PC board stack-up, add as many power and ground planes as possible. Keep the power and ground planes next to each other to ensure low-impedance stack-up or large natural capacitance stack-up.
- Add an EMI pi filter on all the signals exiting the box or entering the box.
- If the system fails EMI tests, find the source by tracing the failed frequencies to their source. For example, assume the design fails at 300 MHz but there is nothing on the board running at that frequency. The source is likely to be a third harmonic of a 100 MHz signal.
- Determine if the failed frequencies are common mode or differential mode. Remove all the cables connected to the box. If the radiation changes, it is common mode. If not, then it is differential mode. Then, go to the source and use termination or decoupling techniques to reduce the radiation. If it is common mode, add pi filters to the inputs and outputs. Adding a common choke onto the cable is an effective solution but an expensive method for EMI reduction.

4.3 Electrostatic Discharge

A buildup of electrical charge can result in electrostatic discharge (ESD) to the device while in operation. Care should be taken when handling these microcontrollers and when storing them. All of the AM13E230x devices are tested to comply with the TI standard ESD specifications, including the peripherals and the port pins. They are rated to withstand the following ESD tests:

- Human-Body Model (HBM), at +/-2000V
- Charged-Device Model (CDM) at +/-500V
  - For the corner pins on all device packages, the CDM value is +/-750V

A supply voltage glitch or ESD will put the device in an unknown state. Therefore, it is important to have a good PCB layout for optimum noise and ESD performance. The similar ESD protection diodes can be utilized for JTAG pins as well. Keep the loop area of critical traces (in this case, JTAG, nRST, X1, X2) as small as possible. If your design needs to bring any pin, like a GPIO, to a connector (for external connectivity) be sure to take special ESD care by adding ESD protection parts. Some systems may require mechanical fixes like metallic shielding, rerouting of cabling, and so forth, to maintain ESD protection. When using these external ESD protection devices, be sure to carefully follow the layout guidelines specified in the device-specific data sheet to maximize its effectiveness.

5 Summary and Checklist

For the most optimal performance when designing PCB systems featuring an AM13E230x MCU, the systems should be carefully designed and tested according to the specifications outlined in this document. To ease the schematic design process, TI provides a checklist spreadsheet outlining the most important requirements for designing with the AM13E230x family of real-time control MCUs. This checklist can be accessed by contacting your local TI Field Sales Representative.

6 References

- AM13E230x Microcontrollers Data Sheet
- AM13E230x Microcontrollers Technical Reference Manual

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release