User's Guide

AM13E230 STM32G4 Migration Guide

ABSTRACT

This Migration Guide assists with migrating from the STMicroelectronics STM32® platform to the Texas Instruments AM13E230x real-time control MCU ecosystem. This guide introduces the AM13E230x core architecture, peripheral considerations, and software development kit. The intent of this guide is to highlight the differences between the two microcontroller platform families and to leverage existing knowledge of the STM32 ecosystem to quickly ramp with the AM13E230x series of MCUs.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 AM13E230x Portfolio Overview

1.1 Introduction

The AM13E230x microcontrollers are low-cost, 32-bit devices built for complex appliance and motor control applications. The high-performance Arm® Cortex-M33 core, operating at up to 200MHz includes a math accelerator for trigonometric operations (TMU) and a Neural-network Processing Unit (NPU) Artificial Intelligence (AI) Engine to enable simultaneous motor control and AI model execution. Rich analog integration on the device offers industry-leading speed, precision, and reduced system cost. The digital peripherals offered on AM13E230x MCUs are specifically built for motor control and PFC applications, and include tailored communications interfaces for appliance and industrial motor control. AM13E23x microcontrollers operate in the 3.3V supply domain, and support an ambient temperature of up to 105°C and junction temperature range of -40°C to 140°C.

The AM13E230x family of MCUs consists of devices with full analog and digital peripheral integration that allow customers to find the MCU that meets project needs, with 7 device package options and 3 memory configurations to choose from. The AM13E230x MCU platform combines the Arm® Cortex®-M33 platform with a holistic low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

For more information on the AM13E230x MCU platform, refer to the device Data Sheet and Technical Reference Manual.

1.2 Portfolio Comparison of STM32G474x and AM13E230x MCUs

Table 1-1 details a baseline comparison between the STM32G474x and AM13E230x families of microcontroller devices.

Table 1-1. Comparison of TI AM13E230x and STM32G474x

		STMicro STM32G474x	TI AM13E230x
Core/Frequency		ARM Cortex-M4F/170 MHz	ARM Cortex-M33/200 MHz
Supply Voltage		1.7 V to 3.6 V	3.3V
Junction Temperature (T_J)		-40°C to 130°C	-40°C to 125°C
Ambient Temperature (T_A)		-40°C to 125°C	-40°C to 105°C
Memory		Up to 512KB	Up to 512KB
RAM		96KB	Up to 128KB
General-Purpose I/O (GPIO) (max)		38 (LQFP 48) 52 (LQFP 64) 66 (LQFP 80) 86 (LQFP 100) 107 (LQFP 128)	38 (LQFP 48) 52 (LQFP 64) 66 (LQFP 80) 86 (LQFP100) 107 (LQFP128)
Analog	Analog to Digital Converter (ADC)	5x, up to 4MSPS at 12-bits	3x, up to 8.9MSPS at 12-bits
	Comparators	7x	4x Comparator Subsystems (CMPSS) with 2x Comparators (CMPH/CMPL), each includes 8-bit reference DAC
	Amplifiers	6x	3x Programmable Gain Amplifiers (PGA)
	Digital to Analog Converter (DAC)	4x	2x DAC Output driven by CMPSS[3:2] DACL
	Internal VREF	Yes	Yes
Digital Communication Peripherals	UART	2x UART 3x USART	Up to 6x via UNICOMM
	I2C	4x	Up to 6x via UNICOMM
	SPI	Up to 4x	Up to 4x via UNICOMM
	CAN-FD	3x	1x

Table 1-1. Comparison of TI AM13E230x and STM32G474x (continued)

		STMicro STM32G474x	TI AM13E230x
Digital Control Peripherals	PWM Channels	Up to 48x	Up to 30x (5x, 6-ch MCPWM modules)
	Enhanced Capture Module (eCAP)	N/A (Implemented via Timer Module)	2x (Supports capture and aPWM modes)
	Enhanced Quadrature Encoder Pulse Module (eQEP)	N/A (Implemented via Timer Module)	3x
Timers	General-Purpose	5x 16-bit 2x 32-bit	1x 16-bit 1x 32-bit
	Watchdog	2x	1x
	SysTick	1x	1x
Hardware Accelerator		FMAC, CRC, CORDIC, AES	TMU, NPU, CRC, AES
Neural-Network Processing Unit		N/A	1x NPU
Security		CRC	AES, secure boot, CRC
Low Power		Active: 100 µA/MHz Standby (RTC): 1.5 µA	RUN: 49 mA @200MHz STANDBY: 1.84mA SHUTDOWN: <5 µA

Note

This table is not inclusive of all features of each device family

2 Device Pinout Comparison

2.1 Device Pin and Signal Comparison Tables

The following sections detail the pin-to-pin and signal-to-signal migration between the STM32G474x and AM13E230x device families.

2.1.1 Device Pin-to-Pin Comparison

The following table describes the pin names on STM32G474x and equivalent pin names on AM13E230x.

Table 2-1. STM32G474x to AM13E230x Pin Migration

STM32G474x Pin Name	AM13E230x Pin Name	Notes
PA0	PA0	
PA1	PA1	
PA2	PA2	
PA3	PA3	
PA4	PA4	
PA5	PA5	
PA6	PA6	
PA7	PA7	
PA8	PA8	
PA9	PA9	
PA10	PA10	
PA11	PA11	
PA12	PA12	
PA13	PA13	
PA14	PA14	
PA15	PA15	
PB0	PA16	
PB1	PA17	
PB2	PA18	
PB3	PA19	
PB4	PA20	
PB5	PA21	
PB6	PA22	
PB7	PA23	
PB8-BOOT0	PA24	All AM13E230x GPIOs can support the BSL INVOKE function via hardware.
PB9	PA25	
PB10	PA26	
PB11	PA27	
PB12	PA28	
PB13	PA29	
PB14	PA30	
PB15	PA31	
PC0	PB0	
PC1	PB1	
PC2	PB2	
PC3	PB3	
PC4	PB4	
PC5	PB5	

Table 2-1. STM32G474x to AM13E230x Pin Migration (continued)

STM32G474x Pin Name	AM13E230x Pin Name	Notes
PC6	PB6	
PC7	PB7	
PC8	PB8	
PC9	PB9	
PC10	PB10	
PC11	PB11	
PC12	PB12	
PC13	PB13	
PC14-OSC32_IN	PB14	No 32KHz LFXTAL input on AM13E230x
PC15-OSC32_OUT	PB15	No 32KHz LFXTAL input on AM13E230x
PD0	PB16	
PD1	PB17	
PD2	PB18	
PD3	PB19	
PD4	PB20	
PD5	PB21	
PD6	PB22	
PD7	PB23	
PD8	PB24	
PD9	PB25	
PD10	PB26	
PD11	PB27	
PD12	PB28	
PD13	PB29	
PD14	PB30	
PD15	PB31	
PE0	PC0	
PE1	PC1	
PE2	PC2	
PE3	PC3	
PE4	PC4	
PE5	PC5	
PE6	PC6	
PE7	PC7	
PE8	PC8	
PE9	PC9	
PE10	PC10	
PE11	PC11	
PE12	PC12	
PE13	PC13	
PE14	PC14	
PE15	PC15	
PF0-OSC_IN	PC16_X1	X1 functions as XTAL IN (crystal oscillator in) or HFCLK_IN or GPIO
PF1-OSC_OUT	PC17_X2	X2 functions as XTAL OUT (crystal oscillator out) or GPIO
PF2	PC18	
PF3	PC19	
PF4	PC20	

Table 2-1. STM32G474x to AM13E230x Pin Migration (continued)

STM32G474x Pin Name	AM13E230x Pin Name	Notes
PF5	PC21	
PF6	PC22	
PF7	PC23	
PF8	PC24	
PF9	PC25	
PF10	PC26	
PF11	PC27	
PF12	PC28	
PF13	PC29	
PF14	PC30	
PF15	PC31	
PG0	PD0	
PG1	PD1	
PG2	PD2	
PG3	PD3	
PG4	PD4	
PG5	PD5	
PG6	PD6	
PG7	PD7	
PG8	PD8	
PG9	PD9	
PG10-NRST	PD10-NRST	nRST only on AM13E230x - no GPIO/muxmode functionality
VBAT	VDD	No VBAT power domain on AM13E230x
VDD	VDD	3.3V Digital Power
VDDA	VDDA	3.3V Analog Power
VREF-	VREFLO	Negative Analog Voltage Reference
VREF_+	VREFHI	Positive Analog Voltage Reference
VREF+		Positive Analog Voltage Reference
VSS	VSS	Digital Ground
VSSA	VSSA	Analog Ground

2.1.2 STM32G474x Alternate Functions and AM13E230x Signal Names

The following table describes the Alternate Function signal names on STM32G474x and the equivalent signal names on AM13E230x.

Note

UNASSIGNED AM13E230x signals indicate that there is no direct equivalent for the STM32G474x functional signal on the AM13E230x platform.

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
Comparator Output		
COMP1_OUT	UNASSIGNED	Replaced by XBAR on AM13E230x
COMP2_OUT	UNASSIGNED	
COMP3_OUT	UNASSIGNED	
COMP4_OUT	UNASSIGNED	
COMP5_OUT	UNASSIGNED	
COMP6_OUT	UNASSIGNED	
COMP7_OUT	UNASSIGNED	
EVENTOUT		
EVENTOUT	OUTPUTXBAR_x	OUTPUTXBAR[7:0]
CAN-FD		
FDCAN1_RX	MCAN0_RX	All FDCANx on STM32G474x map to MCAN0 on AM13E230x
FDCAN1_TX	MCAN0_TX	
FDCAN2_RX	MCAN0_RX	
FDCAN2_TX	MCAN0_TX	
FDCAN3_RX	MCAN0_RX	
FDCAN3_TX	MCAN0_TX	
External Memory Controller		
FMC_A0	EPI0_S0	
FMC_A1	EPI0_S1	
FMC_A10	EPI0_S26	
FMC_A11	EPI0_S27	
FMC_A12	UNASSIGNED	
FMC_A13	UNASSIGNED	
FMC_A14	UNASSIGNED	
FMC_A15	UNASSIGNED	
FMC_A16	UNASSIGNED	
FMC_A17	UNASSIGNED	
FMC_A18	UNASSIGNED	
FMC_A19	UNASSIGNED	
FMC_A2	EPI0_S2	
FMC_A20	EPI0_S20	
FMC_A21	EPI0_S21	
FMC_A22	EPI0_S22	
FMC_A23	EPI0_S23	
FMC_A24	EPI0_S24	
FMC_A25	EPI0_S25	
FMC_A4	EPI0_S4	
FMC_A5	EPI0_S5	

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
FMC_A6	EPI0_S6	
FMC_A7	EPI0_S7	
FMC_A8	EPI0_S8	
FMC_A9	EPI0_S9	
FMC_D0	EPI0_S0	
FMC_D0/FMC_DA0		
FMC_D10	EPI0_S10	
FMC_D10/FMC_DA10		
FMC_D1	EPI0_S1	
FMC_D1/FMC_DA1		
FMC_D11	EPI0_S11	
FMC_D11/FMC_DA11		
FMC_D12	EPI0_S12	
FMC_D12/FMC_DA12		
FMC_D13	EPI0_S13	
FMC_D13/FMC_DA13		
FMC_D14	EPI0_S14	
FMC_D14/FMC_DA14		
FMC_D15	EPI0_S15	
FMC_D15/FMC_DA15		
FMC_D2	EPI0_S2	
FMC_D2/FMC_DA2		
FMC_D3	EPI0_S3	
FMC_D3/FMC_DA3		
FMC_D4	EPI0_S4	
FMC_D4/FMC_DA4		
FMC_D5	EPI0_S5	
FMC_D5/FMC_DA5		
FMC_D6	EPI0_S6	
FMC_D6/FMC_DA6		
FMC_D7	EPI0_S7	
FMC_D7/FMC_DA7		
FMC_D8	EPI0_S8	
FMC_D8/FMC_DA8		
FMC_D9	EPI0_S9	
FMC_D9/FMC_DA9		
FMC_INT	EPI0_S32	
FMC_NL	EPI0_S30	
FMC_NBL0	EPI0_S16	
FMC_NBL1	EPI0_S17	
FMC_NCE/FMC_NE1	EPI0_S26	
FMC_NCE/FMC_NE2	EPI0_S27	
FMC_NE3	EPI0_S34	
FMC_NE4	EPI0_S33	
FMC_NOE	EPI0_S28	
FMC_NWAIT	EPI0_S32	
FMC_NWE	EPI0_S29	

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
High-Resolution Timers/PWM		
HRTIM1_CHA1	MCPWM3_1A	
HRTIM1_CHA2	MCPWM3_1B	
HRTIM1_CHB1	MCPWM3_2A	
HRTIM1_CHB2	MCPWM3_2B	
HRTIM1_CHC1	MCPWM3_3A, MCPWM4_3A	
HRTIM1_CHC2	MCPWM3_3B, MCPWM4_3B	
HRTIM1_CHD1	MCPWM4_1A	
HRTIM1_CHD2	MCPWM4_1B	
HRTIM1_CHE1	MCPWM4_2A, MCPWM3_3A	
HRTIM1_CHE2	MCPWM4_2B, MCPWM3_3B	
HRTIM1_CHF1	MCPWM4_3A	
HRTIM1_CHF2	MCPWM4_3B	
HRTIM1_EEV1	UNASSIGNED	Replaced by XBAR (External Events)
HRTIM1_EEV2		
HRTIM1_EEV3		
HRTIM1_EEV4		
HRTIM1_EEV5		
HRTIM1_EEV6		
HRTIM1_EEV7		
HRTIM1_EEV8		
HRTIM1_EEV9		
HRTIM1_EEV10		
HRTIM1_FLT1	UNASSIGNED	Replaced by XBAR (Fault Conditioning)
HRTIM1_FLT2		
HRTIM1_FLT3		
HRTIM1_FLT4		
HRTIM1_FLT5		
HRTIM1_FLT6		
HRTIM1_SCIN	UNASSIGNED	Replaced by XBAR - Sync In
HRTIM1_SCOUT	UNASSIGNED	Replaced by XBAR - Sync Out
I2C		
I2C1_SCL	UC0_RX_SCL_SCLK	
I2C1_SDA	UC0_TX_SDA_PICO	
I2C1_SMBA	UNASSIGNED	No Dedicated SMBus Alert Signal in UNICOMM module
I2C2_SCL	UC1_RX_SCL_SCLK	
I2C2_SDA	UC1_TX_SDA_PICO	
I2C2_SMBA	UNASSIGNED	No Dedicated SMBus Alert Signal in UNICOMM module
I2C3_SCL	UC2_RX_SCL_SCLK	UC2 - SMBUS Support
I2C3_SDA	UC2_TX_SDA_PICO	UC2 - SMBUS Support
I2C3_SMBA	UNASSIGNED	No Dedicated SMBus Alert Signal in Unicomm
I2C4_SCL	UC3_RX_SCL_SCLK	
I2C4_SDA	UC3_TX_SDA_PICO	
I2C4_SMBA	UNASSIGNED	No Dedicated SMBus Alert Signal in Unicomm

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
I2S2_MCK	UNASSIGNED	No I2S
I2S3_MCK		
I2SCKIN		
IR_OUT	UNASSIGNED	No Infrared Interface (IR)
LPTIM1_ETR	UNASSIGNED	
LPTIM1_IN1	UNASSIGNED	
LPTIM1_IN2	UNASSIGNED	
LPTIM1_OUT	UNASSIGNED	
Low-Power UART		
LPUART1_CTS	UC0_CTS_CS0	
LPUART1_DE/LPUART1_RTS	UC0_RTS_POCI	
LPUART1_RTS_DE	UC0_RTS_POCI	
LPUART1_RX	UC0_RX_SCL_SCLK	
LPUART1_TX	UC0_TX_SDA_PICO	
OMP5_OUT	UNASSIGNED	Replaced by OUTPUTXBAR
Quad SPI		
QUADSPI1_BK1_IO0	UNASSIGNED	No QSPI interface on AM13E230x
QUADSPI1_BK1_IO1		
QUADSPI1_BK1_IO2		
QUADSPI1_BK1_IO3		
QUADSPI1_BK1_NCS		
QUADSPI1_BK2_IO0		
QUADSPI1_BK2_IO1		
QUADSPI1_BK2_IO2		
QUADSPI1_BK2_IO3		
QUADSPI1_BK2_NCS		
QUADSPI1_CLK		
Serial Audio Interface		
SAI1_CK1	UNASSIGNED	No Serial Audio Interface on AM13E230x
SAI1_CK2		
SAI1_D1		
SAI1_D2		
SAI1_D3		
SAI1_FS_A		
SAI1_FS_B		
SAI1_MCLK_A		
SAI1_MCLK_B		
SAI1_SCK_A		
SAI1_SCK_B		
SAI1_SD_A		
SAI1_SD_B		
SPI		
SPI1_MISO	UC0_POCI	
SPI1_MOSI	UC0_TX_SDA_PICO	
SPI1_NSS	UC0_CTS_CS0	
SPI1_SCK	UC0_RX_SCL_SCLK	
SPI2_MISO	UC1_TX_SDA_PICO	

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
I2S2_SD/SPI2_MOSI	UC1_POCI	
SPI2_MOSI/I2S2_SD	UC1_POCI	
SPI2_NSS	UC1_CS0	
I2S2_WS/SPI2_NSS	UC1_CS0	
SPI2_NSS/I2S2_WS	UC1_CS0	
I2S2_CK/SPI2_SCK	UC1_RX_SCL_SCLK	
SPI2_SCK	UC1_RX_SCL_SCLK	
SPI3_MISO	UC3_CTS_CS0	
I2S3_SD/SPI3_MOSI	UC3_TX_SDA_PICO	
SPI3_MOSI/I2S3_SD	UC3_TX_SDA_PICO	
I2S3_WS/SPI3_NSS	UC3_CTS_CS0	
SPI3_NSS/I2S3_WS	UC3_CTS_CS0	
I2S3_CK/SPI3_SCK	UC3_RX_SCL_SCLK	
SPI3_SCK/I2S3_CK	UC3_RX_SCL_SCLK	
SPI4_MISO	UC4_POCI	
SPI4_MOSI	UC4_TX_SDA_PICO	
SPI4_NSS	UC4_CS0	
SPI4_SCK	UC4_RX_SCL_SCLK	
SPI2_SCK/I2S2_CK	UC1_RX_SCL_SCLK	
SPI3_SCK	UC3_RX_SCL_SCLK	
Timers/PWM		
TIM1_BKIN	UNASSIGNED	Break1 In (Replaced with XBAR)
TIM1_BKIN2	UNASSIGNED	Break2 In (Replaced with XBAR)
TIM1_CH1	MCPWM0_1A, MCPWM4_1A	
TIM1_CH1N	MCPWM0_1B, MCPWM4_1B	
TIM1_CH2	MCPWM0_2A, MCPWM4_2A	
TIM1_CH2N	MCPWM0_2B, MCPWM4_2B	
TIM1_CH3	MCPWM0_3A, MCPWM4_3A	
TIM1_CH3N	MCPWM0_3B, MCPWM4_3B	
TIM1_CH4	MCPWM0_1A, MCPWM4_1A	
TIM1_CH4N	MCPWM0_1B, MCPWM4_1B	
TIM1_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
TIM15_BKIN	UNASSIGNED	Break1 In (Replaced with XBAR)
TIM15_CH1	MCPWM3_1A, MCPWM4_2A	
TIM15_CH1N	MCPWM3_1B, MCPWM4_2B	
TIM15_CH2	MCPWM3_2A	
TIM16_CH1	MCPWM3_1A	
TIM16_CH1N	MCPWM3_1B	
TIM17_BKIN	UNASSIGNED	Break1 In (Replaced with INPUTXBAR)
TIM17_CH1	MCPWM3_3A	
TIM2_CH1	MCPWM4_1A	
TIM2_CH2	MCPWM4_1B	
TIM2_CH3	MCPWM4_2A	
TIM2_CH4	MCPWM4_2B	
TIM2_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
TIM20_CH1	MCPWM2_1A, MCPWM3_1A	
TIM20_CH1N	MCPWM2_1B, MCPWM3_1B	
TIM20_CH2	MCPWM2_2A, MCPWM3_2A	
TIM20_CH2N	MCPWM2_2B, MCPWM3_2B	
TIM20_CH3	MCPWM2_3A, MCPWM3_3A	
TIM20_CH3N	MCPWM2_3B, MCPWM3_3B	
TIM20_CH4	MCPWM2_1A, MCPWM3_1A	
TIM20_CH4N	MCPWM2_1B, MCPWM3_1B	
TIM20_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
TIM3_CH1	MCPWM4_3A	
TIM3_CH2	MCPWM4_3B	
TIM3_CH3	MCPWM4_1A	
TIM3_CH4	MCPWM4_1B	
TIM3_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
TIM4_CH1	MCPWM2_2A, MCPWM4_2A	
TIM4_CH2	MCPWM2_2B, MCPWM4_2B	
TIM4_CH3	MCPWM2_3A, MCPWM4_3A	
TIM4_CH4	MCPWM2_3B, MCPWM4_4A	
TIM4_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
TIM5_CH1	MCPWM3_1A	
TIM5_CH2	MCPWM3_1B	
TIM5_CH3	MCPWM3_2A	
TIM5_CH4	MCPWM3_2B	
TIM8_BKIN	UNASSIGNED	Break1 In (Replaced with XBAR)
TIM8_BKIN2	UNASSIGNED	Break2 In (Replaced with XBAR)
TIM8_CH1	MCPWM1_1A, MCPWM4_2A	
TIM8_CH1N	MCPWM1_1B, MCPWM4_2B	
TIM8_CH2	MCPWM1_2A, MCPWM4_3A	
TIM8_CH2N	MCPWM1_2B, MCPWM4_3B	
TIM8_CH3	MCPWM1_3A, MCPWM4_1A	
TIM8_CH3N	MCPWM1_3B, MCPWM4_1B	
TIM8_CH4	MCPWM1_1A, MCPWM4_2A	
TIM8_CH4N	MCPWM1_1B, MCPWM4_2B	
TIM8_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
TIM16_BKIN	UNASSIGNED	Break1 In (Replaced with XBAR)
TIM17_CH1N	MCPWM3_3B	
TIM2_CH1/TIM2_ETR	MCPWM4_1A	
TIM20_BKIN	UNASSIGNED	Break1 In (Replaced with XBAR)
TIM20_BKIN2	UNASSIGNED	Break2 In (Replaced with XBAR)
TIM5_ETR	UNASSIGNED	ETR = External Trigger Input (Replaced by XBAR)
UART		
UART4_RTS_DE	UC3_RTS_POCI	No DE (Driver Enable) Signal in AM13E230x
UART4_DE/UART4_RTS	UC3_RTS_POCI	

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
UART4_CTS	UC1_CTS_CS0	
UART4_CTS/UART4_NSS	UC1_CTS_CS0	
UART4_RX	UC3_RX_SCL_SCLK	
UART4_TX	UC3_TX_SDA_PICO	
UART5_DE/UART5_RTS	UC4_RTS_POCI	
UART5_CTS	UC4_CTS_CS0	
UART5_RTS_DE	UC4_RTS_POCI	
UART5_RX	UC4_RX_SCL_SCLK	
UART5_TX	UC4_TX_SDA_PICO	
UCPD1_CRS_SYNC	UNASSIGNED	No USB/USB Power Delivery Support in AM13E230x
UCPD1_FRSTX	UNASSIGNED	No USB/USB Power Delivery Support in AM13E230x
UCPD1_FRSTX1/UCPD1_FRSTX2	UNASSIGNED	No USB/USB Power Delivery Support in AM13E230x
USART1_CK	UNASSIGNED	No Synchronous UART Clock in AM13E230x
USART1_CTS/USART1_NSS	UC0_CTS_CS0	
USART1_DE/USART1_RTS	UC0_RTS_POCI	
USART1_CTS	UC0_CTS_CS0	
USART1_RTS_DE	UC0_RTS_POCI	
USART1_RX	UC0_RX_SCL_SCLK	
USART1_TX	UC0_TX_SDA_PICO	
USART2_CK	UNASSIGNED	No Synchronous UART Clock in AM13E230x
USART2_CTS/USART2_NSS	UC1_CTS_CS0	
USART2_DE/USART2_RTS	UC1_RTS_POCI	
USART2_CTS	UC1_CTS_CS0	
USART2_RTS_DE	UC1_RTS_POCI	
USART2_RX	UC1_RX_SCL_SCLK	
USART2_TX	UC1_TX_SDA_PICO	
USART3_CK	UNASSIGNED	No Synchronous UART Clock in AM13E230x
USART3_CTS/USART3_NSS	UC2_CTS	
USART3_DE/USART3_RTS	UC2_RTS	
USART3_CTS	UC2_CTS	
USART3_RTS	UC2_RTS	
USART3_RTS_DE	UC2_RTS	
USART3_RX	UC2_RX_SCL	
USART3_TX	UC2_TX_SDA	
DEBUG		
CRS_SYNC	UNASSIGNED	No CRS = Clock Recovery System in AM13E230x
SYS_JTDI	DEBUG_JTDI	
SYS_JTDO-SWO	DEBUG_JTDO-SWO	
SYS_JTRST	UNASSIGNED	No JTAG TRST Signal in AM13E230x
RCC_MCO	XCLKOUT	Replaced by XCLKOUT
RTC_OUT2	UNASSIGNED	No RTC in AM13E230x
RTC_REFIN	UNASSIGNED	No RTC in AM13E230x
SYS_JTCK-SWCLK	DEBUG_JTCK_SWCLK	JTAG Clock / SW Clock
SYS_SWCLK-JTCK	DEBUG_JTCK_SWCLK	JTAG Clock / SW Clock

Table 2-2. STM32G474x Alternate Function vs. AM13E230x Signal (continued)

STM32G474x Alternate Function Name	AM13E230x Signal Name	Notes
SYS_JTMS-SWDIO	DEBUG_TMS_SWDIO	JTAG Test Mode Select / SW Data IO
SYS_SWDIO-JTMS	DEBUG_TMS_SWDIO	JTAG Test Mode Select / SW Data IO
SYS_TRACECLK	TRACE_CLK	Trace Clock
SYS_TRACED0	TRACE_DATA0	Trace Data0
SYS_TRACED1	TRACE_DATA1	Trace Data1
SYS_TRACED2	TRACE_DATA2	Trace Data2
SYS_TRACED3	TRACE_DATA3	Trace Data3

2.1.3 STM32G474x Additional Functions and AM13E230x Analog Functions

The following table describes the Additional Function signal names on STM32G474x and equivalent Analog Function signal names on AM13E230x.

Table 2-3. STM32G474x Additional Function / AM13E230x Analog Function

STM32G474x Additional Function Name	AM13E230x Analog Function Name	Notes
OPAMP6_VOUT	PGA2_OUT	
OPAMP6_VINP	PGA2_P	
OPAMP4_VINP	PGA0_P	
OPAMP5_VINP	PGA1_P	
RTC_OUT1	UNASSIGNED	No RTC/TAMP in AM13E230x
OSC32_IN	UNASSIGNED	No 32KHz LFXTAL in AM13E230x
OSC32_OUT	UNASSIGNED	No 32KHz LFXTAL in AM13E230x
OPAMP6_VINM	PGA2_M	
RTC_TAMP2	UNASSIGNED	No RTC/TAMP in AM13E230x
OPAMP3_VINP	PGA2_P	
WKUP4/LSCO	UNASSIGNED	
ADC1_IN10	A0_10	
ADC2_IN10	A1_10	
NRST	NRST	No Functional Muxing/Signals on NRST pin in AM13E230x
ADC12_IN6	A0_6/A1_6/CMP2	
ADC12_IN7	A0_7/A1_7/CMP2	
ADC12_IN8	A0_8/A1_8	
ADC12_IN9	A0_9/A1_9	
OPAMP2_VINM	PGA1_M	
ADC12_IN1	A0_1/A1_1/CMP0/CMP2	
ADC12_IN2	A0_2/A1_2/CMP0/PGA0_P0/PGA1_M0/ PGA2_P0	
ADC1_IN3	A0_3/CMP1/PGA0_OUT	
OPAMP2_VINP	PGA1_P	
ADC1_IN4	A0_4/CMP1/PGA0_M0	
ADC2_IN17	A1_17/CMP2_DACL/CMP0	
ADC2_IN13	A1_13/CMP2_DACL/CMP1	
ADC2_IN3	A1_3/CMP3_DACL/PGA1_OUT	
ADC2_IN4	A1_4/CMP1/PGA0_P1/PGA1_P0	
ADC2_IN5	A1_5	
ADC2_IN11	A1_11/PGA1_M1/PGA2_M0	
ADC3_IN12/ ADC1_IN15	A0_15/A2_12/A0_15/CMP3/PGA1_P2/ PGA2_P1	

Table 2-3. STM32G474x Additional Function / AM13E230x Analog Function (continued)

STM32G474x Additional Function Name	AM13E230x Analog Function Name	Notes
ADC3_IN1/ ADC1_IN12	A0_12/A2_1/CMP0/PGA1_M2/PGA2_OUT	
ADC2_IN12	A1_12/CMP3/PGA2_M1	
VREFBUF_OUT	VREFHI	
ADC3_IN4	A2_4/CMP3	
ADC345_IN6	A0_23/A1_23/A2_6/CMP3/ADCINCAL0	
ADC3_IN2	A2_2	
ADC345_IN14	A0_23/A1_23/A2_14	
ADC345_IN15	A0_24/A1_24/A2_15	
ADC345_IN16	A0_25/A1_25/A2_16	
ADC3_IN3	A2_3	
ADC4_IN1	A0_18	
ADC4_IN2	A0_19	
COMP5_INM	A2_17/CMP0/PGA2_M2	
ADC12_IN14	A0_14/A1_14/CMP1/CMP1/PGA0_P2/ PGA1_OUT	
ADC4_IN3/ ADC1_IN11	A0_11/CMP2/PGA0_OUT/PGA1_P3	
ADC3_IN5	A2_5/CMP0/PGA2_P2/PGA0_P3/PGA1_P4	
ADC4_IN4/ ADC1_IN5	A0_5/CMP2/PGA1_P5/PGA2_P3	
ADC4_IN5/ ADC2_IN15	A1_15/CMP1/PGA0_P4/PGA1_OUT	
ADC4_IN12/ ADC5_IN12	A0_21/A1_21/PGA0_M1	
ADC4_IN13/ ADC5_IN13	A0_22/A1_22/PGA1_P6	
ADC345_IN7	A0_26/A1_26/A2_7/CMP1	
ADC345_IN8	A0_27/A1_27/A2_8/CMP1	
ADC345_IN9	A1_28/A0_28/A2_9/CMP0	
ADC345_IN10	A0_29/A1_29/A2_10/CMP0	
ADC345_IN11	A0_30/A1_30/A2_11/CMP2	
COMP7_INM	A0_20/A1_20/CMP2	
ADC5_IN1	A1_18/PGA0_OUT	
ADC5_IN2	A1_19	
UCPD1_DBCC2	UNASSIGNED	No USB PD in AM13E230x
USB_DM	UNASSIGNED	No USB in AM13E230x
USB_DP	UNASSIGNED	No USB in AM13E230x
UCPD1_CC2	UNASSIGNED	No USB PD in AM13E230x
UCPD1_CC1	UNASSIGNED	No USB PD in AM13E230x
RTC_TAMP3	UNASSIGNED	No RTC/TAMP in AM13E230x
RTC_TAMP1	UNASSIGNED	No RTC/TAMP in AM13E230x
OSC_IN	X1	
COMP3_INM	CMP2_M	
COMP3_INP	CMP3_P	
COMP1_INM	CMP1_M	
COMP1_INP	CMP1_P	
COMP2_INM	CMP2_M	
COMP2_INP	CMP2_P	
DAC1_OUT1	CMP2_DACL	
DAC1_OUT2	CMP2_DACL	
DAC2_OUT1	CMP3_DACL	
OPAMP1_VINM	PGA0_M	

Table 2-3. STM32G474x Additional Function / AM13E230x Analog Function (continued)

STM32G474x Additional Function Name	AM13E230x Analog Function Name	Notes
COMP4_INP	CMP4_P	
COMP4_INM	CMP4_M	
OPAMP3_VINM	PGA2_M	
COMP6_INP	CMP2_P	
COMP7_INM	CMP3_M	
COMP5_INP	CMP1_P	
COMP7_INP	CMP3_P	
COMP6_INM	CMP2_M	
OPAMP4_VINM	PGA0_VNM	
COMP5_INM	CMP1_M	
OPAMP5_VOUT	PGA1_OUT	
UCPD1_DBCC1	UNASSIGNED	
PVD_IN	UNASSIGNED	
RTC_TS	UNASSIGNED	
OSC_OUT	X2	
OPAMP1_VINP	PGA0_P	
OPAMP1_VOUT	PGA0_OUT	
OPAMP1_VINM	PGA0_M	
OPAMP2_VOUT	PGA1_OUT	
OPAMP3_VOUT	PGA2_OUT	
OPAMP4_VOUT	PGA0_OUT	
OPAMP5_VINM	PGA1_M	

2.2 Device Pinout Comparison by Package Type

All AM13E230x device package types are designed to be pin-to-pin compatible with the equivalent package for the STM32G474x device. The following diagrams detail the pin compatibilites and differences across all STM32G474x-compatible device packages.

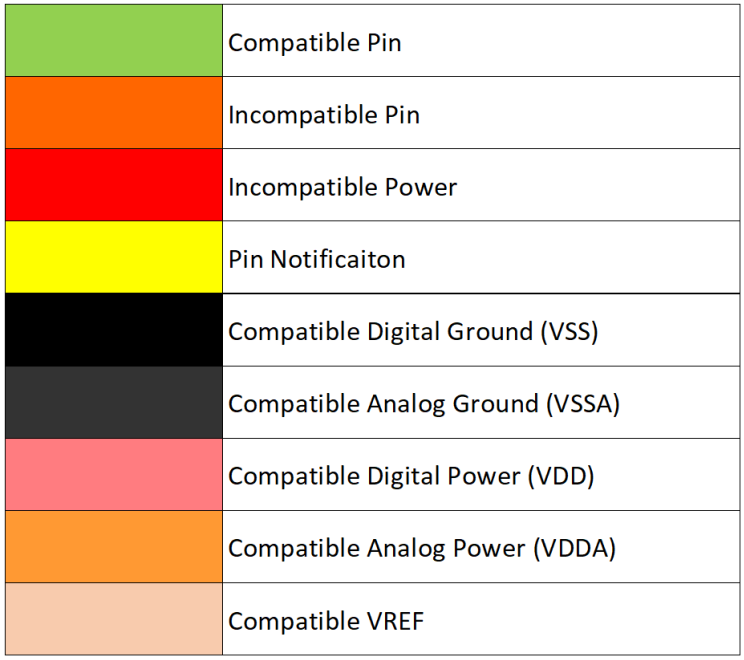


Figure 2-1. Legend

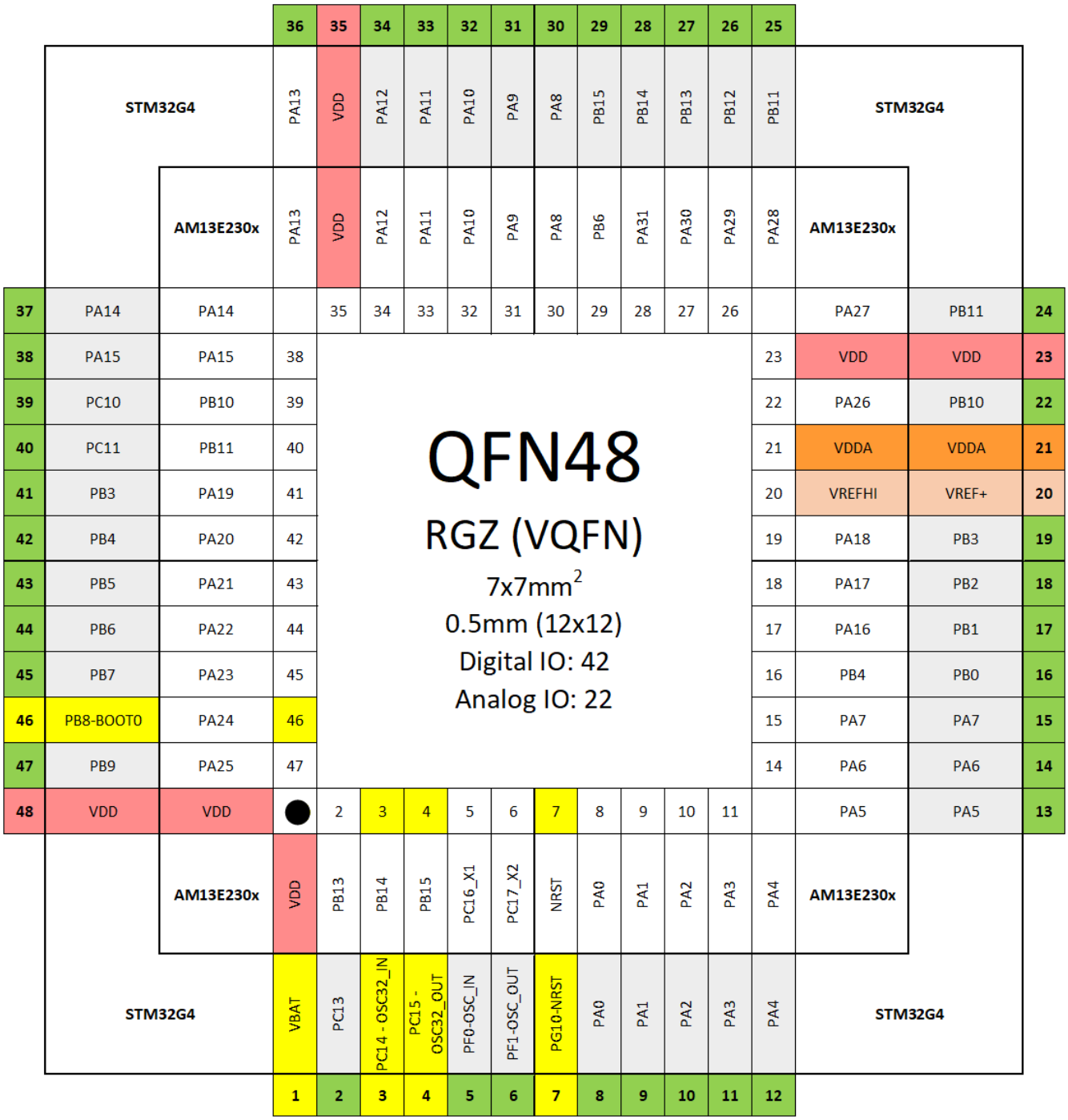


Figure 2-2. 48-Pin QFN: AM13E230x (RGZ) and STM32G474x UFQFPN48 Pin-Overlay

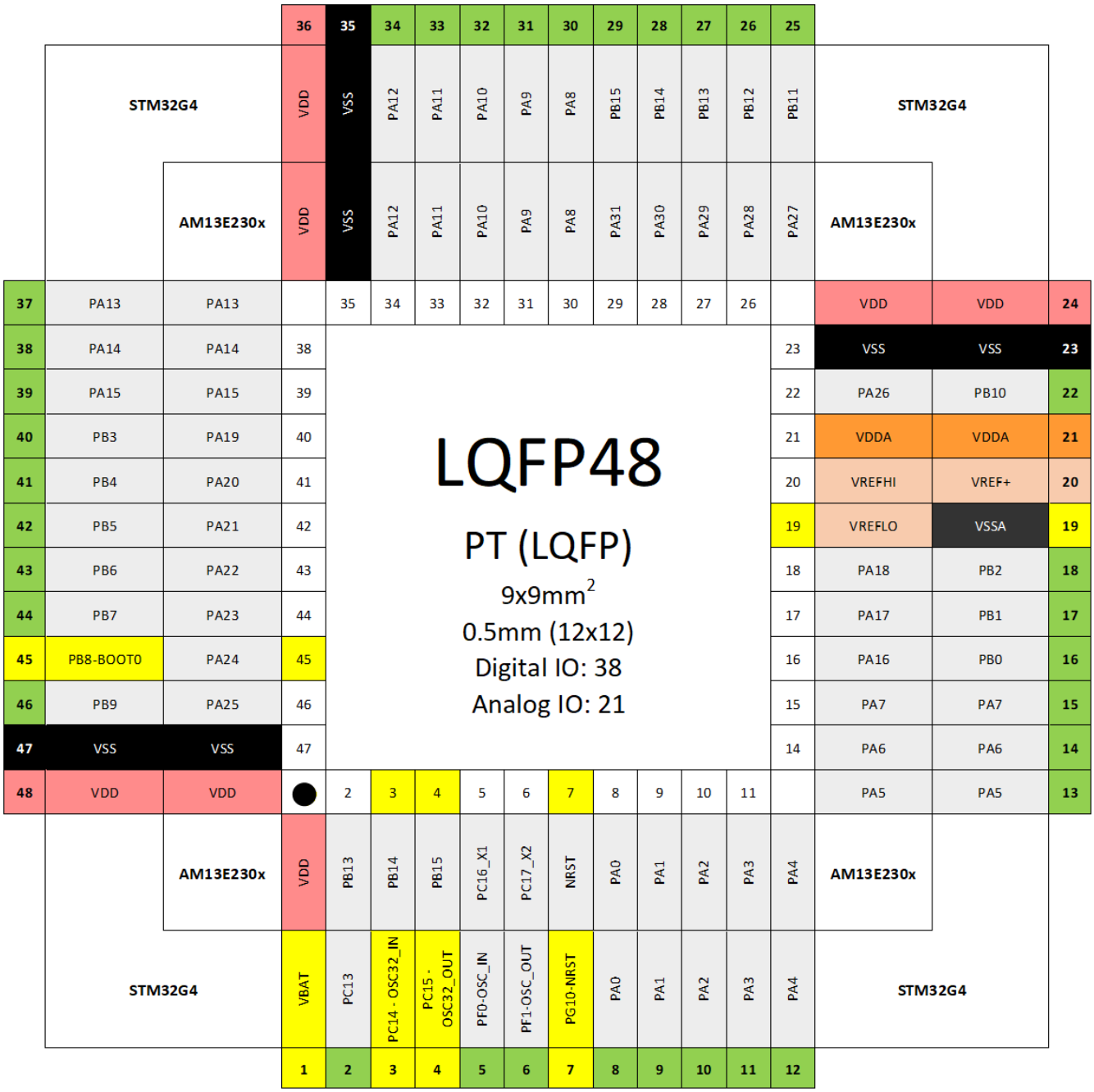


Figure 2-3. 48-Pin QFP: AM13E230x (PT) and STM32G474x LQFP64 Pin-Overlay

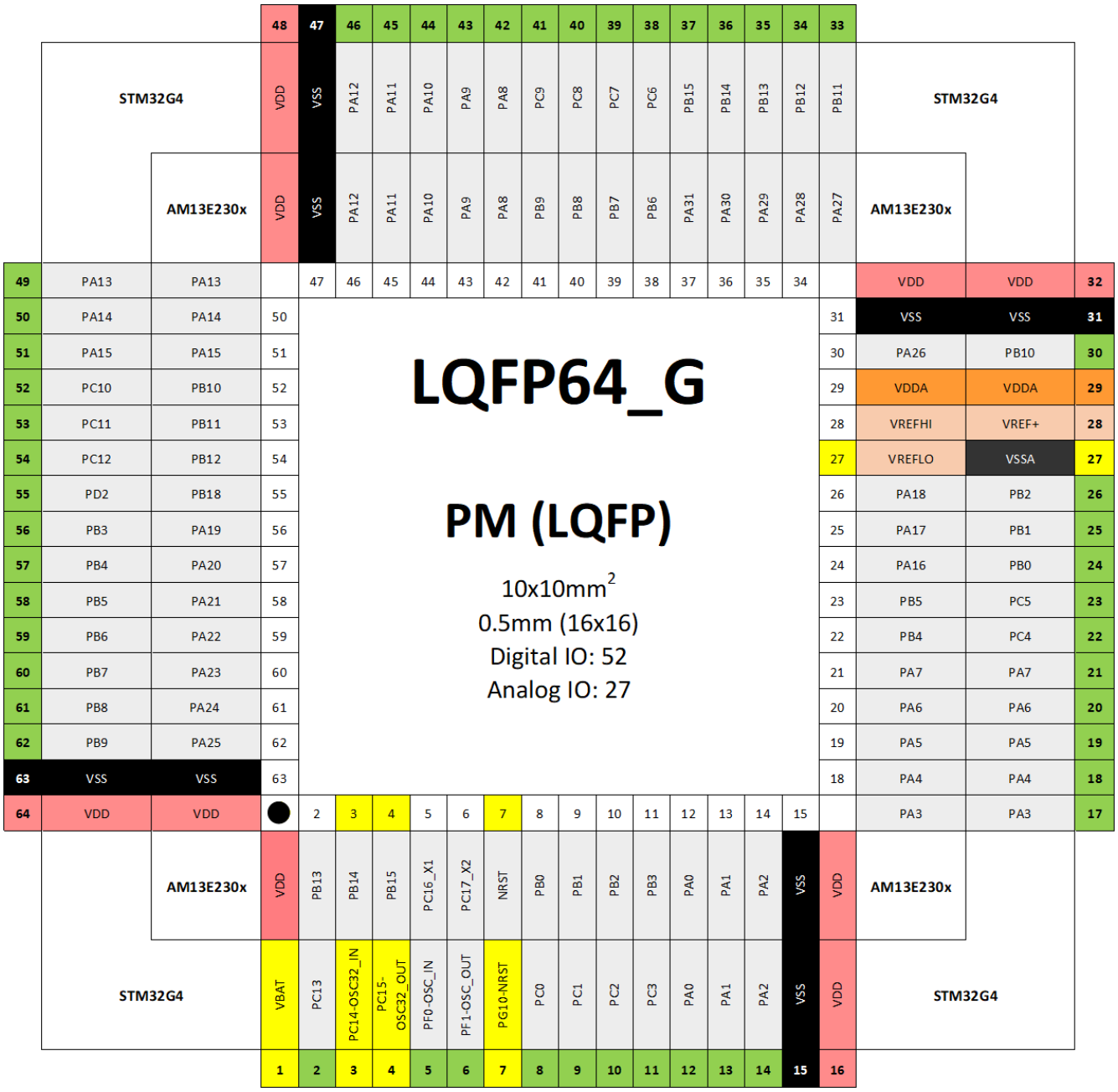


Figure 2-4. 64_G-Pin QFP: AM13E230x (PM) and STM32G474x LQFP64 Pin-Overlay

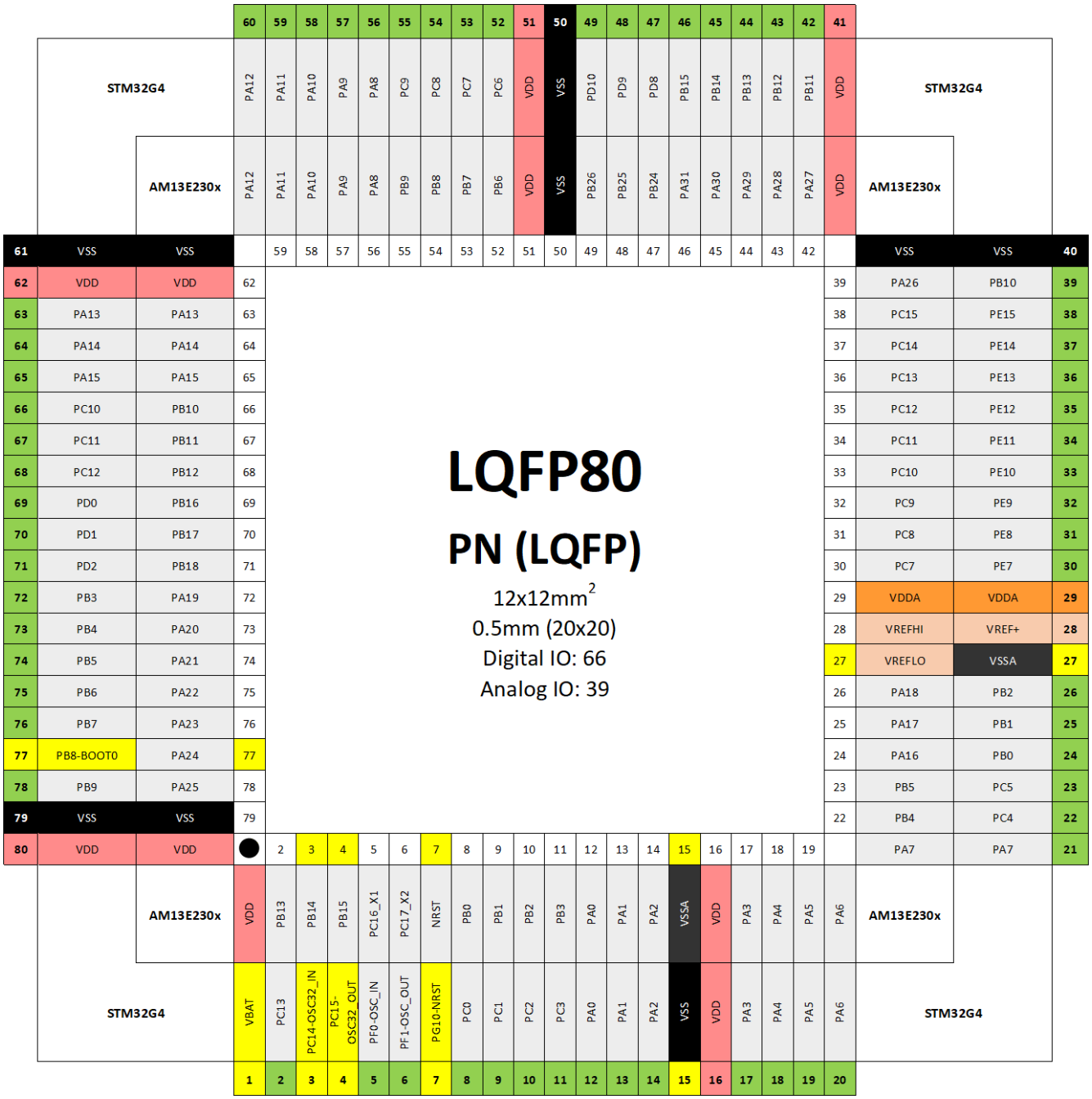


Figure 2-5. 80-Pin QFP: AM13E230x (PN) and STM32G474x LQFP80 Pin-Overlay

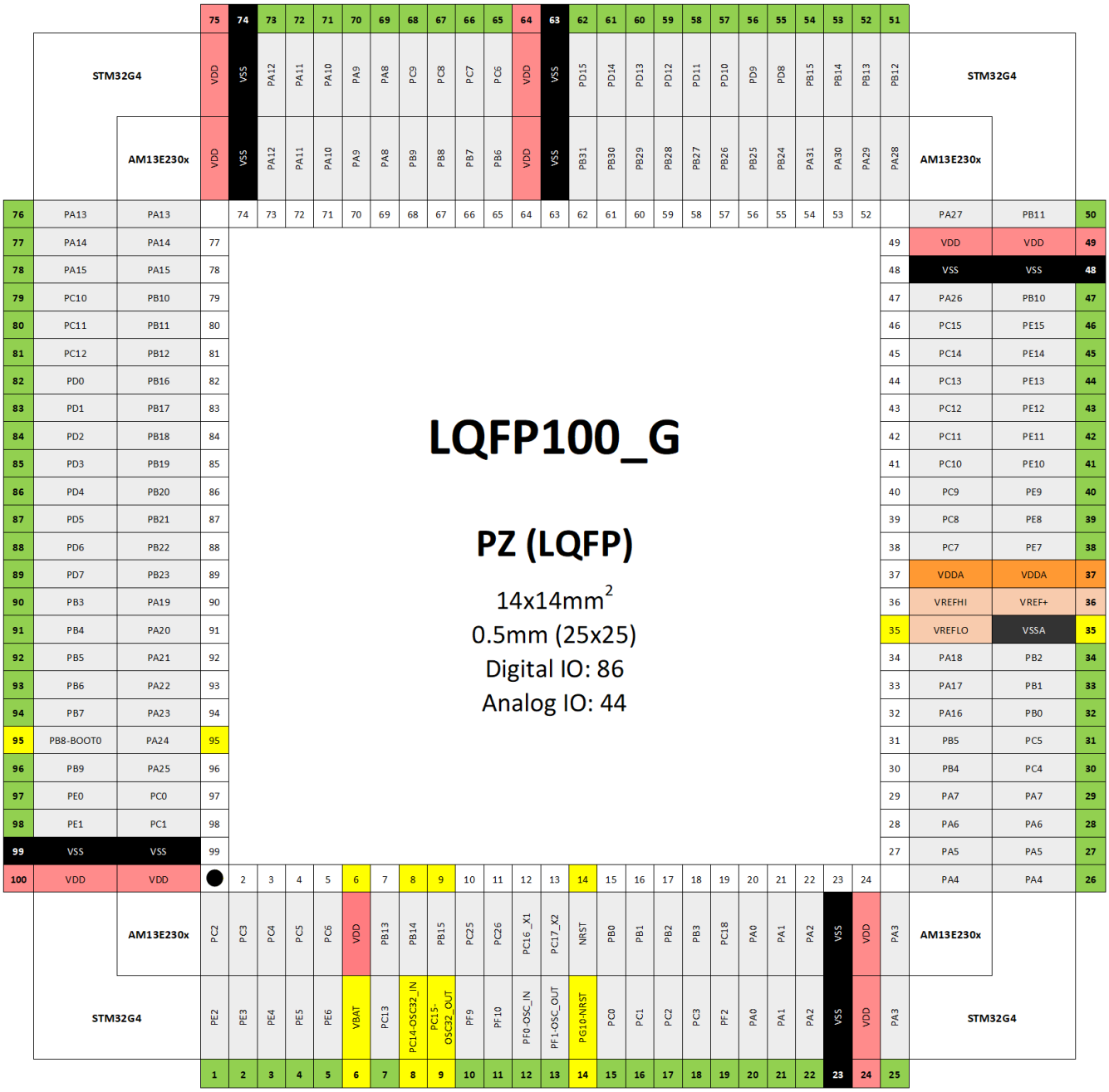


Figure 2-6. 100_G-Pin QFP: AM13E230x (PZ) and STM32G474x LQFP100 Pin-Overlay

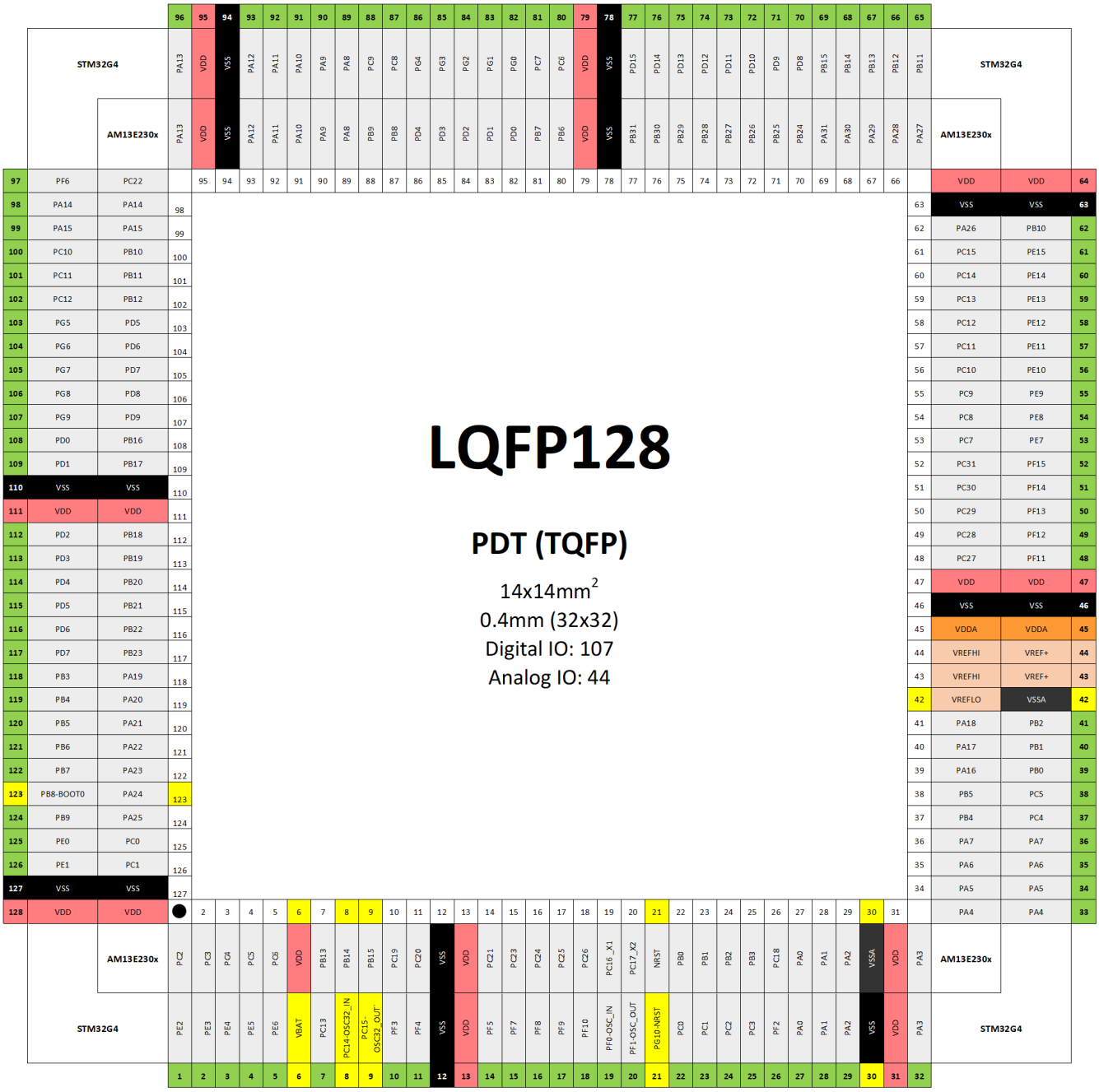


Figure 2-7. 128-Pin QFP: AM13E230x (PDT) and STM32G474x LQFP128 Pin-Overlay

2.3 Block Diagram Comparison of STM32G474x and AM13E230x

Figure 2-8 shows the device block diagram for the STM32G474x device.

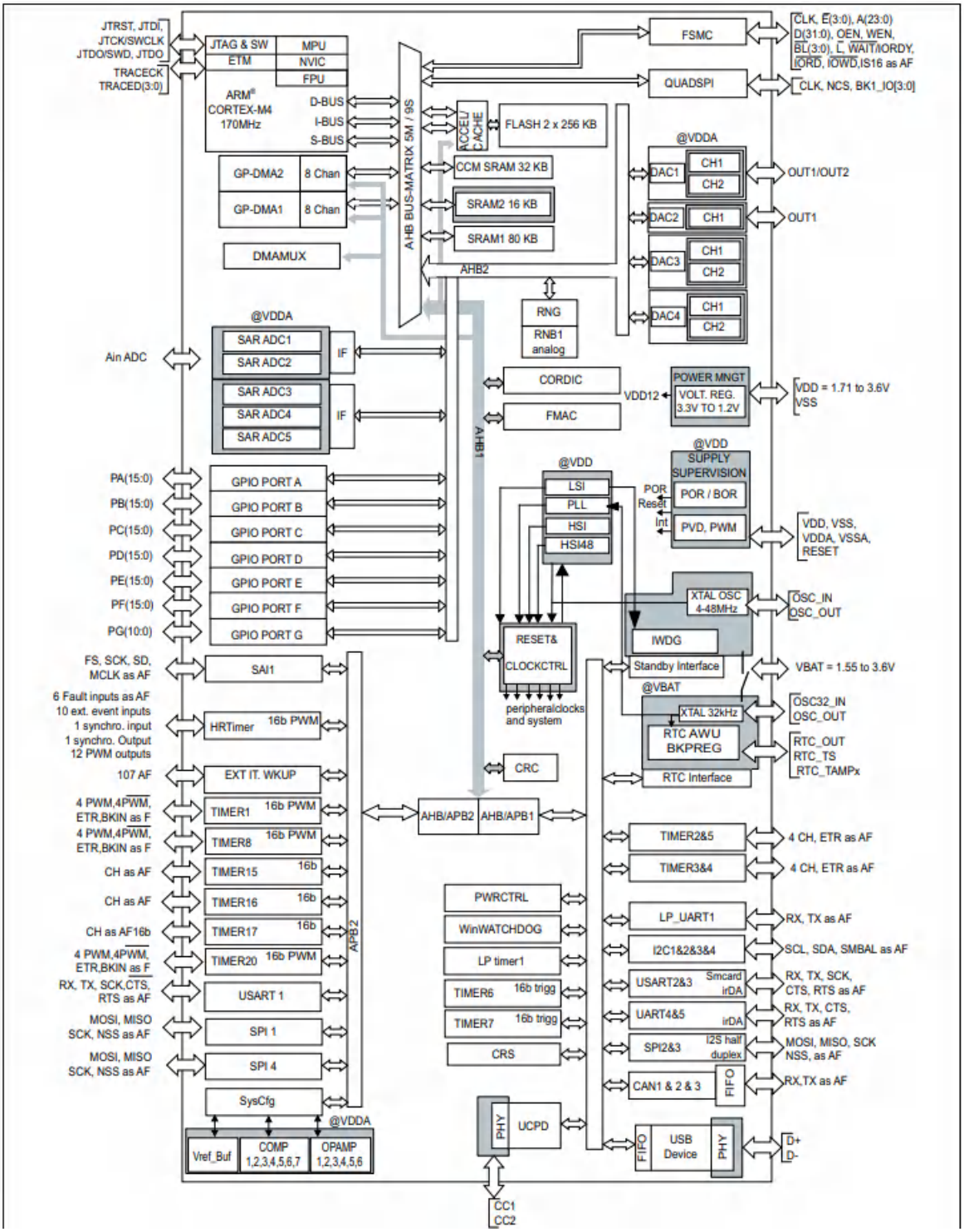


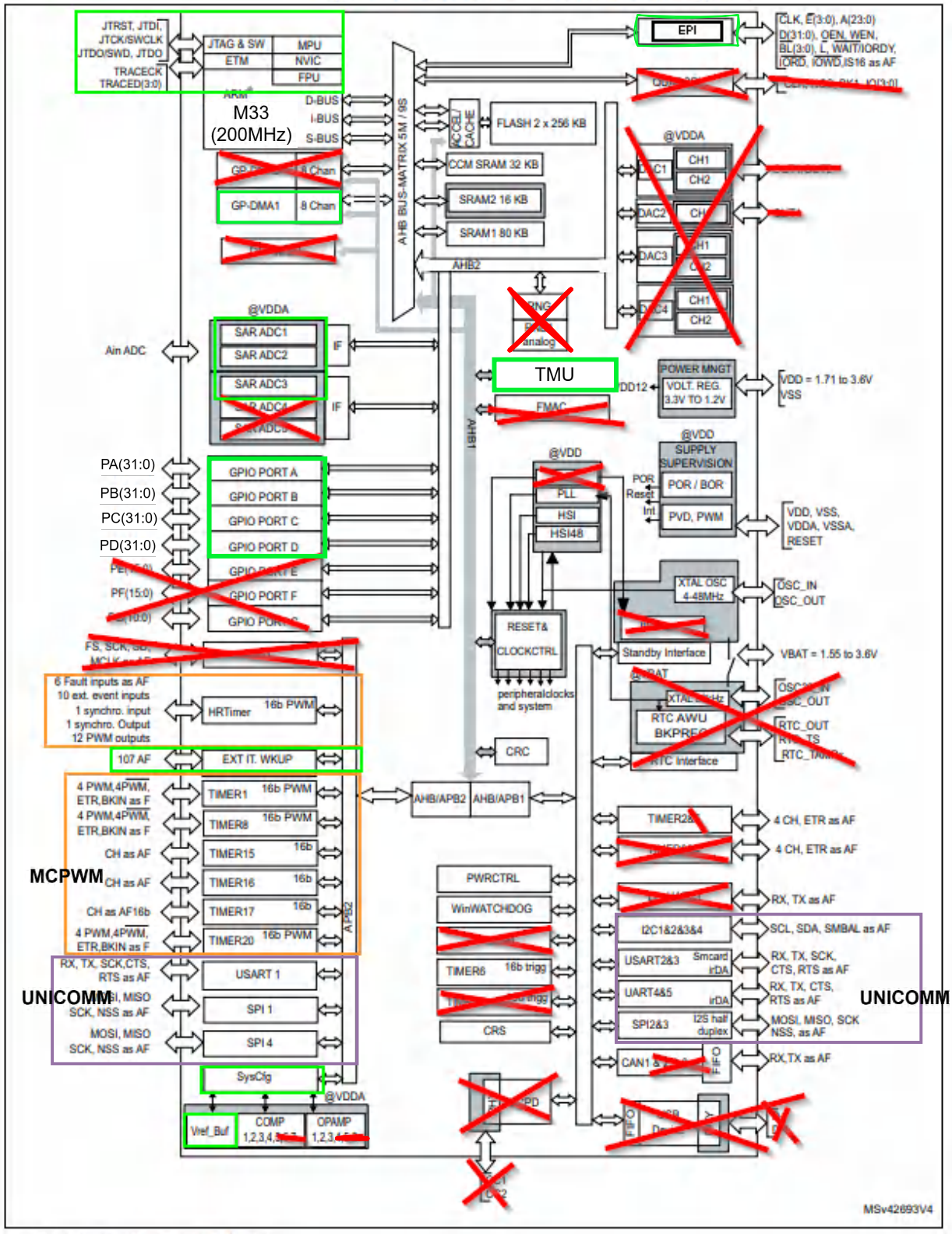
Figure 2-8. STM32G474x Block Diagram

Figure 2-9 shows the STM32G474x Block Diagram with annotations to show the differences between the two families of MCU devices.

- RED crossed-out blocks indicate peripherals/features that are not present on the AM13E230x device

- GREEN outlined blocks indicate equivalent peripherals/features on the AM13E230x device
  - Some GREEN outlined blocks have text overlays to show the AM13E230x peripheral name
- ORANGE outlined blocks show the equivalent timer signals on STM32G474x are MCPWM on AM13E230x
- PURPLE outlined blocks show the equivalent serial communications interfaces on STM32G474x are part of the UNICOMM interface on AM13E230x

Figure 1. STM32G474xB/xC/xE block diagram



1. AF: alternate function on I/O pins.

Figure 2-9. STM32G474x Block Diagram with AM13E230x Annotations

3 Core Architecture Comparison

3.1 CPU

The key difference between STM32G474x and AM13E230x devices is their core CPU. STM32G474x has an ARM Cortex-M4 core, and AM13E230x has an ARM Cortex-M33 core. As a result, the maximum core speed differs between the two devices, which has a profound affect on the capabilities and features of each device family.

Table 3-1. Comparison of CPU Feature Sets

Feature	STM32G474x	AM13E230x
Architecture	Arm® Cortex®-M4 core	Arm® Cortex®-M33
Maximum MCLK	170 MHz	200 MHz
CPU instruction cache	32 cache lines of 4 x 64 or 2 x 128 bits	1 KB of cache
Memory protection unit (MPU)	Yes	Yes
System timer (SYSTICK)	Yes	Yes
Hardware Accelerator	FMAC, AES	TMU, NPU, CRC, AES
Hardware Breakpoints / Watchpoints	8 HW breakpoints 8 HW watchpoints	8 HW breakpoints 8 HW watchpoints
Boot routine storage	Flash (system memory)	ROM
Bootstrap loader storage	System memory	ROM
Bootloader interface support	UART, I2C, SPI, USB, FDCAN	UART, MCAN, I2C
DMA	Yes	Yes

3.2 Embedded Memory Comparison

3.2.1 Flash Features

The following section details the Flash differences between STM32G474x and AM13E230x.

Table 3-2. Flash Feature Comparison

Features	STM32G474x	AM13E230x
Flash memory	• Up to 512KB	• Up to 512KB
Memory organization	• Single bank mode (read width of 128 bits) • Dual bank mode (read width of 64 bits)	• 1 bank – devices up to 256KB • 2 banks – devices with >256KB
Flash Wait States	• Default: 1 • Configurable: 0 to 4	• Default: 2 • Configurable: 1 to 16
Flash Word Size	• 64 bits + 8 ECC bits	• 128-bit flash word size (144-bit when ECC is present)
Programming Resolution	• 64 bits (Double word)	• 128 bit word
Multi-Word Programming	• 32 words (256 bytes)	• 2 words (32 bytes) • 4 words (64 bytes)
Erase	• Page erase • Bank erase • Mass erase (both banks)	• Sector erase (1KB) • Bank (up to 256KB) Erase
Write Protection	• Single bank mode - up to 4 areas can be defined • Dual bank mode - up to 2 areas can be defined	• Static - latched at boot and held until Power on Reset • Dynamic - configurable at runtime
Read Protection	• Yes	• No

Table 3-2. Flash Feature Comparison (continued)

Features	STM32G474x	AM13E230x
Flash Memory Read Operations	• 64 bits	• 128 bits
Error code correction (ECC)	• 8 bits per 64-bit double-word	• 16 bits per 128-bit word – 8 ECC bits for upper 64b – 8 ECC bits for lower 64b
Securable Memory Area	• Single bank mode - 1 for all memory • Dual bank mode - 1 per bank	• No
Info Memory	• Yes	• Yes (NONMAIN)
OTP Data Region	• 1KB (128b double word) OTP (one-time programmable) bytes for user data	• Yes (in NONMAIN)
Prefetch	• Yes	• Yes
CPU Instruction Cache	• 32 cache lines of 4 x 64 or 2 x 128 bits on ICode (1 KB RAM)	• 1 KB of cache

The AM13E230x MCUs provide up to 512KB of embedded flash program memory (2 banks of up to 256KB) with built-in error correction code (ECC).

3.2.2 Flash Organization

The flash memory is used for storing application code and data, the device boot configuration, and parameters which are preprogrammed by TI from the factory. The flash memory is organized into one or more banks, and the memory in each bank is further mapped into one or more logical memory regions and assigned system address space for use by the application.

Memory Banks

The nonvolatile memory system provides support for up to 4 flash memory banks (enumerated as BANK0 through BANK3). The number of flash banks present is device dependent. On AM13E230x devices, a program/erase operation on a bank will also stall read requests issued to the bank which is executing the program/erase operation, but it will not stall read requests issued to any other bank. As such, the presence of multiple banks enables application cases such as:

- Dual-image firmware updates (an application can execute code out of one flash bank while a second image is programmed to a second symmetrical flash bank without stalling the application execution)
- EEPROM emulation (an application can execute code out of one flash bank while a second flash bank is used for writing data without stalling the application execution)

Flash Memory Regions

The memory within each bank is mapped to one or more logical regions based upon the functions that the memory in each bank supports. There are four regions:

- FACTORY – Device Id and other parameters
- NONMAIN – Device boot configuration (BCR and BSL)
- MAIN – Application code and data
- DATA – Data or EEPROM emulation

Devices with one bank implement the FACTORY, NONMAIN, and MAIN regions on BANK0 (the only bank present), and the data region is not available. Devices with multiple banks also implement FACTORY, NONMAIN, and MAIN regions on BANK0, but include additional banks (BANK1 through BANK3) that can implement MAIN or DATA regions. All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software.

3.2.3 Embedded SRAM

This section details the differences between the on-device SRAM for STM32G474x and AM13E230x.

Table 3-3. Comparison of SRAM Features

Feature	STM32G474x	AM13E230x
SRAM Size	Up to 128 Kbytes SRAM organized by: • 80 Kbytes SRAM1 • 16 Kbytes SRAM2 • 32 Kbytes CCM SRAM	Up to 128 KB SRAM, organized into 4 banks of 32KB • BANK0: 32KB • BANK1: 32KB • BANK2: 32KB • BANK3: 32KB
Zero wait states at maximum CPU clock frequency	Yes	Yes
Access resolution	8 bits (byte), 16 bits (half-word), 32 bits (word)	8 bits (byte), 16 bits (half-word), 32 bits (word)
Parity check	Yes	Yes (All blocks have hardware parity support)

3.3 Power Up and Reset Summary and Comparison

Similar to STM32G474x devices, AM13E230x devices have a minimum operating voltage and have modules in place to ensure that the device starts up properly by holding the device or portions of the device in a reset state. The following table shows a comparison on how this is done between the two families and what modules control the power up process and reset across the families.

Table 3-4. Power-Up Voltage Level-Based Resets

Feature	STM32G474x	AM13E230x
Module governing power/reset	PWR (power) and RCC (Reset and Clock Control) modules	Power Management Unit (PMU) and Clock Management Unit (CKM)
POR (Power-On Reset)	Complete device reset. First level voltage release for power up. Lowest voltage level release for power down.	First step in the boot process. Used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are then used to determine if the device supply has reached a sufficient level for the device to run correctly
BOR (Brownout Reset)	Sometimes programmable. Set voltage level that releases reset state on power up, or resets device on power down.	Ensures that the external supply to the device is maintained at the proper level to enable the correct operation of internal circuits, including the core regulator. The BOR threshold is not programmable and is derived from the internal bandgap circuit. The threshold is fixed and always higher than the POR threshold.
PVD (Programmable Voltage Detector)	Configurable voltage monitor that can provide interrupts	N/A

STM32G474x defines different reset domains, while AM13E230x devices have different levels of reset states. For AM13E230x devices the reset levels have a set order. When a level is triggered, all subsequent reset levels are asserted until the device is released into RUN mode. The following table gives a brief description and comparison between STM32G474x reset domains and AM13E230x reset states. Figure 3-1 shows the relationship between all of the AM13E23x reset states.

Table 3-5. AM13E230x Reset States vs STM32G474x Reset Domains

STM32G474x Reset States		AM13E230x Reset Domains	
Reset Domain	**Triggers**	**Reset Type**	**Triggers**
Power Reset • All registers reset except those outside VCORE domain	• POR, BOR • Exits from Standby or Shutdown modes	Power-On Reset (POR) • Resets shutdown memory, re-enables NRST and SWD, triggers BOR	• POR voltage level threshold • SW-based trigger • NRST pin held low for >1s
		Brownout Reset (BOR) • Resets PMU, VCORE, and associated logic. Triggers BOOTRST	• POR or BOR voltage level threshold • Exit from SHUTDOWN mode
No equivalent to AM13E230x BOOTRST. Boot Configuration is read on the fourth clock cycle of SYSCLK after a Power Reset.		Boot Reset (BOOTRST) • Executes boot configuration routine • Resets majority of core logic and registers (includes RTC, clock, and IO configurations) • SRAM power cycled and memory is lost • Triggers SYSRST	• BOR or software trigger • Fatal clock failure • NRST held low for <1s
System Reset • Sets all registers to their reset values unless specified otherwise in the register description	• Source is identified by checking the reset flags in the Control/Status register, RCC_CSR	System Reset (SYSRST) • Resets CPU state and all peripherals except RTC, LFCLK, and SYSOSC frequency correction loop • Device enters RUN mode on exit	• BOOTRST • BSL entry or exit • Watchdog timer • Software trigger • Debug subsystem
No equivalent to AM13E230x CPURST.		CPU Reset (CPURST) • Resets CPU logic only • Peripheral states are not affected	• Software and debug subsystem triggers only
RTC Reset • Resets only the LSE oscillator, RTC, backup registers, and RCC RTC domain control register	• Software or VDD/VBAT power on if both supplies were previously powered off	N/A	

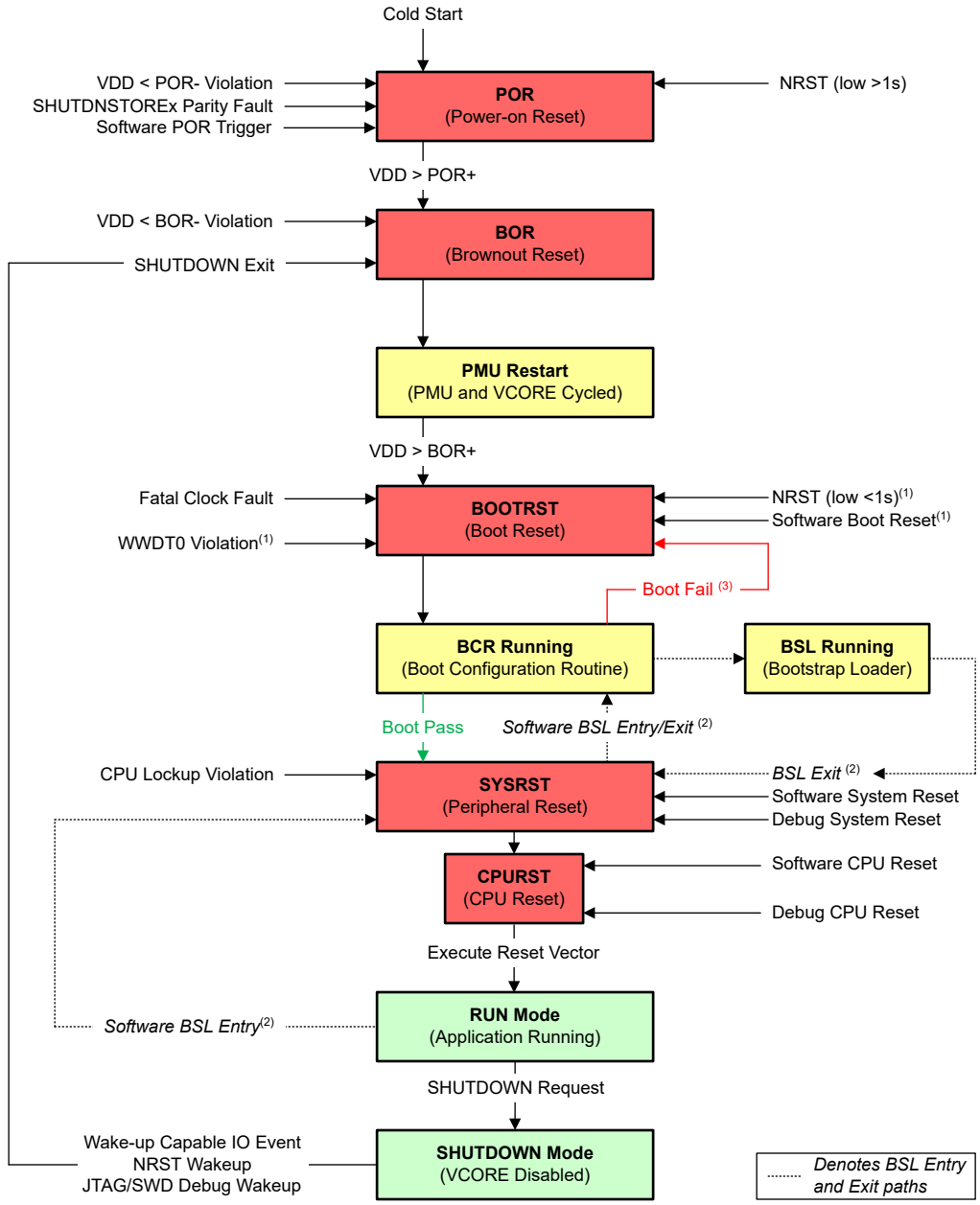


Figure 3-1. AM13E230x Reset Levels

3.4 Clocks Summary and Comparison

AM13E230x and STM32G474x rely on internal and external clocks and oscillators to generate low to high frequency clocks for use by the device subsystems. This section details the relevant clocks and oscillators for both devices.

Table 3-6. Oscillator Comparisons

Oscillator Type	STM32G474x	AM13E230x
Internal Oscillators	HSI16 - 16MHz • High speed Internal 16MHz RC oscillator	SYSOSC - 32MHz • System oscillator
	HSI48 - 48MHz • High speed Internal 48 MHz Internal oscillator)	No direct equivalent
	MSI - 100KHz to 48MHz • Multi speed Internal RC oscillator	No direct equivalent
	LSI RC - 32KHz to 40KHz • Low Speed Internal RC oscillator	LFOSC - 32.768KHz • Low-frequency oscillator
	PLL - up to 170MHz	SYSPLL - up to 200MHz • System Phase-Locked Loop with programmable frequency
External Oscillators	HSE - 4MHz to 48MHz • High speed external clock (crystal/ ceramic resonator oscillator)	XTAL - 10MHz to 25MHz • External crystal oscillator
		XTAL SE - 4MHz to 48MHz • External single-ended oscillator
		HFCLK_IN - 4MHz to 48MHz • External digital clock
	LSE - 32.768KHz • Low Speed External crystal	No direct equivalent

Table 3-7. Clock Comparison

Clock Type	STM32G474x Clock	AM13E230x Clock
System Clocks	SYSCLK	MCLK - up to 200MHz • Main system clock for PD1 peripherals/bus
	HCLK	CPUCLK - up to 200MHz • Derived from MCLK
	N/A	ULPCLK - up to 50MHz • Bus clock for PD0 peripherals
	LSI clock	LFCLK - 32KHz • Low-frequency clock
	N/A	HFCLK • Generated by XTAL (SE) or HFCLK_IN
	HCLK	HSCLK • High-speed clock
Peripheral-Specific Clocks	FDCAN clock	CAN_CLK • CAN-FD functional clock
External Clocks	OSC_OUT/OSC32_OUT	CLK_OUT • Clock output unit

Table 3-8. Peripheral Clock Sources

Peripheral	STM32G474 Clock Source	AM13E230x Clock Source
ADC	SYSCLK, PLLPCLK	MCLK
RTC	HSE/32, LSE or LSI	-
WATCHDOG	LSI	LFCLK
CAN	HSE, PLLQCLK, PCLK	CANCLK
UART	SYSCLK, HSI16, LSE, APB1 or APB2	MCLKDIV2
I2C	SYSCLK, HSI16, APB1 clock (PCLK1)	MCLKDIV2
SPI	-	MCLKDIV2
TIMERS	Defined by hardware	MCLKDIV2

3.5 Operating Modes Summary and Comparison

Two core power domains are provided on the AM13E230x device: PD1 and PD0. PD1 ('switching' power domain) is always powered in RUN and SLEEP modes and switched off in STOP and STANDBY modes. PD0 ('always on' domain) is always powered in RUN, SLEEP, STOP and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode. The PD1 domain includes the CPU subsystem, DMA, SRAM, and PD1 peripheral buses: Fast Peripheral Interconnect, Peripheral Interconnect, and CPU Interconnect which run from MCLK, MCLK/2, and MCLK/4, respectively.

- The PD0 domain includes the PD0 peripherals and PD0 bus segment (PD0 Interconnect) which runs at MCLK/4 in RUN and SLEEP mode, 4MHz in STOP mode, and 32kHz in STANDBY mode. This clock source, derived from MCLK/4 is referred to as ULPCLK. The PD0 domain is powered in all modes except SHUTDOWN and can be thought of as an "always-on" domain
- The VDDC domain includes both PD1 and PD0

Operating Modes Comparison

STM32G474 devices have similar operating modes. The table below gives a brief comparison between STM32G474x and AM13E23x devices.

Table 3-9. Operating Modes Comparison Between STM32G474x and AM13E23x Devices

STM32G474x		AM13E230x	
Mode	**Description**	**Mode**	**Description**
Run	• Primary operating state for executing code • Power consumption can be reduced by slowing down system clocks or gating clocks to unused peripherals	RUN	• The CPU is actively executing code and any peripheral can be enabled. • MCLK and CPUCLK run from a fast clock source (SYSOSC, HFCLK, or SYSPLL) • The VDDC domain is supplied by the on-chip MAIN LDO • All functions are available at the highest frequency in this mode • If needed, software can be configured to a lower PLL frequency or lower system clock frequency to save dynamic power
Low-power run	• CPU clock frequency is reduced below 2 MHz • The code is executed from SRAM or Flash memory • The on-chip regulator is in low-power mode to minimize the regulator's operating current		
Sleep	• CPU is disabled (clock gated)	SLEEP	• Configuration is same as RUN, but the CPU is disabled (clock gated)
Low-power sleep	• Enter this mode from *Low-power run mode* • CPU clock disabled • System reverts to *Low-power run mode* when wakeup is triggered		

Table 3-9. Operating Modes Comparison Between STM32G474x and AM13E23x Devices (continued)

STM32G474x			AM13E230x		
Mode		**Description**	**Mode**		**Description**
Stop	Stop 0	• Lowest power consumption while retaining SRAM and register contents • All clocks in VCORE domain are stopped	STOP		• PD1 power domain is switched off, PD1 peripherals are disabled and kept in retention • CPU, DMA, SRAM, FLASH, PLL, XTAL retained • VDDC voltage reduced to 10%, PD0 peripherals operate at 4MHz
	Stop 1	• Same as Stop 0 mode except main regulator is OFF and low-power regulator is ON			
Standby		• Achieves lowest power consumption with BOR • VCORE domain is powered off • SRAM and register contents are not retained, except for registers in RTC domain and standby circuits	STANDBY	STANDBY0	• PD1 power domain is switched off, PD1 peripherals are disabled and kept in retention • CPU, DMA, SRAM, FLASH, PLL, XTAL retained • VDDC voltage reduced to 10%, PD0 peripherals operate at 32KHz
				STANDBY1	• Same as STANDBY0 except PD0 peripherals are not actively clocked
Shutdown		• Internal regulator is switched off • PLL and oscillators are powered down • SRAM and register contents are not retained	SHUTDOWN		• Core regulator disabled • Core clocks are powered down • SRAM and register contents are not retained

3.6 Interrupt and Events Comparison

Interrupts and exceptions

The AM13E230x and STM32G474x MCUs both register and map interrupt and exception vectors depending on the device's available peripherals. A summary and comparison of the interrupt vectors for each family of devices is included in Table 3-10. A lower value of priority for an interrupt or exception is given higher precedence over interrupts with a higher priority value.

For some of these vectors, the priority is user-selectable. For others, the priority is fixed. In the AM13E230x and STM32G474x, exceptions such as NMI, reset, and hard fault handlers are given negative priority values to indicate that these always have the highest precedence over peripheral interrupts. For peripherals with selectable interrupt priorities, up to four programmable priority levels are available on both families of devices.

Table 3-10. Interrupt Comparison

NVIC Number	STM32G474x		AM13E230x	
	Interrupt/Exception	**Priority**	**Interrupt/Exception**	**Priority**
-	-	-	Reset	Fixed: -4
-14	-	-	NMI	Fixed: -2
-13	-	-	HardFault	Fixed: -1
-12	-	-	MemManage	Settable
-11	-	-	BusFault	Settable
-10	-	-	UsageFault	Settable
-5	-	-	SVCall	Settable
-4	-	-	DebugMonitor	Settable
-2	-	-	PendSV	Settable

Table 3-10. Interrupt Comparison (continued)

NVIC Number	STM32G474x		AM13E230x	
	Interrupt/Exception	Priority	Interrupt/Exception	Priority
-1	-	-	SysTick	Settable
-	Reset	Fixed: -3	-	-
-	NMI	Fixed: -2	-	-
-	HardFault	Fixed: -1	-	-
-	MemManage	Settable	-	-
-	BusFault	Settable	-	-
-	UsageFault	Settable	-	-
-	PendSV	Settable	-	-
-	SysTick	Settable	-	-
0	WWDG	Settable	PMCU	Settable
1	PVD_PVM	Settable	Debug	Settable
2	RTC/TAMP/CSS_LSE	Settable	Flash	Settable
3	RTC_WKUP	Settable	WWDT0	Settable
4	FLASH	Settable	GPIO0	Settable
5	RCC	Settable	GPIO1	Settable
6	EXTI0	Settable	GPIO2	Settable
7	EXTI1	Settable	GPIO3	Settable
8	EXTI2	Settable	ADC0_SEQ0	Settable
9	EXTI3	Settable	ADC0_SEQ1	Settable
10	EXTI4	Settable	ADC0_SEQ2	Settable
11	DMA1_CH1	Settable	ADC0_SEQ3	Settable
12	DMA1_CH2	Settable	ADC0_DCOMP	Settable
13	DMA1_CH3	Settable	ADC1_SEQ0	Settable
14	DMA1_CH4	Settable	ADC1_SEQ1	Settable
15	DMA1_CH5	Settable	ADC1_SEQ2	Settable
16	DMA1_CH6	Settable	ADC1_SEQ3	Settable
17	DMA1_CH7	Settable	ADC1_DCOMP	Settable
18	ADC1_2	Settable	ADC2_SEQ0	Settable
19	USB_HP	Settable	ADC2_SEQ1	Settable
20	USB_LP	Settable	ADC2_SEQ2	Settable
21	FDCAN1_IT0	Settable	ADC2_SEQ3	Settable
22	FDCAN1_IT1	Settable	ADC2_DCOMP	Settable
23	EXTI9_5	Settable	MCAN	Settable
24	TIM1_BRK/TIM15	Settable	PWM0_INT	Settable
25	TIM1_UP/TIM16	Settable	PWM1_INT	Settable
26	TIM1_TRG_COM/ TIM17/TIM1_DIR/ TIM1_IDX	Settable	PWM2_INT	Settable
27	TIM1_CC	Settable	PWM3_INT	Settable
28	TIM2	Settable	PWM4_INT	Settable
29	TIM3	Settable	ECAP0	Settable
30	TIM4	Settable	ECAP1	Settable
31	I2C1_EV	Settable	EQEP0	Settable
32	I2C1_ER	Settable	EQEP1	Settable
33	I2C2_EV	Settable	EQEP2	Settable
34	I2C2_ER	Settable	UC0	Settable

Table 3-10. Interrupt Comparison (continued)

NVIC Number	STM32G474x		AM13E230x	
	Interrupt/Exception	Priority	Interrupt/Exception	Priority
35	SPI1	Settable	UC1	Settable
36	SPI2	Settable	UC2	Settable
37	USART1	Settable	UC3	Settable
38	USART2	Settable	UC4	Settable
39	USART3	Settable	UC5	Settable
40	EXTI15_10	Settable	DMA	Settable
41	RTC_ALARM	Settable	TINIE_LITE	Settable
42	USBWakeUP	Settable	EPI	Settable
43	TIM8_BRK/TIM8_TERR /TIM8_IERR	Settable	AES.INT_EVENT0	Settable
44	TIM8_UP	Settable	TIMG4_0	Settable
45	TIM8_TRG_COM/TIM8 _DIR/TIM8_IDX	Settable	TIMG12_0	Settable
46	TIM8_CC	Settable	TMU_LUF_INT	Settable
47	ADC3	Settable	TMU_LVF_INT	Settable
48	FSMC	Settable	Reserved	Settable
49	LPTIM1	Settable	Reserved	Settable
50	TIM5	Settable	Reserved	Settable
51	SPI3	Settable	Reserved	Settable
52	UART4	Settable	Reserved	Settable
53	UART5	Settable	Reserved	Settable
54	TIM6_DACUNDER	Settable	Reserved	Settable
55	TIM7_DACUNDER	Settable	Reserved	Settable
56	DMA2_CH1	Settable	Reserved	Settable
57	DMA2_CH2	Settable	Reserved	Settable
58	DMA2_CH3	Settable	Reserved	Settable
59	DMA2_CH4	Settable	Reserved	Settable
60	DMA2_CH5	Settable	Reserved	Settable
61	ADC4	Settable	Reserved	Settable
62	ADC5	Settable	Reserved	Settable
63	UCPD1 global interrupt	Settable	Reserved	Settable
64	COMP1_2_3	Settable		
65	COMP4_5_6	Settable		
66	COMP7	Settable		
67	HRTIM_Master_IRQn	Settable		
68	HRTIM_TIMA_IRQn	Settable		
69	HRTIM_TIMB_IRQn	Settable		
70	HRTIM_TIMC_IRQn	Settable		
71	HRTIM_TIMD_IRQn	Settable		
72	HRTIM_TIME_IRQn	Settable		
73	HRTIM_TIM_FLT_IRQn	Settable		
74	HRTIM_TIMF_IRQn	Settable		
75	CRS	Settable		
76	SAI	Settable		

Table 3-10. Interrupt Comparison (continued)

NVIC Number	STM32G474x		AM13E230x	
	Interrupt/Exception	Priority	Interrupt/Exception	Priority
77	TIM20_BRK/ TIM20_TERR/ TIM20_IERR	Settable		
78	TIM20_UP	Settable		
79	TIM20_TRG_COM/ TIM20_DIR/TIM20_IDX	Settable		
80	TIM20_CC	Settable		
81	FPU	Settable		
82	I2C4_EV	Settable		
83	I2C4_ER	Settable		
84	SPI4	Settable		
85	AES	Settable		
86	FDCAN2_IT0	Settable		
87	FDCAN2_IT1	Settable		
88	FDCAN3_IT0	Settable		
89	FDCAN3_IT1	Settable		
90	RNG	Settable		
91	LPUART	Settable		
92	I2C3_EV	Settable		
93	I2C3_ER	Settable		
94	DMAMUX_OVR	Settable		
95	QUADSPI	Settable		
96	DMA1_CH8	Settable		
97	DMA2_CH6	Settable		
98	DMA2_CH7	Settable		
99	DMA2_CH8	Settable		
100	CORDIC	Settable		
101	FMAC	Settable		

3.7 Debug and Programming Comparison

Both AM13E230x and STM32G474x MCUs support standard debug interfaces supported by a variety of debugger hardware.

Table 3-11. Debug Feature Comparison

Debug Feature	STM32G474x	AM13E230x
Debug Port	• JTAG-DP (5-pin) • SW-DP (2-pin)	• JTAG-DP (4-pin) • SW-DP (2-pin)
Break Points	FPB (Flash Patch Breakpoint) unit: • Implements hardware breakpoints, patches code and data from code space to system space • 2x literal comparators for matching against literal loads from Code Space and remapping to a corresponding area in the System Space • 6x instruction comparators for matching against instruction fetches from Code Space	BPU (Breakpoint Unit): • 8x comparators used to generate a debug event when the address of an instruction fetch matches the address programmed into the respective BPU comparator

Table 3-11. Debug Feature Comparison (continued)

Debug Feature	STM32G474x	AM13E230x
Watchpoints	DWT (Data Watchpoint Trigger) • 4x comparators configurable as a hardware watchpoint, trigger to an ETM, PC sampler, or data address sampler	DWT (Data Watchpoint and Trace Unit) • 4x comparators that support generating an event upon a data address match (watchpoint event) or an instruction address match (PC watchpoint event)
Processor Trace	NO	MTB (Micro Trace Buffer) • Processor trace engine based on the ARM CoreSight MTB-M33 MTB
External Trace	NO	Embedded Trace Macrocell (ETM) • Streams a full-instruction program-counter trace with a 64-bit cycle-accurate timestamp counter
Low-Power Debug	YES • Supported in Sleep, Stop, and Standby modes	YES • Supported in all modes except SHUTDOWN
EnergyTrace	NO	YES
Peripheral Debug	YES	YES
Debug Access Disable	YES	YES

System Bootloader

Both AM13E230x and STM32G474x devices have reserved space in flash memory containing system information used to re-program the flash memory through a variety of standard interfaces. On AM13E230x devices, this is referred to as the Bootstrap Loader (BSL).

Table 3-12. System Bootloader Feature Comparison

BSL Features	STM32G474x	AM13E230x
BSL Started on Blank Device	YES	YES
Auto-detect Programming Interface	YES	YES
Security	• Memory security and access restriction options	• Access is always protected with a 256-bit password and features a configurable security alert handling for resisting brute force attacks • The BSL can return a 32-bit CRC of a code or data region (1KB minimum region size) to verify programming
Customizable	NO	YES
Invoke Methods	• HW: Set BOOT0 pin to HIGH, reset the device • SW: Execute a software jump to the bootloader address	• HW: Trigger using user-configured BSL INVOKE GPIO pin • SW: Execute a BSL entry (RESETLEVEL 0x02)
Interfaces Supported		
UART	YES	YES
I2C	YES	YES
SPI	YES	NO
CAN	YES	YES
USB	YES	NO

4 Digital Peripheral Comparison

4.1 General-Purpose I/O (GPIO)

The foundational, general-purpose I/O systems on STM32G474x and AM13E230x are compared in Table 4-1 below.

Table 4-1. GPIO Feature Comparison

Features	STM32G474x	AM13E230x
Output modes	• Push-pull • Open drain with pullup or pulldown (only applicable to a limited set of pins)	• Push-pull
Output Frequency	4 speed ranges per pin: • Low (2 MHz) • Medium (10MHz) • High (50 MHz) • Very High (up to 100 MHz depending on VDD/ load)	Speed range depends on IO type: • SDIO (Standard-Drive I/O) – 16MHz, 32MHz • HSIO (High-Speed I/O) – 16MHz, 24MHz, 32MHz, 40MHz
Drive Strength	Up to 20mA (sink/source capability per pin, depending on I/O type)	• Low drive: 2mA • High drive: 6mA
Input modes	• Floating • Pull-up • Push-down • Analog	• Floating • Pull-up • Push-down • Analog
Atomic bit set and reset	YES	YES
GPIO locking	YES	NO
Fast Toggle	• Every 2 CPU clock cycles	• Every CPU clock cycle
Wake-Up	GPIO pins can act as EXTI wakeup sources from Stop/ Standby modes	"FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port.
Controllable via DMA	NO	YES
User-Controllable Input Glitch Filtering	NO	YES
User-Controllable Input Hysteresis	NO	YES

Note

The GPIO module for the AM13E230x platform does not manage the complete digital IO functionality (for example, pullup, pulldown, or other functional muxing). For complete digital IO control details, refer to IOMUX. Similar to any other peripheral, the GPIO has inputs and outputs (with output enable) that allow the GPIO to interface with the IOMUX to make connections to the IO pins.

4.2 Serial Communications Peripherals

STM32G474x and AM13E230x MCUs both have standard serial communications peripherals - UART, I2C, and SPI. However, the hardware implementation and feature set differs in various ways.

On STM32G474x devices, UART, I2C, and SPI are independent, standalone peripheral blocks.

AM13E230x introduces a unified serial communication peripheral, referred to as UNICOMM. The UNICOMM module is a run-time configurable peripheral capable of supporting UART, I2C (Controller), I2C (Target) or SPI communications protocols. This gives users the flexibility to vary the number of instances per peripheral depending on the application requirements. For more information on UNICOMM, refer to the **UNICOMM**

chapters in the AM13E230x Technical Reference Manual. The below details the feature sets available for each UNICOMM instance on AM13E230x.

Table 4-2. Available UNICOMM Configurations Per AM13E230x Instance

SPG Instance	UNICOMM Instance	Supported Serial Protocols	Available Peripheral Types
SPG0	UC0	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC1	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC2	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target
SPG1	UC3	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC4	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC5	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target

4.2.1 Universal Asynchronous Receiver-Transmitter (UART)

Table 4-3. UART Feature Set Comparison

UART Feature	STM32G474x USART/UART	AM13E230x UNICOMM UART
DMA Access	Yes	Yes
TX/RX FIFO Depth	8 entries	16 entries
Hardware Flow Control (CTS/RTS)	Yes	Yes
Configurable Data Length	7, 8, or 9 bits	5, 6, 7 or 8 bits
Multi-processor Support	Yes	Yes
Synchronous Mode	Yes	No
Smartcard Mode (ISO7816)	Yes	Yes (Basic instances)
Single-wire Half Duplex Support	Yes	Yes
IrDA HW Support	Yes	No
LIN HW Support	Yes	Yes (Basic+ instances)
DALI HW Support	Yes	No
RS485 HW Support	Yes	Yes
Manchester Code HW Support	Yes	No
Low-Power Mode Wakeup	Yes	No
Autobaud Detection	Yes	No

4.2.2 Serial Peripheral Interface (SPI)

Table 4-4. SPI Feature Set Comparison

Feature	STM32G474x SPI	AM13E230x UNICOMM SPI
Controller or peripheral operation	Yes	Yes
DMA Access	Yes	Yes
TX/RX FIFO Depth	4 entries	16 entries
Supported SPI Formats	Motorola SPI, Texas Instruments, I2S	Motorola SPI or Texas Instruments
Data Bit Width (Controller mode)	4 to 16 bits	4 to 16 bits
Data Bit Width (Peripheral mode)	4 to 16 bits	7 to 16 bits
Maximum Speed	75 Mbits/s in controller and up to 41 Mbits/s in peripheral mode	50 Mbits/s
Multi-controller Support	Yes (Multi-controller via bus arbitration)	No
Full-duplex Transfers	Yes	Yes
Half-duplex Transfer (bidirectional data line)	Yes	No
Simplex Transfer (unidirectional data line)	Yes	No
Hardware Chip Select Management	Yes (NSS hardware mode support)	Yes
Programmable Clock Polarity and Phase	Yes (CPOL and CPHA)	Yes (CTL0.SPO and CTL0.SPH bit)

Table 4-4. SPI Feature Set Comparison (continued)

Feature	STM32G474x SPI	AM13E230x UNICOMM SPI
Programmable Data Order (MSB first or LSB first)	Yes	Yes
Hardware CRC	Yes (polynomial configurable)	No

4.2.3 Inter-Integrated Circuit (I2C)

Table 4-5. I2C Feature Set Comparison

Feature	STM32G474x I2C	AM13E230x UNICOMM I2CC/I2CT
Controller and Target Modes	Yes	Yes
DMA Access	Yes	Yes
TX/RX FIFO Depth	8 entries	16 entries
Multi-Controller Support	Yes	Yes
Standard-mode (up to100 kHz) Support	Yes	Yes
Fast-mode (up to 400kHz) Support	Yes	Yes
Fast-mode Plus (up to 1MHz) Support	Yes	Yes
Addressing Modes	7-bit and 10-bit	7-bit and 10-bit
Target Addresses	Dual addressing and 1 configurable mask	Dual addressing and 1 configurable mask (Advanced I2CT instances)
General Call Support	Yes	Yes
Programmable Setup and Hold Times	Yes	No
Clock Stretching	Yes	Yes
Software Reset	Yes	Yes
Programmable analog and digital noise filters	Yes (digital filter up to 15 I2C clock cycles, analog filter configurable)	Yes (Basic instances - digital filter, Advanced instances - analog filter)

4.3 Timers

Table 4-6. Timer Type Comparison

STM32G474x		AM13E230x	
Timer Name	**Abbreviated Name**	**Timer Name**	**Abbreviated Name**
Advanced control	TIM1, TIM8, TIM20	N/A	N/A
General-purpose	TIM2-5, TIM15-17	General-purpose	TIMG4 and TIMG12
High resolution	HRTIM	N/A	N/A
Basic	TIM6, TIM7	N/A	N/A
Low Power	LPTIM	N/A	N/A

Note

AM13E23x has only 2 timers (TIMG4, TIMG12)

Table 4-7. Timer Feature Comparison

Feature	STM32G474x Timers	AM13E230x Timers
Resolution	16-bit (most), 32-bit (TIM2, TIM5)	16-bit (TIMG4), 32-bit (TIMG12)
PWM	Yes (except basic timers)	Yes
Capture	Yes	Yes
Compare	Yes	Yes
One-shot	Yes (available in advanced and general-purpose timer)	Yes
Up down count functionality	Yes	Yes
Power Modes	Yes	Yes

Table 4-7. Timer Feature Comparison (continued)

Feature	STM32G474x Timers	AM13E230x Timers
QEI support	Yes (TIM1-5, TIM8)	Yes
Programmable pre-scalar	Yes (16-bit)	Yes (8-bit)
Shadow register mode	Yes	Yes
Events/Interrupt	Yes	Yes
Fault Event Mechanism	Yes (in advanced timer for motor control)	Yes (in advance timer)
Auto reload functionality	Yes	Yes

Table 4-8. Timer Module Replacement

STM32G474x Timer	AM13E230x equivalent	Reasoning
TIM1, TIM8, TIM20	Replaced by MCPWM and eQEP peripherals	Advanced control, 16-bit resolution, QEI support
TIM2/5	TIMG12	General-purpose, 32-bit resolution
TIM3, TIM4	TIMG4	General purpose, 16-bit resolution
TIM6/7	-	Basic Timer
TIM15/16/17	-	General purpose
LPTIM	Any timer in PD0	LPTIM sources LFCLK, PD0- low power mode in AM13E23x

Table 4-9. Timer Use-Case Comparisons

Feature	STM32G474x Timer	AM13E230x Timer Support
PWM	TIM1-4, TIM8, TIM15-17 support edge and center-aligned PWM. Basic Timers (TIM6/7, LPTIM) do not generate PWM.	TIMG4 and TIMG12
Capture	Supported on all general purpose and advanced timers	TIMG4 and TIMG12
Compare	Supported on all general purpose and advanced timers	TIMG4 only
One-shot	Supported on all timers including LPTIM	TIMG4 and TIMG12
Prescaler	16-bit prescaler (all TIMx), LPTIM has a 3bit prescalar	TIMG4 only
Synchronization	TIM1-4, TIM8, TIM15 can be master/slave in synchronization chains	TIMG4 and TIMG12

4.4 Windowed Watchdog Timer (WWDT)

Table 4-10. WWDT Type Comparison

Key	STM32G474x	AM13E230x
Name	1. Independent Watchdog Timer 2. Windowed Watchdog Timer	Windowed Watchdog Timer
Abbreviated name (same order)	1. IWDG 2. WWDG	WWDT

Table 4-11. Watchdog Timer Feature Comparison

Feature	STM32G474x	AM13E230x
Window mode	Yes	Yes
Interval timer mode	Yes	Yes
LFCLK source	No	Yes
Interrupts	Yes	Yes
Counter resolution	12 bit (IWDG), 7 bit (WWDG)	25 bit

Table 4-11. Watchdog Timer Feature Comparison (continued)

Feature	STM32G474x	AM13E230x
Clock divider	WWDG no, IWDG yes	Yes

4.5 Controller Area Network (CAN)

Table 4-12. CAN Comparison

Feature	STM32G474x FDCAN	AM13E230x MCAN
CAN FD Support	Yes (up to 64 data bytes)	Yes (up to 64 data bytes)
AUTOSAR and SAE J1939 support	Yes	Yes
ISO 11898-1: 2015 Compliant	Yes	Yes
Configurable transmit FIFO	Yes	Yes
Maskable interrupt	Yes	Yes
clock domains	Two (APB bus interface and CAN core kernel clock)	Two (CAN clock and host clock)
Loopback test mode	No	Yes
Power down Support	No	Yes

Note

The MCAN module on AM13E230x supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols.

5 Analog Peripherals Comparison

5.1 Analog to Digital Converter (ADC)

Table 5-1. ADC Feature Set Comparison

Features	STM32G474x	AM13E230
Resolution (bits)	12	12
Conversion Rate (Msps)	4	6.9
Oversampling (Bits)	16 bits	16 bits
Hardware Oversampling	256x	128x
FIFO	No (uses data register (ADC_DR) with DMA for continuous transfers)	Yes
ADC Reference (V)	Internal: VREFINT(~1.2V)	Selectable internal reference of 2.5V or 3.3V
	External: VRef +pin or VDDA	Ratiometric external reference set by VREFHI/VREFLO
Operating Power Modes	• Independent • Dual mode • Deep-Power-Down • Auto Off	• Burst Mode • Oversampling/Undersampling mode • External Reference Mode • Internal Reference Mode
Auto Power Down	Yes	No
External Input Channels	20	32
Internal Input Channels	VREFINT, temperature sensor, VBAT	VREF, Temperature Sensor, PGA Connectivity
DMA Support	Yes	Yes
ADC Window Comparator Unit	No	No
Simultaneous Sampling	Yes	Yes
Number of ADC	5	3

5.2 Comparator Subsystem (CMPSS)

Table 5-2. Comparator Feature Set Comparison

Feature	STM32G474X	AM13E230x
Available Comparators	Up to 7 (COMP1-COMP7)	Up to 4 (CMP0-CMP3)
Output Routing	• Internal to timers • EXTI line • External pin	• MCPWM XBAR • Output XBAR
Noninverting Input Sources	Multiplexed GPIO pins	CMPx HP / CMPx LP
Inverting Input Sources	• Multiplexed GPIO pins • DAC Channels 1/2 • Internal Vref (1.22V) • Buffered Vref divider – 1/4*Vref – 1/2*Vref – 3/4*Vref	• CMPx HN / CMPx LN • 12-bit DACH • 12-bit DACL
Register Lock	Comparator control and status registers can be write-protected (read only).	Yes, some COMP registers (writes require key)
Window Comparator Configuration	Yes	Yes
Input Short Mode	Yes	Yes
Operating Modes	High speed, Medium speed, Lower Power	N/A
Fast PWM Shutdowns	Yes	Yes
Output Filtering	Blanking Filter	Digital Filtering

Table 5-2. Comparator Feature Set Comparison (continued)

Feature	STM32G474X	AM13E230x
Output Polarity Control	Yes	Yes
Interrupts	Rising edge	No
	Falling edge	
	Both edge	
Exchange Inputs Mode	Yes	No

Table 5-3. Comparator Programmable Hysteresis Comparison

Hysteresis	MIN (mV)		TYP (mV)		MAX (mV)	
	STM32G474x	AM13E230x	STM32G474x	AM13E230x	STM32G474x	AM13E230x
0x	-	-6	0	0	-	6
1x	4	1	9	10	16	19
2x	7	7	18	20	32	34
3x	11	14	27	30	47	51
4x	15	19	36	41	63	70
5x	19	25	45	52	79	88
6x	23	31	54	64	95	109
7x	26	37	63	77	110	131

5.3 Digital to Analog Converter (DAC)

Note

On AM13E230x devices, there is not an independent, dedicated DAC module. Each 12-bit reference DACL output, part of the Comparator Subsystem (CMPSS LITE) can be configured to drive a reference voltage into the negative input of its respective comparator. The CMPSS2 and CMPSS3 instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not usable, including the high DAC, both comparators, and the digital filters.

Note

5.4 Programmable Gain Amplifier (PGA)

Table 5-4. PGA Feature Set

Feature	STM32G474x	AM13E230x
Input Type	Rail-to-rail	Rail-to-rail
Gain Bandwidth	7-13MHz	7-15MHz
Amplifier Configurations	• Follower configuration mode • Standalone mode (external gain setting mode) • PGA modes	• Buffer mode: PGA works in unity gain mode • Standalone mode: PGA operates as a conventional op-amp • Non-inverting mode: PGA works as a non-inverting op-amp • Subtractor mode: PGA output voltage equals to the subtraction of the two inputs
Input/Output Routing	• External pin routing • ADC input • COMP input	• External pin • ADC input • DAC input
Fault Detection	• External comparators • ADC monitoring	NO

Table 5-4. PGA Feature Set (continued)

Feature	STM32G474x	AM13E230x
Chopper Stabilization	Yes	Yes

6 System-Level Migration

The following section details the necessary migration steps for replacing the STM32G474x with an AM13E230x MCU in an existing PCB system.

Note

This section does not provide a comprehensive guide to all hardware design requirements when designing an AM13E230x PCB system - only those that must be considered when migrating from the STM32G474x platform to AM13E230x. Consult the *AM13E230x Hardware Design Guide* for more information.

6.1 Power, Clock, Reset Migration

The power, clock, and reset schemes required to power on and boot the microcontroller are largely the same between the two devices. This section outlines the requirements for each of these design aspects.

Power

STM32G474x and AM13E230x are both supplied by 3.3V. The power pin naming conventions are largely identical, with few differences. Table 6-1 details the migration requirements for power.

Table 6-1. Power Pin Requirements

STM32G474x Pin	AM13E230x Pin	Migration Requirement
VDD	VDD	• Ensure decoupling capacitor requirements are met
VBAT	VDD	• Note that there is no VBAT power domain on AM13E230x. This pin must be supplied by 3.3V and have the proper decoupling capacitance
VDDA	VDDA	• Ensure ferrite bead/decoupling capacitor requirements are met
VREF-	VREFLO	• Can be connected to GND in most cases
VREF_+	VREFHI	• Ensure decoupling capacitor requirements are met • Note differences in internal voltage reference levels between devices
VREF+	VREFHI	
VSS	VSS	• Digital GND, no additional requirement
VSSA	VSSA	• Analog GND, no additional requirement

Clock

STM32G474x and AM13E230x microcontrollers can be clocked by both internal or external oscillators. The external oscillator migration is detailed in Table 6-2.

Table 6-2. External Clock Requirements

STM32G474x Pin	AM13E230x Pin	Migration Requirement
PC14-OSC32_IN	PB14	• AM13E230x does not have input pins for a low-frequency crystal • Remove signal traces from a low-frequency crystal to these pins if necessary • PB14/PB15 can be used as GPIO
PC15-OSC32_OUT	PB15	

Table 6-2. External Clock Requirements (continued)

STM32G474x Pin	AM13E230x Pin	Migration Requirement
PF0-OSC_IN	PC16_X1	• A 10-25MHz crystal OR 4-48MHz external digital clock can be connected to these pins • If clocking the device using the internal oscillator, these pins can be use as GPIO
PF1_OSC_OUT	PC17_X2	

Reset/Boot

Table 6-3. Reset and Boot Pin Requirements

STM32G474x Pin	AM13E230x Pin	Migration Requirement
PG10-NRST	PD10-NRST	• Active low reset input to the device. No additional requirement • **Cannot** be used as GPIO on AM13E230x
PB8-BOOT0	PA24	• Boot mode/method is configured through software bootloader on AM13E230x • This pin does not need to be pulled high/low externally

6.2 Boot ROM Configured Pins

Several communication interface pins are configured by default in the AM13E230x Boot ROM for communicating with the Bootstrap Loader (BSL). While the pin assignments can be modified (with restrictions), it is important to note the default pins and what changes may be required for users migrating from STM32G474x to AM13E230x.

Table 6-4. Boot ROM Configured Interfaces

AM13E230x BSL Interface	STM32G474x Pin	AM13E230x Pin / Interface	Migration Requirements	Additional Configuration
UART	PA0	PA0 / UC4_RX_SCL_SCLK	• These pins must be available at an external header if intending to boot using UART	• Alternatively, the BSL can be modified to support any **UC4** instance configured for UART
	PA1	PA1 / UC4_TX_SDA_PICO		
I2C	PB7	PA23 / UC2_RX_SCL	• These pins must be available at an external header if intending to boot using I2C	• Alternatively, the BSL can be modified to support any **UC2** instance configured for I2C
	PB6	PA22 / UC2_TX_SDA		
MCAN	PA11	PA11 / MCAN0_RX	• These pins must be connected to a CAN transceiver/bus if intending to boot using MCAN	• Alternatively, the BSL can be modified to support any **MCAN0** instance
	PA12	PA12 / MCAN0_TX		

6.3 Additional Considerations

Unsupported Peripherals on AM13E230x

There are several peripherals that exist on STM32G474x, but are not implemented on AM13E230x. Consult the tables in Section 2.1.2 and Section 2.1.3 to check for compatibility at the peripheral and signal type level.

System Re-Design for AM13E230x

If there are enough interface migrations to warrant a PCB re-design, it is highly encouraged to utilize the SysConfig tool to verify all pin assignments and ensure that the drop-in AM13E230x is fully compatible with all existing and changed system requirements.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025