Application Note

TPLD Application in DC-DC Design

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ABSTRACT

TI programmable logic device (TPLD) family offers abundant logic resources, enabling flexible applications across consumer electronics, industrial systems, and data centers. This article proposes a method for utilizing TPLDs as PWM expanders in DC/DC power applications through graphical programming, thereby saving valuable DSP resources.

Table of Contents

1 Introduction....2
2 PCM Buck DC/DC Diagram....2
3 TPLD-Based DC/DC PWM Generation....3
3.1 TPLD-Based Topology PWM Generation....3
3.2 TPLD-Based PCM PWM Generation....5
3.3 TPLD-Based Multiphase Clock Generation....6
4 Summary....8
5 References....8

Trademarks

1 Introduction

The TPLD family integrates a rich set of peripheral resources, including general-purpose logic gates, RS flip-flops, comparators, and timers, making it widely applicable across diverse scenarios with stringent logic and timing requirements. In multiphase DC/DC applications, the number of PWM channels, logic levels, and phase-shifted clocks pose significant challenges to both DSP resource utilization and software development. This paper presents a solution that utilizes TPLD as a PWM expander, effectively addressing the challenges of limited DSP resources and complex software development in single phase/interleaved parallel DC/DC converters.

2 PCM Buck DC/DC Diagram

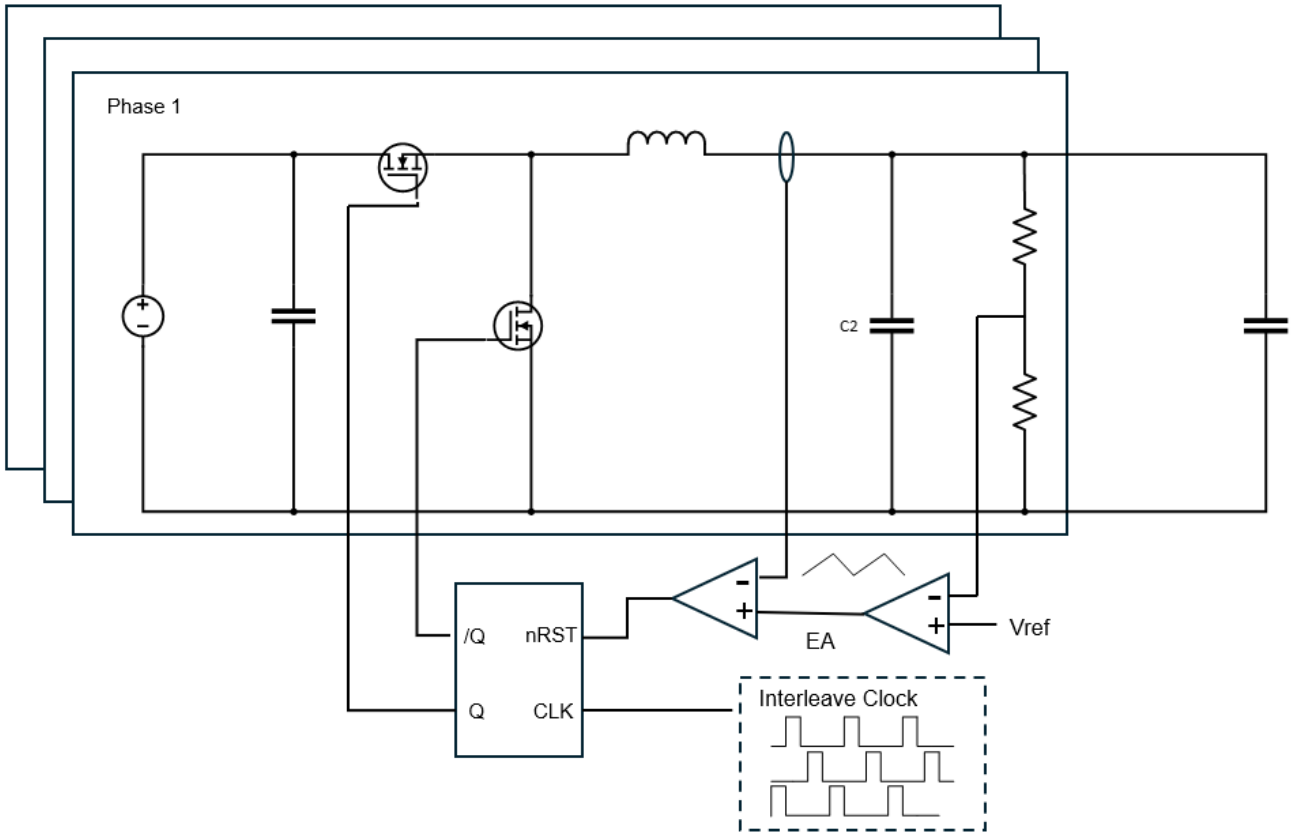

Figure 2-1. Peak Current Mode Buck Diagram

This paper discusses TPLD applications based on Buck converter topology. As shown in Figure 2-1, the architecture utilizes Peak Current Mode (PCM) control, which reduces the control-to-output small-signal transfer function to a first-order (single-pole) system. This significantly simplifies loop compensation network design and delivers fast load transient response. In multiphase power applications, interleaving technology is widely adopted; its primary advantage lies in shifting the phases of inductor currents across different phases to cancel output voltage ripples, thereby reducing the required output capacitance in high-current scenarios. Based on the level of DSP integration, this paper introduces three distinct implementation schemes: (1) The host DSP provides a single-phase base PWM signal, which TPLD then expands to support the target topologies, such as Buck, ACF, or PSFB; (2) The DSP provides the clock and error signals, while the TPLD handles the complete PWM signal generation; (3) TPLD independently manages both clock phase-shifting and PWM signal generation.

3 TPLD-Based DC/DC PWM Generation

3.1 TPLD-Based Topology PWM Generation

This section details the implementation scheme where the host DSP generates the initial PWM waveform, and TPLD handles the generation of the corresponding complementary PWM signals. As shown in Figure 2, the DSP or analog controller generates the initial closed-loop PWM signal. TPLD then processes the rising edge of this PWM signal using internal inverters and delay blocks to generate the complementary PWM waveforms with dead-time insertion.

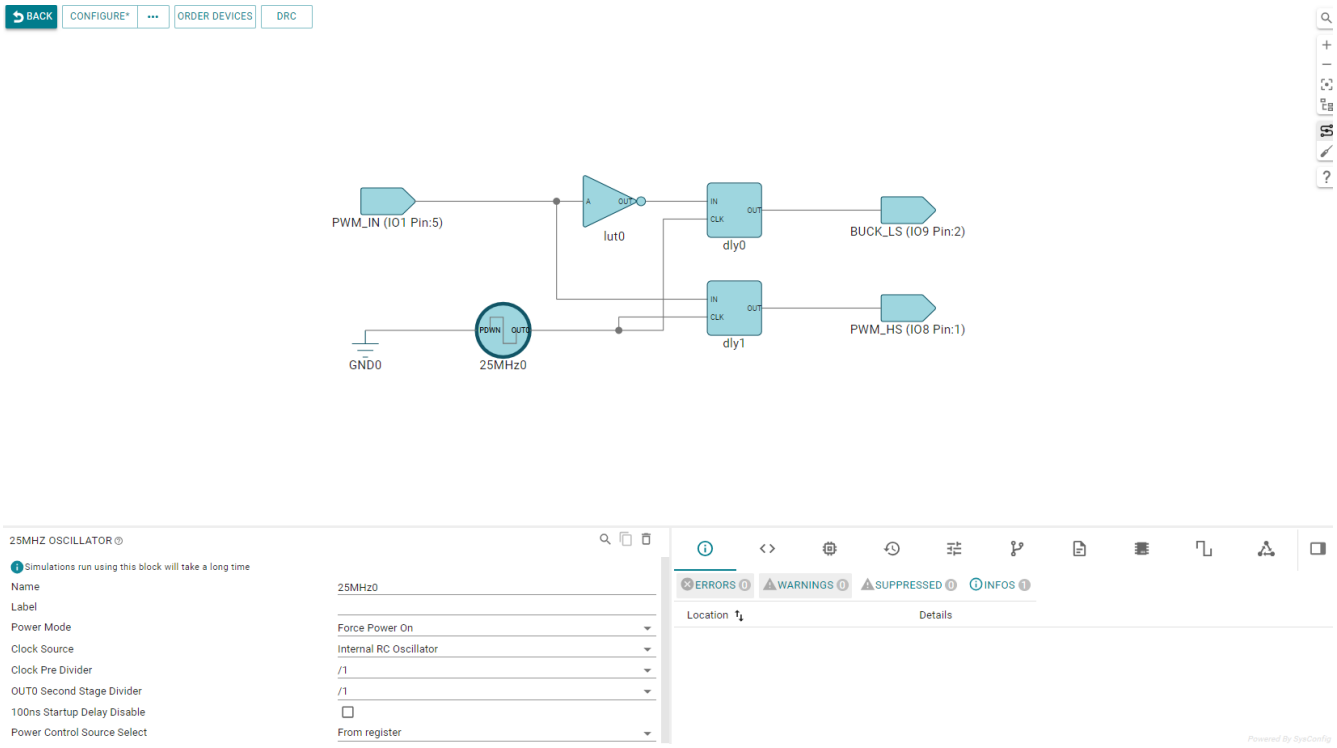

Figure 3-1. Synchronous Buck PWM Logic Diagram

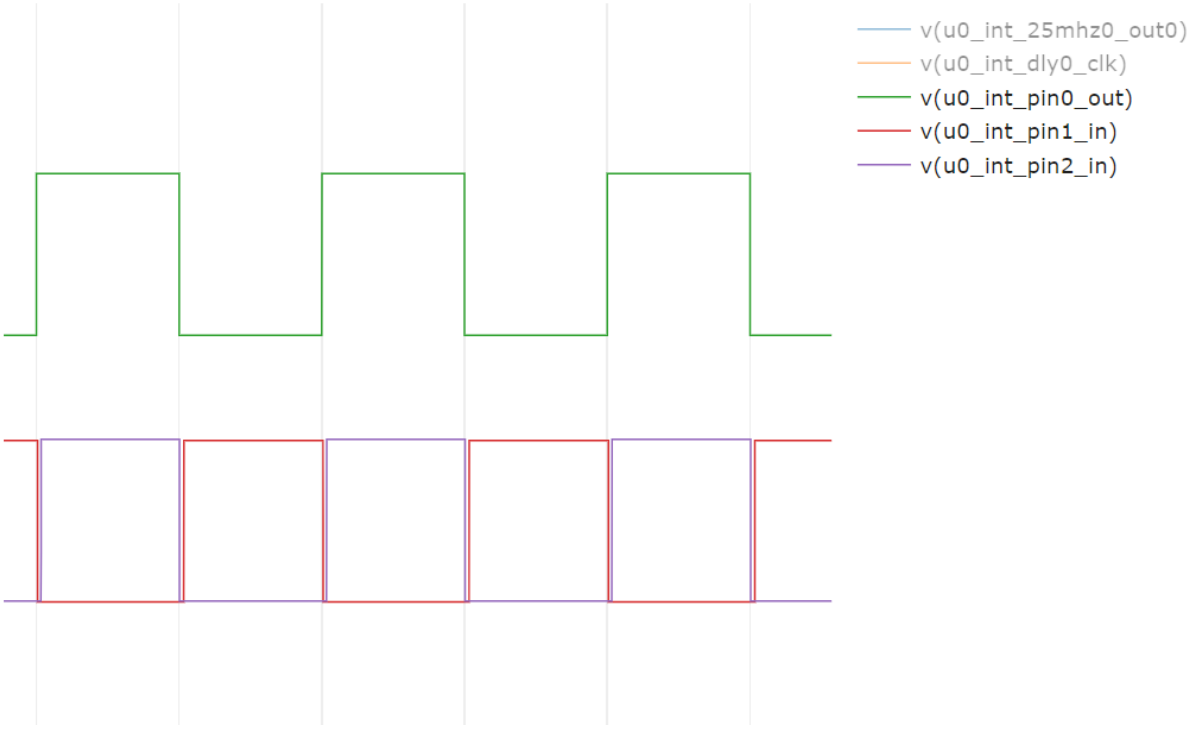

Figure 3-2. Synchronous Buck Simulation Waveforms

In practical applications, the GPIOs can be configured to operate in digital input mode with a Schmitt trigger to enhance the noise immunity of TPLD. For dead-time control, the configuration can also be offloaded to external RC circuits on the output GPIOs or implemented via the inherent dead-time design of the gate drivers, thereby simplifying TPLD internal logic design. The primary advantage of this scheme is its simple implementation; however, the disadvantage is that it only saves a single PWM channel in a standard Buck converter. In contrast, for more complex topologies, such as Synchronous Rectification Active Clamp Forward (SR-ACF) requiring 4 PWMs, or Phase-Shifted Full-Bridge (PSFB) requiring eight PWMs, this approach can offload a significantly higher number of host controller GPIO and PWM resources.

3.2 TPLD-Based PCM PWM Generation

This section introduces the implementation of Peak Current Mode (PCM) PWM signal generation in a Buck converter using TPLD. As shown in Figure 5, the host controller or an external operational amplifier provides the compensated error signal. TPLD utilizes its internal comparator to compare this error signal with the triangular inductor current waveform, generating an initial comparator output. This output is then processed by an RS flip-flop synchronized with the clock signal to establish the initial PWM waveform. Finally, the internal logic circuitry generates complementary PWM outputs.

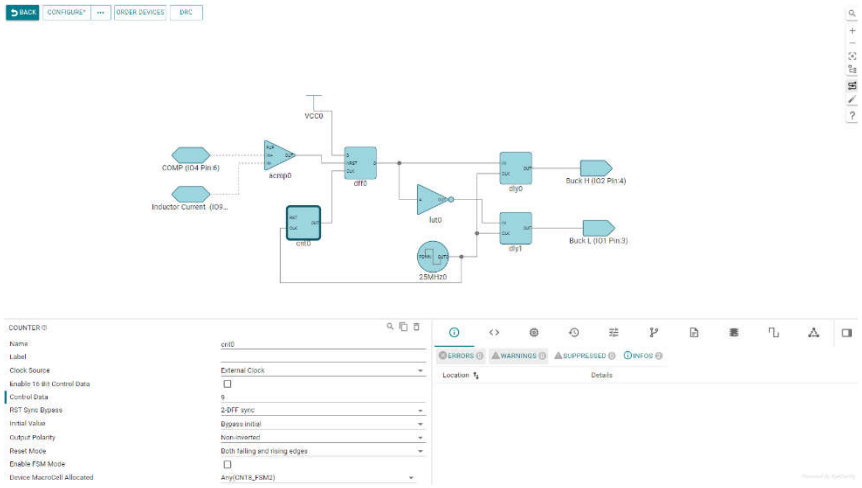

Figure 3-3. PCM Buck PWM Logic Diagram

Figure 3-3 illustrates a simplified control block diagram. In practical designs, the overall performance and reliability of this implementation can be enhanced through the following methods:

1. When the duty cycle exceeds 50%, slope compensation must be introduced to the current sensing signal derived from the clock to prevent subharmonic oscillation
2. Internal comparators or additional logic circuitry can be utilized to construct maximum duty cycle limiting and cycle-by-cycle overcurrent protection circuits
3. For high-frequency applications, an external high-speed comparator can be employed to achieve faster transient response.

3.3 TPLD-Based Multiphase Clock Generation

Clock and PWM generation for a buck converter can be implemented by TPLD. As shown in Figure 3-4, the internal 2MHz oscillator is used as the source clock. A 50% duty-cycle Phase-1 clock is generated through the counter block and D flip-flops. Four interleaved phase clocks are then derived from the Phase-1 clock by using delay blocks, enabling interleaved multiphase operation.

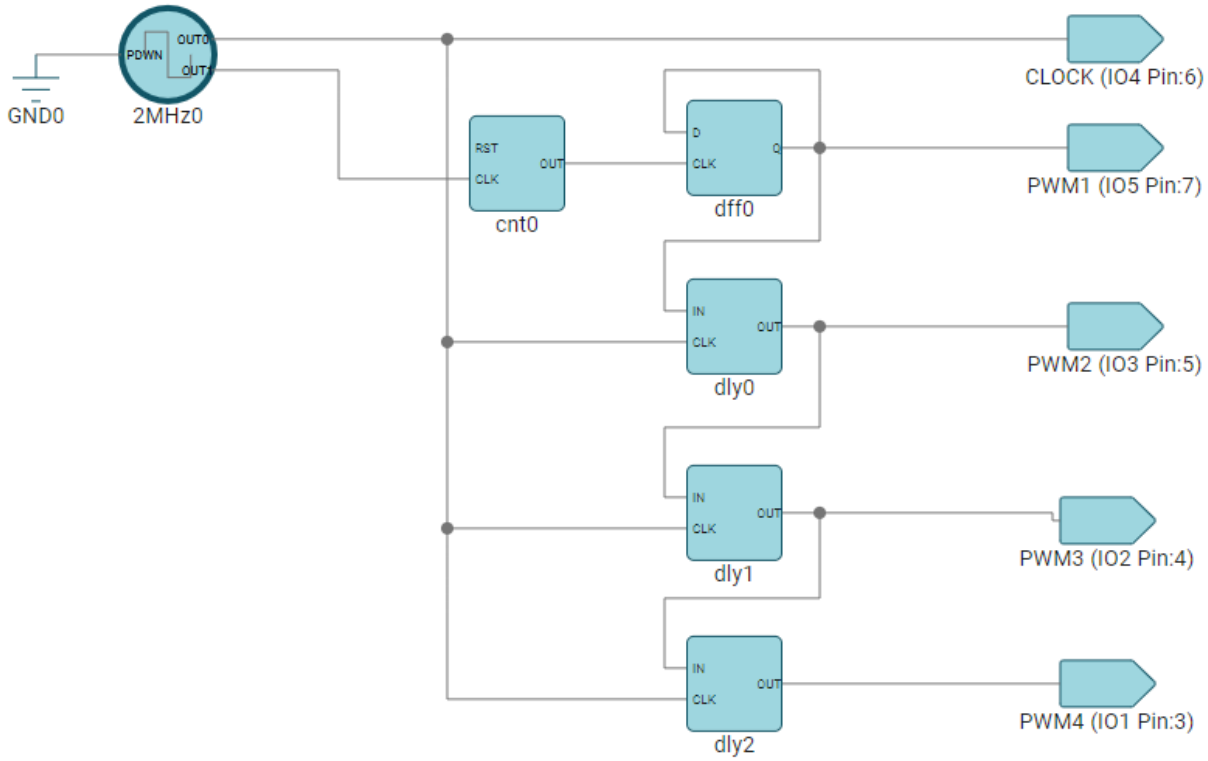

Figure 3-4. Interleaved Phase-Clock Logic Diagram

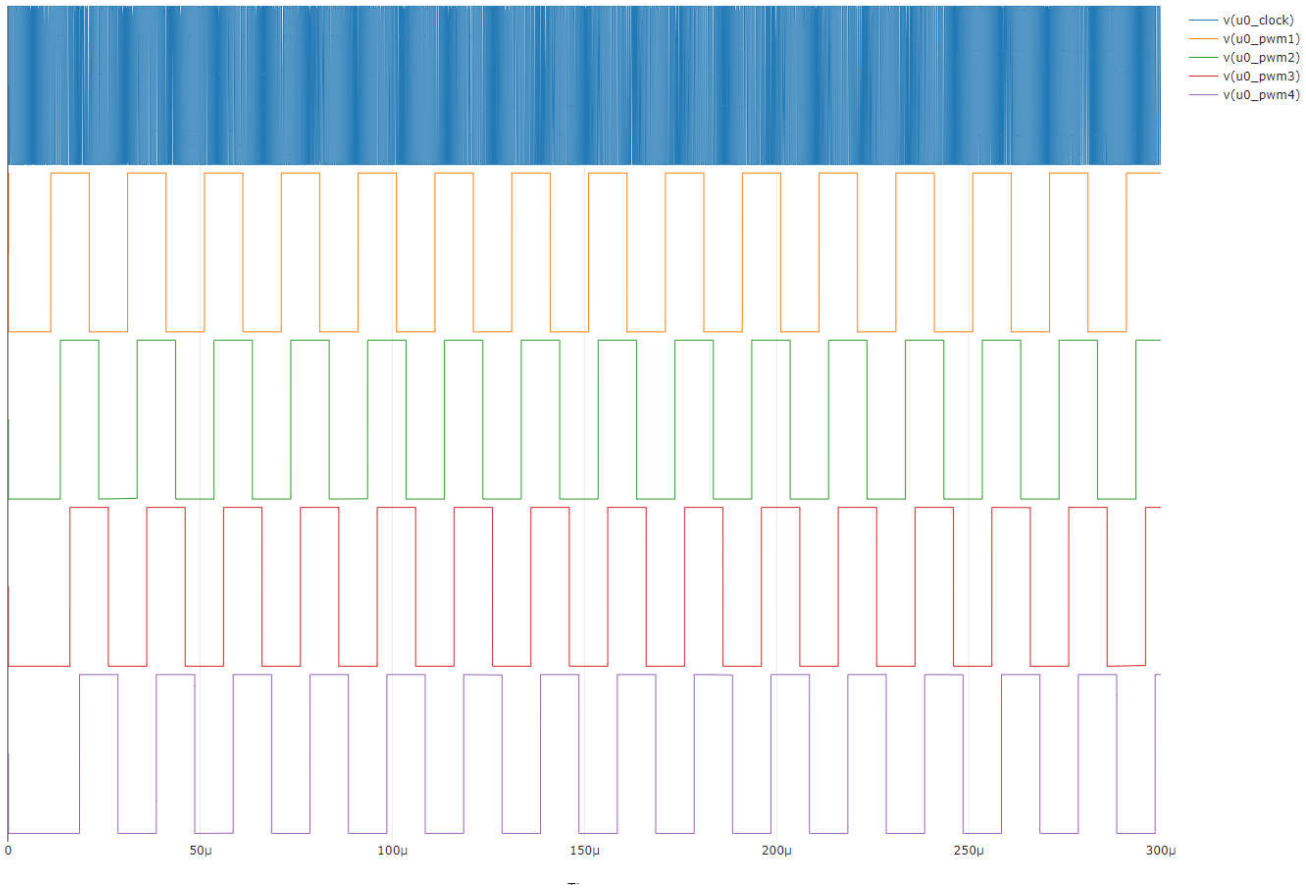

Figure 3-5. Interleaved Phase-Clock Simulation Waveforms

Based on this config, TPLD can interface with the two mentioned PWM generation schemes to implement interleaved parallel DC/DC designs. In this implementation, TPLD can process nearly all functional tasks within the DC/DC converter circuitry except for loop compensation. This approach further reduces host controller resource requirements in multiphase power supply applications.

4 Summary

This paper utilizes TI's TPLD series as a graphical-programmed PWM expander in single /interleaved DC/DC converters. By processing the design of clock phase-shifting and complementary PWM generation, TPLD significantly offloads clock and PWM logic control resources from the host controller. This approach effectively conserves DSP resources, lowers software complexity, and facilitates hardware engineers in rapid development.

Learn more about TPLD with the *Engineer's guide to programmable logic*.

5 References

1. Texas Instruments, *TPLD1202 Programmable Logic Device With I2 C/SPI and 10-GPIO* , datasheet.
2. Texas Instruments, *High-Speed Operation in TPLD*, application brief.
3. Texas Instruments, *Power Sequencing With Feedback Using TI Programmable Logic Devices*, application brief.
4. Texas Instruments, *使用 TI 可编程逻辑器件 (TPLD) 中的时序分量*, application note.
5. Texas Instruments, *Parallel Operation of the Buck-Boost Converters Using LM5177 Buck-Boost Controller*, application note.

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