Functional Safety Information

DRV8705-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for DRV8705-Q1 (VQFN 32 pin package package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for the SPI variant as a reference.

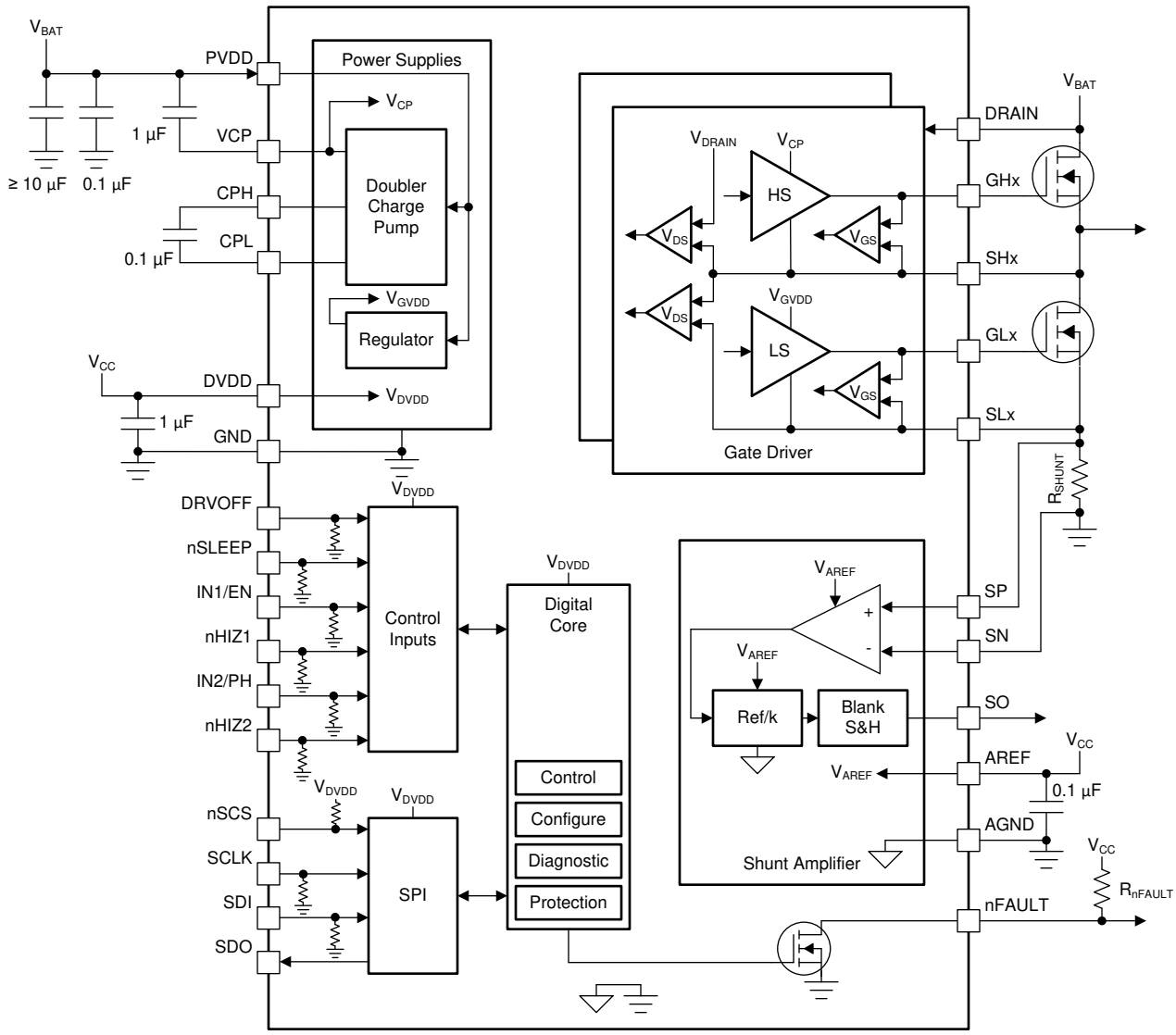

Figure 1-1. DRV8705S-Q1 Functional Block Diagram

Figure 1-2 shows the device functional block diagram for the HW variant as a reference.

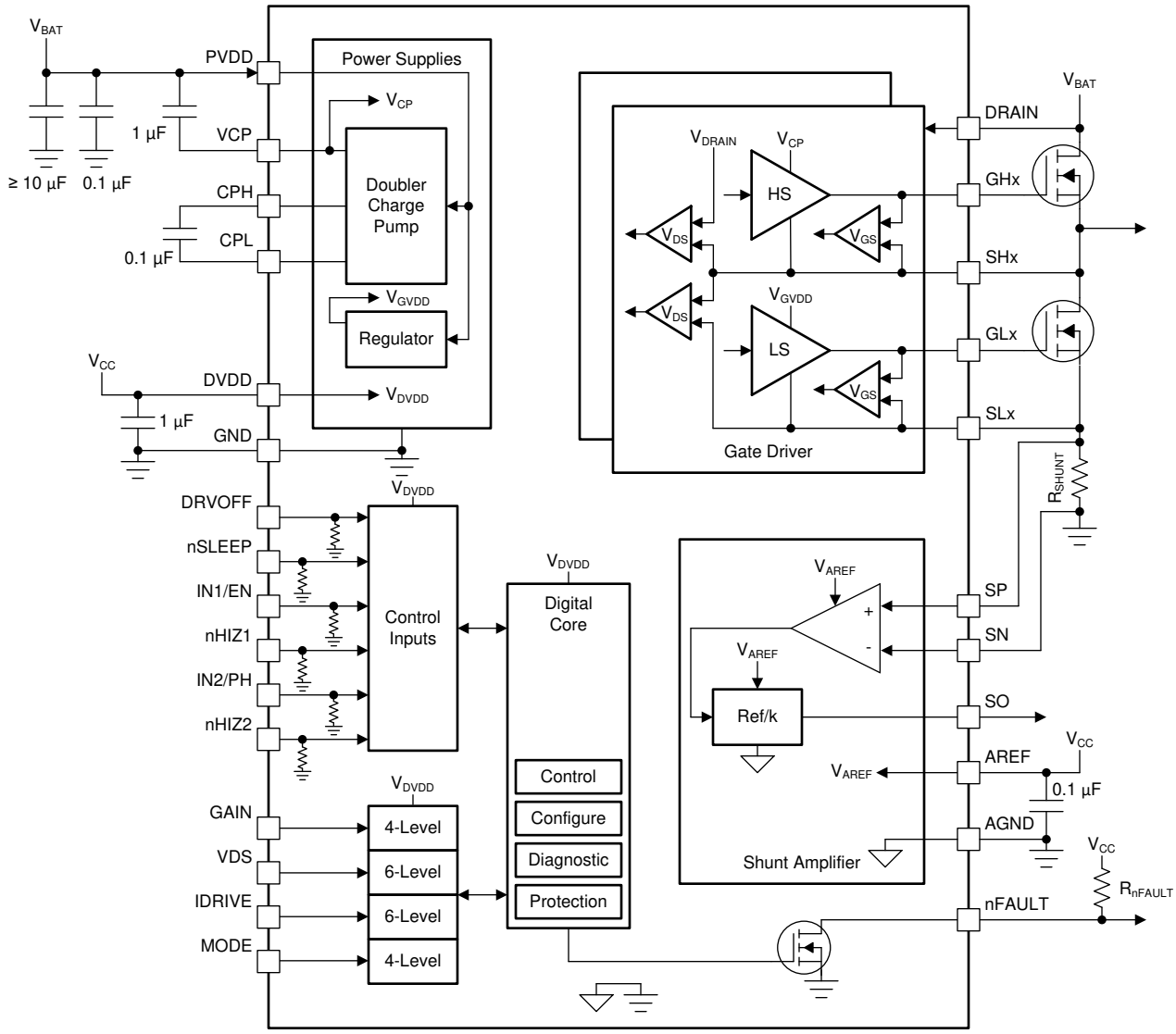

Figure 1-2. DRV8705H-Q1 Functional Block Diagram

DRV8705-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8705-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	20
Die FIT Rate	3
Package FIT Rate	17

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8705-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Low side gate turned ON, when commanded OFF	12.0%
Low side gate turned OFF, when commanded ON	12.5%
Low side gate to source voltage too high or too low	4.0%
Low side gate driver slew rate too fast or too slow	3.0%
High side gate turned ON, when commanded OFF	13.5%
High side gate turned OFF, when commanded ON	16.0%
High side gate to source voltage too high or too low	4.0%
High side gate driver slew rate too fast or too slow	3.0%
Dead time between high side FET and low side FET transition incorrect	5.5%
Current sense feedback and regulation incorrect	10.0%
Drain Source voltage monitoring incorrect	6.5%
Incorrect communication or fault indication	10.0%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8705-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 for SPI variant, see Table 4-3 for HW variant)
- Pin open-circuited (see Table 4-4 for SPI variant, see Table 4-5 for HW variant)
- Pin short-circuited to an adjacent pin (see Table 4-6 for SPI variant, see Table 4-7 for HW variant)
- Pin short-circuited to supply (PVDD) (see Table 4-8 for SPI variant, see Table 4-9 for HW variant)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 and Figure 4-2 show the DRV8705-Q1 pin diagrams. The DRV8705-Q1 has two pin diagram variants, an SPI variant (DRV8705S-Q1) and a HW variant (DRV8705H-Q1). For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8705-Q1 data sheet.

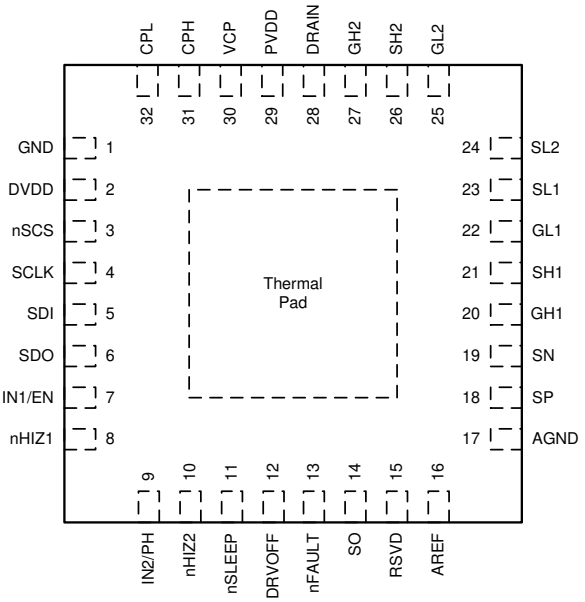

Figure 4-1. DRV8705S-Q1 Pin Diagram

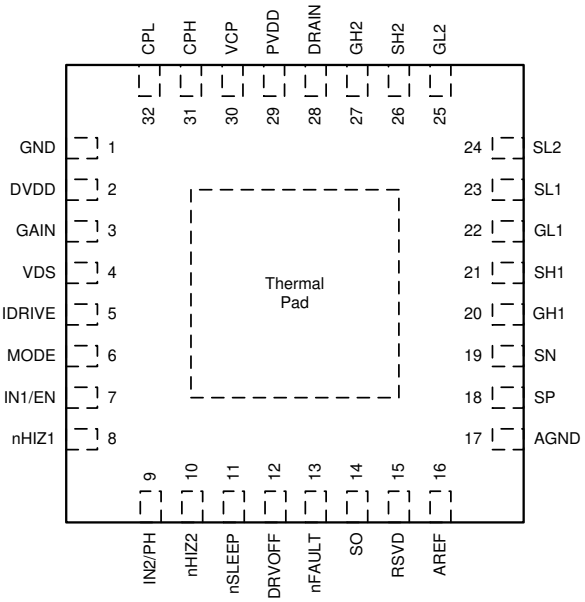

Figure 4-2. DRV8705H-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table and primary application section of the datasheet.

Table 4-2. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No impact. Intended operation.	D
DVDD	2	Device external digital power supply stuck low. Device non-operational.	B

Table 4-2. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
nSCS	3	SPI communication compromised.	B
SCLK	4	SPI communication compromised.	B
SDI	5	SPI communication compromised.	B
SDO	6	SPI communication compromised.	B
IN1/EN	7	Gate driver control input stuck low. Driver output may not match input.	B
nHIZ1	8	Gate driver control input stuck low. Driver output disabled.	B
IN2/PH	9	Gate driver control input stuck low. Driver output may not match input.	B
nHIZ2	10	Gate driver control input stuck low. Driver output disabled.	B
nSLEEP	11	Device stuck in sleep state. Outputs non-operational.	B
DRVOFF	12	Driver disable input stuck low. Gate driver disable function non-operational.	B
nFAULT	13	Device fault output indicator always active.	B
SO	14	Device current sense feedback invalid.	B
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply stuck low. Current sense invalid.	B
AGND	17	No impact. Intended operation.	D
SP	18	Device current sense feedback invalid.	B
SN	19	Device current sense feedback invalid.	B
GH1	20	HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SH1	21	HS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SL1	23	No impact. Intended operation.	D
SL2	24	No impact. Intended operation.	D
GL2	25	LS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SH2	26	HS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	Device overcurrent monitors and open load diagnostic non-operational.	B
PVDD	29	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	A
CPH	31	Device charge pump non-operational. Device CPUV fault.	A
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

Table 4-3. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No impact. Intended operation.	D
DVDD	2	Device external digital power supply stuck low. Device non-operational.	B
GAIN	3	Device GAIN setting potentially incorrect.	B
VDS	4	Device VDS setting potentially incorrect.	B
IDRIVE	5	Device IDRIVE setting potentially incorrect.	B
MODE	6	Device MODE setting potentially incorrect.	B
IN1/EN	7	Gate driver control input stuck low. Driver output may not match input.	B
nHIZ1	8	Gate driver control input stuck low. Driver output disabled.	B
IN2/PH	9	Gate driver control input stuck low. Driver output may not match input.	B
nHIZ2	10	Gate driver control input stuck low. Driver output disabled.	B
nSLEEP	11	Device stuck in sleep state. Outputs non-operational.	B
DRVOFF	12	Driver disable input stuck low. Gate driver disable function non-operational.	B

Table 4-3. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
nFAULT	13	Device fault output indicator always active.	B
SO	14	Device current sense feedback invalid.	B
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply stuck low. Current sense invalid.	B
AGND	17	No impact. Intended operation.	D
SP	18	Device current sense feedback invalid.	B
SN	19	Device current sense feedback invalid.	B
GH1	20	HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SH1	21	HS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SL1	23	No impact. Intended operation.	D
SL2	24	No impact. Intended operation.	D
GL2	25	LS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SH2	26	HS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	Device overcurrent monitors and open load diagnostic non-operational.	B
PVDD	29	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	A
CPH	31	Device charge pump non-operational. Device CPUV fault.	A
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

Table 4-4. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device behavior undefined, may retain operation due to alternative AGND pin path.	C
DVDD	2	Device external digital power supply missing. Device non-operational.	B
nSCS	3	SPI communication compromised.	B
SCLK	4	SPI communication compromised.	B
SDI	5	SPI communication compromised.	B
SDO	6	SPI communication compromised.	B
IN1/EN	7	Gate driver control input pulled low. Driver output may not match input.	B
nHIZ1	8	Gate driver control input pulled low. Driver output disabled.	B
IN2/PH	9	Gate driver control input pulled low. Driver output may not match input.	B
nHIZ2	10	Gate driver control input pulled low. Driver output disabled.	B
nSLEEP	11	Device stuck in sleep state. Outputs non-operational.	B
DRVOFF	12	Driver disable input pulled low. Gate driver disable function non-operational.	B
nFAULT	13	Device fault output indicator invalid.	B
SO	14	Device current sense feedback invalid.	B
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply missing. Current sense invalid.	B
AGND	17	Device behavior undefined, may retain operation due to alternative GND pin path.	C
SP	18	Device current sense feedback invalid.	B
SN	19	Device current sense feedback invalid.	B
GH1	20	HS1 external MOSFET non-operational.	B
SH1	21	HS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET non-operational.	B

Table 4-4. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SL1	23	LS1 VDS monitor non-operational.	B
SL2	24	LS2 VDS monitor non-operational.	B
GL2	25	LS2 external MOSFET non-operational.	B
SH2	26	HS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET non-operational.	B
DRAIN	28	HS1 and HS2 VDS monitors and open load diagnostics non-operational.	B
PVDD	29	Device external power supply missing. Device gate drivers and shunt amplifier non-operational.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	B
CPL	32	Device charge pump non-operational. Device CPUV fault.	B

Table 4-5. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device behavior undefined, may retain operation due to alternative AGND pin path.	C
DVDD	2	Device external digital power supply missing. Device non-operational.	B
GAIN	3	Device GAIN setting fixed to level 3.	B
VDS	4	Device VDS setting fixed to level 4.	B
IDRIVE	5	Device IDRIVE setting fixed to level 4.	B
MODE	6	Device MODE setting fixed to level 3.	B
IN1/EN	7	Gate driver control input pulled low. Driver output may not match input.	B
nHIZ1	8	Gate driver control input pulled low. Driver output disabled.	B
IN2/PH	9	Gate driver control input pulled low. Driver output may not match input.	B
nHIZ2	10	Gate driver control input pulled low. Driver output disabled.	B
nSLEEP	11	Device stuck in sleep state. Outputs non-operational.	B
DRVOFF	12	Driver disable input pulled low. Gate driver disable function non-operational.	B
nFAULT	13	Device fault output indicator invalid.	B
SO	14	Device current sense feedback invalid.	B
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply missing. Current sense invalid.	B
AGND	17	Device behavior undefined, may retain operation due to alternative GND pin path.	C
SP	18	Device current sense feedback invalid.	B
SN	19	Device current sense feedback invalid.	B
GH1	20	HS1 external MOSFET non-operational.	B
SH1	21	HS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET non-operational.	B
SL1	23	LS1 VDS monitor non-operational.	B
SL2	24	LS2 VDS monitor non-operational.	B
GL2	25	LS2 external MOSFET non-operational.	B
SH2	26	HS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET non-operational.	B
DRAIN	28	HS1 and HS2 VDS monitors and open load diagnostics non-operational.	B
PVDD	29	Device external power supply missing. Device gate drivers and shunt amplifier non-operational.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	B

Table 4-5. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CPL	32	Device charge pump non-operational. Device CPUV fault.	B

Table 4-6. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device external digital power supply stuck low. Device non-operational.	B
DVDD	2	SPI communication compromised.	B
nSCS	3	SPI communication compromised.	B
SCLK	4	SPI communication compromised.	B
SDI	5	SPI communication compromised.	B
SDO	6	SPI communication compromised. Gate driver control input mismatch.	B
IN1/EN	7	Gate driver control input mismatch.	B
nHIZ1	8	Gate driver control input mismatch.	B
IN2/PH	9	Gate driver control input mismatch.	B
nHIZ2	10	Gate driver control input mismatch. Device may enter sleep state.	B
nSLEEP	11	Device may enter sleep state or disable gate drivers.	B
DRVOFF	12	Device may disable gate driver or fault output indicator invalid.	B
nFAULT	13	Device fault indicator or current sense invalid.	B
SO	14	No impact. Intended operation.	D
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply stuck low. Current sense invalid.	B
AGND	17	Current sense invalid.	B
SP	18	Current sense invalid.	B
SN	19	Current sense invalid and HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault	B
GH1	20	HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault	B
SH1	21	GL1 output invalid, may violate GL1 voltage rating.	A
GL1	22	LS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SL1	23	Low-side VDS monitor sense accuracy impacted.	C
SL2	24	LS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
GL2	25	GL2 output invalid, may violate GL1 voltage rating.	A
SH2	26	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
GH2	27	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	High-side VDS monitor sense accuracy impact.	C
PVDD	29	Device charge pump non-operational. Device CPUV fault.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	A
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

Table 4-7. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device external digital power supply stuck low. Device non-operational.	B
DVDD	2	Device GAIN setting potentially incorrect.	B
GAIN	3	Device GAIN and VDS setting potentially incorrect.	B
VDS	4	Device VDS and IDRIVE setting potentially incorrect.	B

Table 4-7. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IDRIVE	5	Device IDRIVE and MODE setting potentially incorrect.	B
MODE	6	Device MODE setting potentially incorrect and gate driver control input mismatch.	B
IN1/EN	7	Gate driver control input mismatch.	B
nHIZ1	8	Gate driver control input mismatch.	B
IN2/PH	9	Gate driver control input mismatch.	B
nHIZ2	10	Gate driver control input mismatch. Device may enter sleep state.	B
nSLEEP	11	Device may enter sleep state or disable gate drivers.	B
DRVOFF	12	Device may disable gate driver or fault output indicator invalid.	B
nFAULT	13	Device fault indicator or current sense invalid.	B
SO	14	No impact. Intended operation.	D
RSVD	15	No impact. Intended operation.	D
AREF	16	Device external analog power supply stuck low. Current sense invalid.	B
AGND	17	Current sense invalid.	B
SP	18	Current sense invalid.	B
SN	19	Current sense invalid and HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault	B
GH1	20	HS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault	B
SH1	21	GL1 output invalid, may violate GL1 voltage rating.	A
GL1	22	LS1 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
SL1	23	Low-side VDS monitor sense accuracy impacted.	C
SL2	24	LS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
GL2	25	GL2 output invalid, may violate GL1 voltage rating.	A
SH2	26	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
GH2	27	HS2 external MOSFET off, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	High-side VDS monitor sense accuracy impact.	C
PVDD	29	Device charge pump non-operational. Device CPUV fault.	B
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	A
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

Table 4-8. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Short-Circuited to Supply (PVDD)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
DVDD	2	Low voltage pin max voltage violated.	A
nSCS	3	Low voltage pin max voltage violated.	A
SCLK	4	Low voltage pin max voltage violated.	A
SDI	5	Low voltage pin max voltage violated.	A
SDO	6	Low voltage pin max voltage violated.	A
IN1/EN	7	Low voltage pin max voltage violated.	A
nHIZ1	8	Low voltage pin max voltage violated.	A
IN2/PH	9	Low voltage pin max voltage violated.	A
nHIZ2	10	Low voltage pin max voltage violated.	A
nSLEEP	11	Low voltage pin max voltage violated.	A
DRVOFF	12	Low voltage pin max voltage violated.	A

Table 4-8. DRV8705S-Q1 (SPI Variant) Pin FMA for Device Pins Short-Circuited to Supply (PVDD) (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
nFAULT	13	Low voltage pin max voltage violated.	A
SO	14	Low voltage pin max voltage violated.	A
RSVD	15	No impact. Intended operation.	D
AREF	16	Low voltage pin max voltage violated.	A
AGND	17	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
SP	18	Current sense invalid.	B
SN	19	Current sense invalid.	B
GH1	20	HS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault.	B
SH1	21	LS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault. May violate GL1 voltage rating.	A
SL1	23	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
SL2	24	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
GL2	25	LS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault. May violate GL1 voltage rating.	A
SH2	26	LS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	High-side VDS monitor sense accuracy impact.	B
PVDD	29	No impact. Intended operation.	D
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	B
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

Table 4-9. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Supply (PVDD)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
DVDD	2	Low voltage pin max voltage violated.	A
GAIN	3	Low voltage pin max voltage violated.	A
VDS	4	Low voltage pin max voltage violated.	A
IDRIVE	5	Low voltage pin max voltage violated.	A
MODE	6	Low voltage pin max voltage violated.	A
IN1/EN	7	Low voltage pin max voltage violated.	A
nHIZ1	8	Low voltage pin max voltage violated.	A
IN2/PH	9	Low voltage pin max voltage violated.	A
nHIZ2	10	Low voltage pin max voltage violated.	A
nSLEEP	11	Low voltage pin max voltage violated.	A
DRVOFF	12	Low voltage pin max voltage violated.	A
nFAULT	13	Low voltage pin max voltage violated.	A
SO	14	Low voltage pin max voltage violated.	A
RSVD	15	No impact. Intended operation.	D
AREF	16	Low voltage pin max voltage violated.	A
AGND	17	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
SP	18	Current sense invalid.	B
SN	19	Current sense invalid.	B

Table 4-9. DRV8705H-Q1 (HW Variant) Pin FMA for Device Pins Short-Circuited to Supply (PVDD) (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GH1	20	HS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault.	B
SH1	21	LS1 external MOSFET non-operational. Device VDS fault.	B
GL1	22	LS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault. May violate GL1 voltage rating.	A
SL1	23	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
SL2	24	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
GL2	25	LS1 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault. May violate GL1 voltage rating.	A
SH2	26	LS2 external MOSFET non-operational. Device VDS fault.	B
GH2	27	HS2 external MOSFET gate stuck high, energy limited by TDRIVE. Device VGS fault.	B
DRAIN	28	High-side VDS monitor sense accuracy impact.	B
PVDD	29	No impact. Intended operation.	D
VCP	30	Device charge pump non-operational. Device CPUV fault.	B
CPH	31	Device charge pump non-operational. Device CPUV fault.	B
CPL	32	Device charge pump non-operational. Device CPUV fault.	A

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