Functional Safety Information

LDC3114-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LDC3114-Q1 (TSSOP-16 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

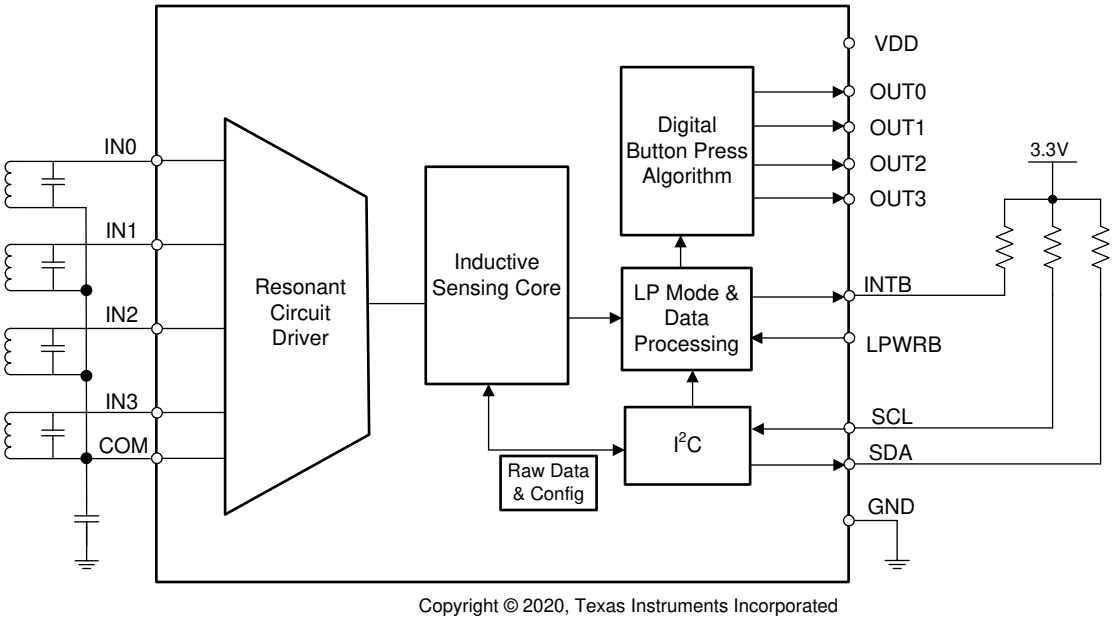

Figure 1-1. Functional Block Diagram

LDC3114-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LDC3114-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	2
Package FIT Rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 5.4 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LDC3114-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Sensor oscillator fails to start	15%
Sensor oscillation is distorted	10%
I^2C communication errors	25%
Digital output (OUTx) errors	25%
Low power / normal mode not functioning	25%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LDC3114-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LDC3114-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LDC3114-Q1 data sheet.

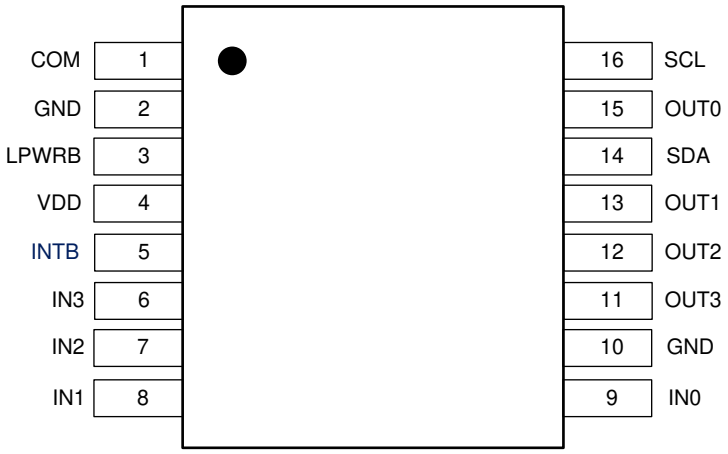

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is powered within published absolute maximum operating conditions.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COM	1	COM is grounded without a bypass capacitor. Will cause an error in sensor input and unpredictable LC sensor behavior	B
GND	2	Normal operation	D
LPWRB	3	Device stuck in Low Power Mode	B
VDD	4	Power supply shorted to ground	B
INTB	5	INTB is stuck low	B
IN3	6	No LC sensor input	B
IN2	7	No LC sensor input	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN1	8	No LC sensor input	B
IN0	9	No LC sensor input	B
GND	10	Normal operation	D
OUT3	11	May result in output status error	B
OUT2	12	May result in output status error	B
OUT1	13	May result in output status error	B
SDA	14	SDA will be stuck low. I^2C read/write will be non-functional	B
OUT0	15	May result in output status error	B
SCL	16	SCL will be stuck low. I^2C read/write will be non-functional	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COM	1	No common return path for LC resonator sensors	B
GND	2	No power supply to device	B
LPWRB	3	Failure to set functional mode	B
VDD	4	No power supply to device	B
INTB	5	INTB does not assert for button presses or error conditions	B
IN3	6	No LC sensor input	B
IN2	7	No LC sensor input	B
IN1	8	No LC sensor input	B
IN0	9	No LC sensor input	B
GND	10	No power supply to device	B
OUT3	11	Output is not connected to a load. May result in output status error	B
OUT2	12	Output is not connected to a load. May result in output status error	B
OUT1	13	Output is not connected to a load. May result in output status error	B
SDA	14	I^2C read/write will be non-functional	B
OUT0	15	Output is not connected to a load. May result in output status error.	B
SCL	16	I^2C read/write will be non-functional	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COM	1	GND	COM is grounded without a bypass capacitor. Will cause an error in sensor input and unpredictable LC sensor behavior	B
GND	2	LPWRB	Device stuck in Low Power Mode	B
LPWRB	3	VDD	Device stuck in Normal Power Mode	B
VDD	4	INTB	INTB stuck high; loss of INTB functionality	B
INTB	5	IN3	Loss of INTB functionality and error in sensor input	B
IN3	6	IN2	Error in LC sensor input	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN2	7	IN1	Error in LC sensor input	B
IN1	8	IN0	Error in LC sensor input	B
IN0	9	GND	No LC sensor input	B
GND	10	OUT3	May result in output status error	B
OUT3	11	OUT2	May result in output status error	B
OUT2	12	OUT1	May result in output status error	B
OUT1	13	SDA	May result in output status error	B
SDA	14	OUT0	I^2C read/write will be non-functional	B
OUT0	15	SCL	May result in output status error and I^2C read/write will be non-functional	B
SCL	16	COM	I^2C read/write will be non-functional	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COM	1	Will cause unpredictable LC sensor behavior	B
GND	2	Power supply shorted to ground	B
LPWRB	3	Device stuck in Normal Power Mode	B
VDD	4	Normal operation	D
INTB	5	Loss of INTB functionality	B
IN3	6	No LC sensor input	B
IN2	7	No LC sensor input	B
IN1	8	No LC sensor input	B
IN0	9	No LC sensor input	B
GND	10	Power supply shorted to ground	B
OUT3	11	Error in logic output	B
OUT2	12	Error in logic output	B
OUT1	13	Error in logic output	B
SDA	14	I^2C read/write will be non-functional	B
OUT0	15	Error in logic output	B
SCL	16	I^2C read/write will be non-functional	B

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