Functional Safety Information

TPS6244x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS62441-Q1 and TPS62442-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

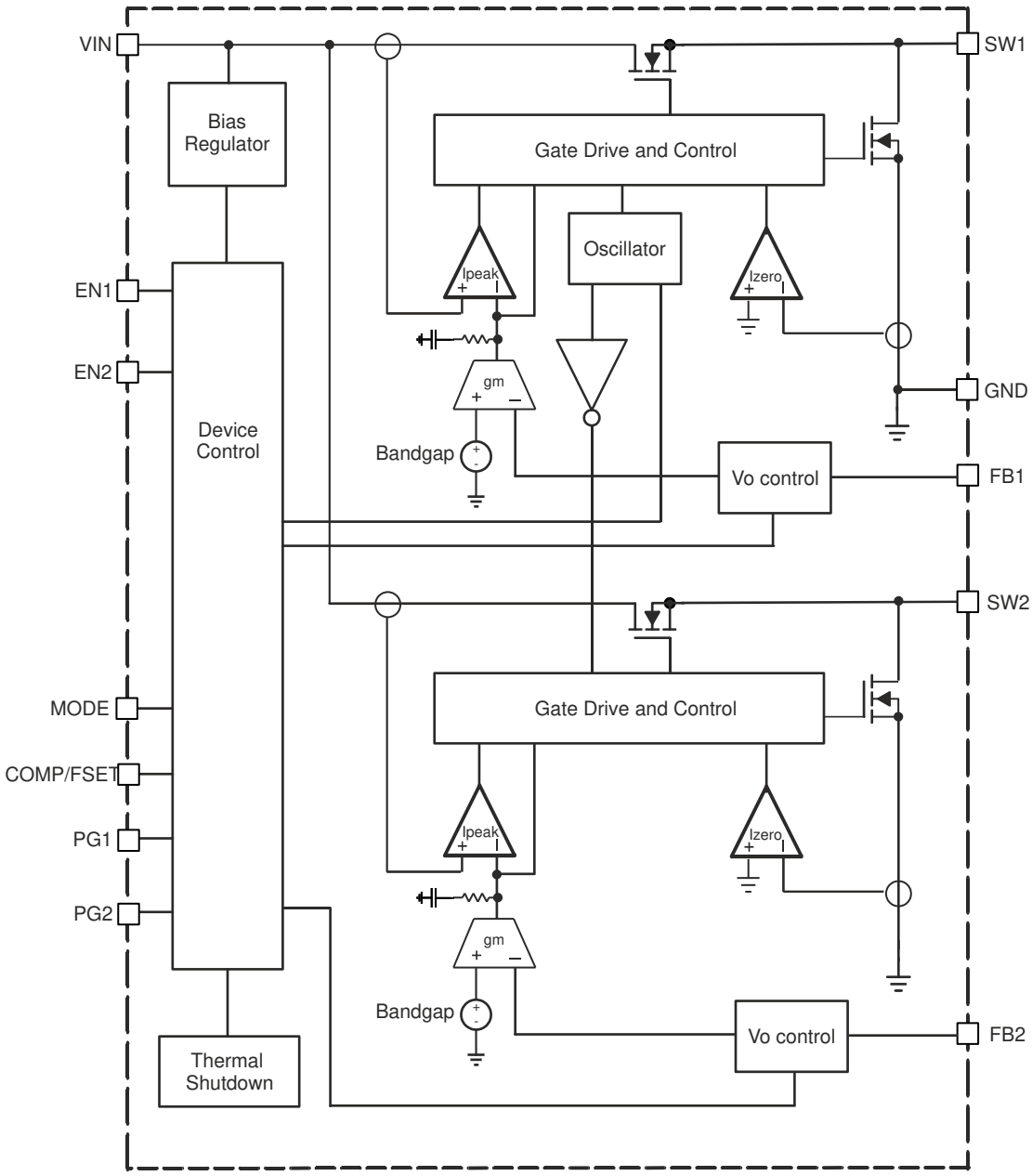

Figure 1-1. Functional Block Diagram

TPS6244x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS6244x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	5
Package FIT Rate	6

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS6244x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	24%
SW output not in specification – voltage or timing	11%
SW power HS or LS FET stuck on	28%
EN or PG false trip or fails to trip	12%
frequency or output voltage range not in spec	11%
no device communication	13%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS6244x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS6244x-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS6244x-Q1 data sheet.

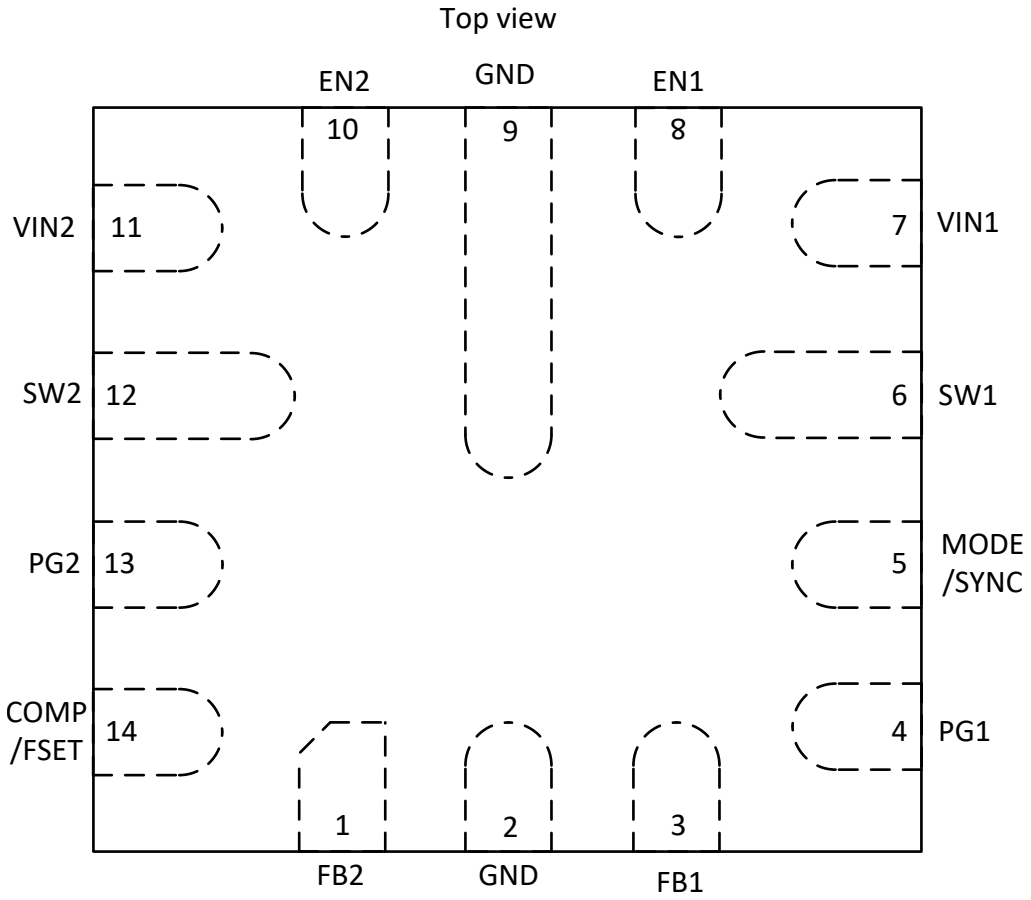

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application, please refer to the 'Simplified Schematics' on the 1st page in the TPS6244x-Q1 data sheet.

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FB2	1	Converter 2 output voltage regulated to VIN (100% mode)	B
GND	2	No effect, normal operation	D
FB1	3	Converter 1 output voltage regulated to VIN (100% mode)	B
PG1	4	No operation, no power good indication	B
MODE/SYNC	5	Intended functionality	D
SW1	6	Potential device damage	A
VIN1	7	Converter 1 does not power up, no output voltage on converter 1	B
EN1	8	Converter 1 is disabled, no output voltage on converter 1	B
GND	9	No effect, normal operation	D
EN2	10	Converter 2 is disabled, no output voltage on converter 2	B
VIN2	11	Converter 2 does not power up, no output voltage on converter 2	B
SW2	12	Potential device damage	A
PG2	13	No operation, no power good indication	B
COMP/FSET	14	Intended functionality, device operates in fix frequency	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FB2	1	Undetermined output voltage behavior of converter 2; open loop operation	B
GND	2	Device does not power up, no output volatge	B
FB1	3	Undetermined output voltage behavior of converter 1; open loop operation	B
PG1	4	Intended functionality	B
MODE/SYNC	5	Undetermined device operation	B
SW1	6	Output volatge 1 not functional, open loop operation.	B
VIN1	7	Converter 1 does not power up	B
EN1	8	Undetermined device operation; converter 1 might power up or not	B
GND	9	Device does not power up, no output volatge	B
EN2	10	Undetermined device operation; converter 2 might power up or not	B
VIN2	11	Converter 2 does not power up	B
SW2	12	Converter 2 not functional, open loop operation.	B
PG2	13	Intended functionality	B
COMP/FSET	14	Normal operation	D

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
FB1	3	PG1	Converter 2 does not regulate	B
PG1	4	MODE/SYNC	No device damage, but performance degradation	B
MODE/SYNC	5	SW1	Potential internal device damage	A
SW2	12	PG2	Potential internal device damage	A
PG2	13	COMP/FSET	Potential internal device damage	A
COMP/FSET	14	FB2	Converter 2 does not regulate	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
FB2	1	Potential device damage	A
GND	2	Device does not power up, no output voltage	B
FB1	3	Potential device damage	A
PG1	4	Potential device damage	A
MODE/SYNC	5	Intended functionality; FPWM mode	D
SW1	6	Potential device damge	A
VIN1	7	Normal operation	D
EN1	8	Intended functionality; Converter 1 enable	D
GND	9	Device does not power up, no output voltage	B
EN2	10	Intended functionality; Converter 2 enable	D
VIN2	11	Normal operation	D
SW2	12	Potential device damge	A
PG2	13	Potential device damage	A
COMP/FSET	14	Intended functionality; device operates in fix frequency	D

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