Functional Safety Information

TPS55288-Q1 and TPS552882-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS55288-Q1 and TPS552882-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagrams for reference.

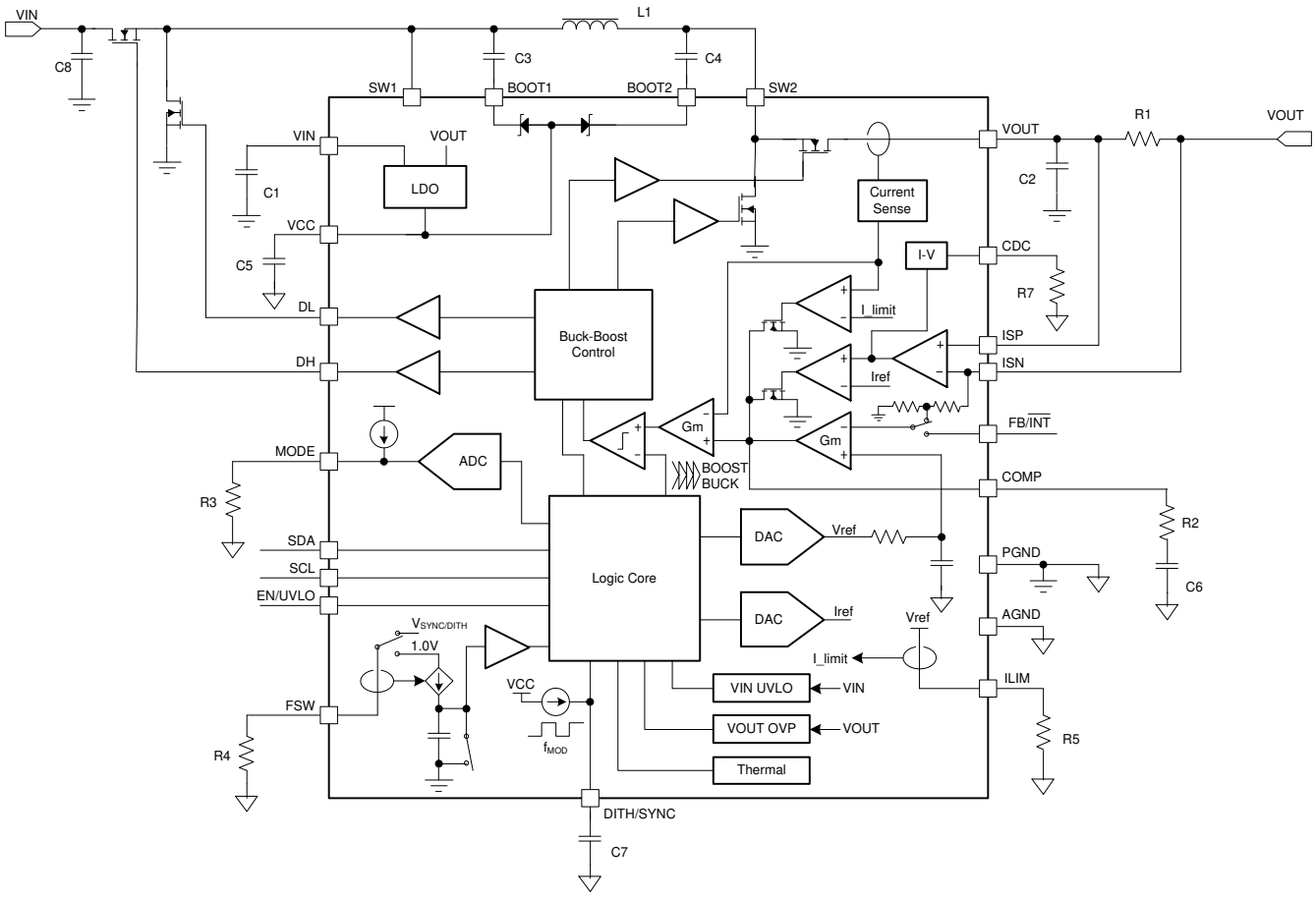

Figure 1-1. TPS55288-Q1 Functional Block Diagram

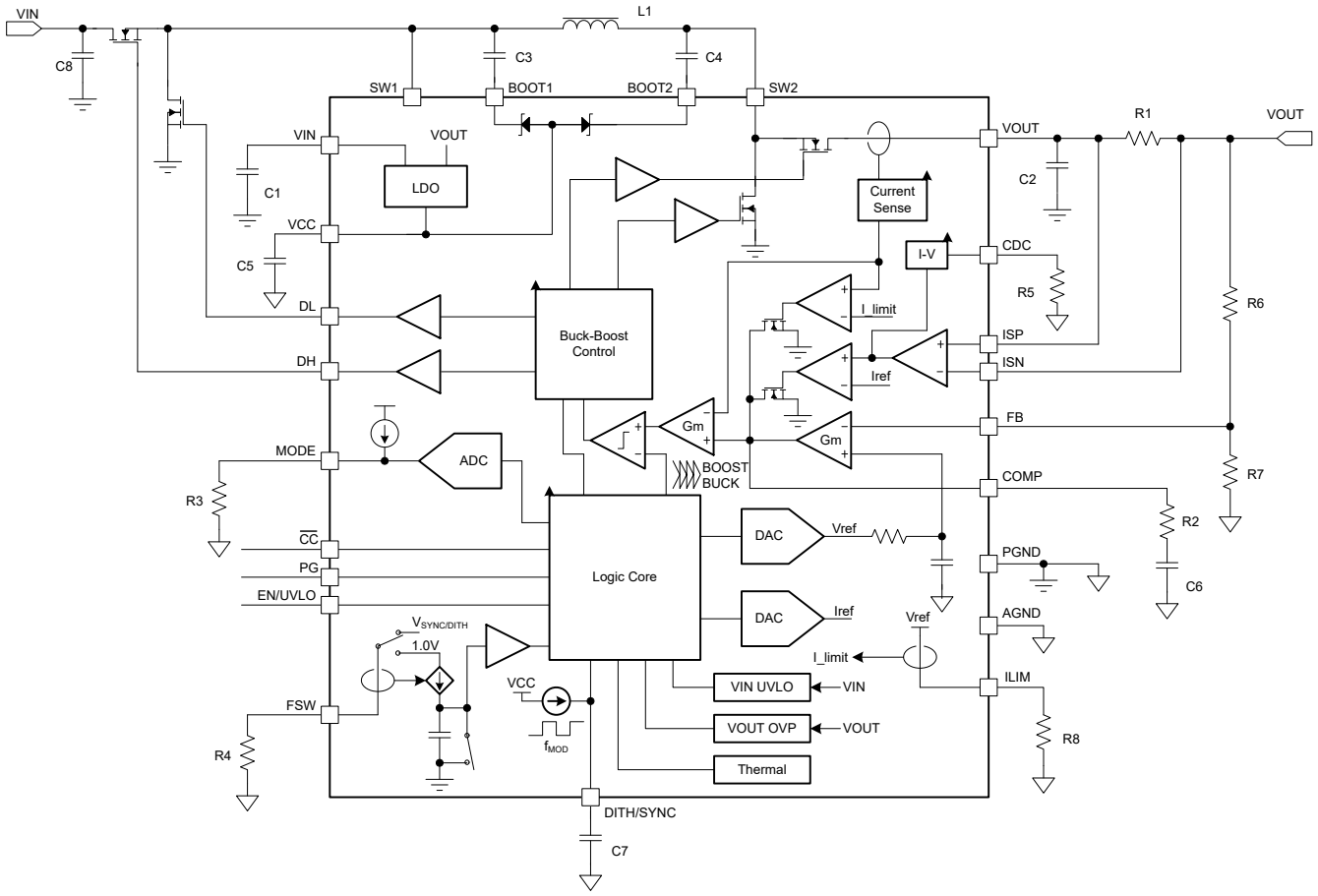

Figure 1-2. TPS552882-Q1 Functional Block Diagram

The TPS55288-Q1 and TPS552882-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS55288-Q1 and TPS552882-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	34
Die FIT Rate	11
Package FIT Rate	23

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1000 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS55288-Q1 and TPS552882-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO not in specification voltage or timing	50%
VO No output GND or HIZ	15%
SW FETs stuck on	25%
EN enable fails or false enable	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS55288-Q1 and TPS552882-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 and Figure 4-2 show the TPS55288-Q1 and TPS552882-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the *TPS55288-Q1 36-V, 16-A Buck-Boost Converter with I²C Interface* and *TPS552882-Q1 36-V, 16-A Buck-Boost Converter* data sheets.

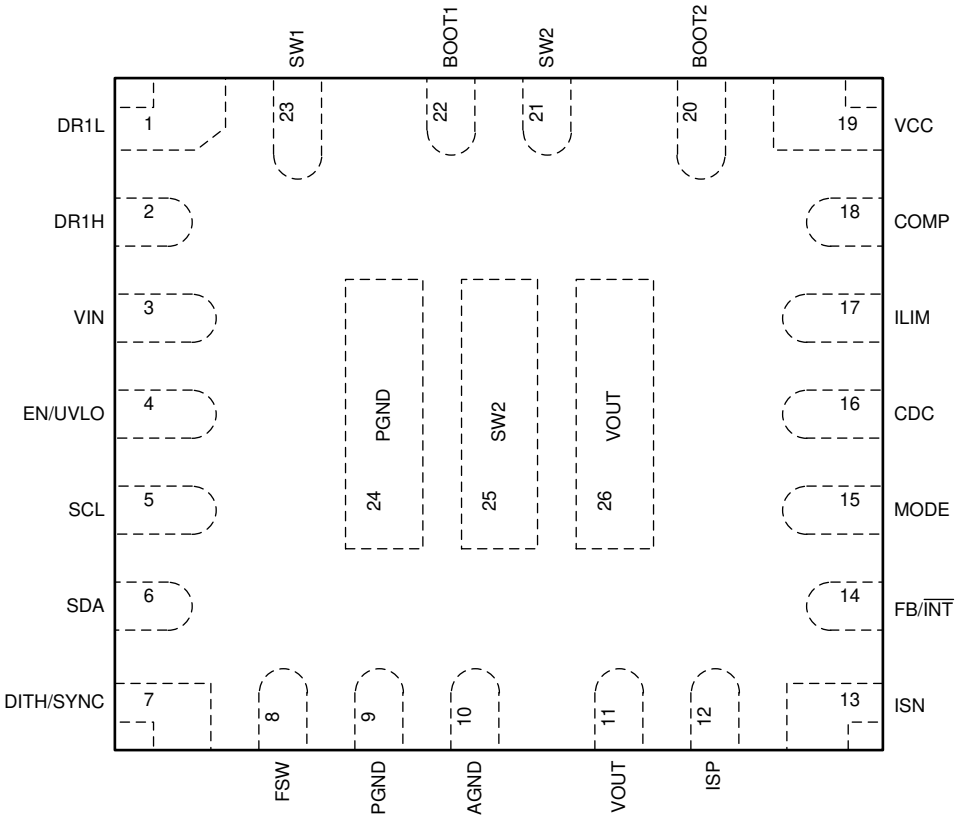

Figure 4-1. TPS55288-Q1 Pin Diagram

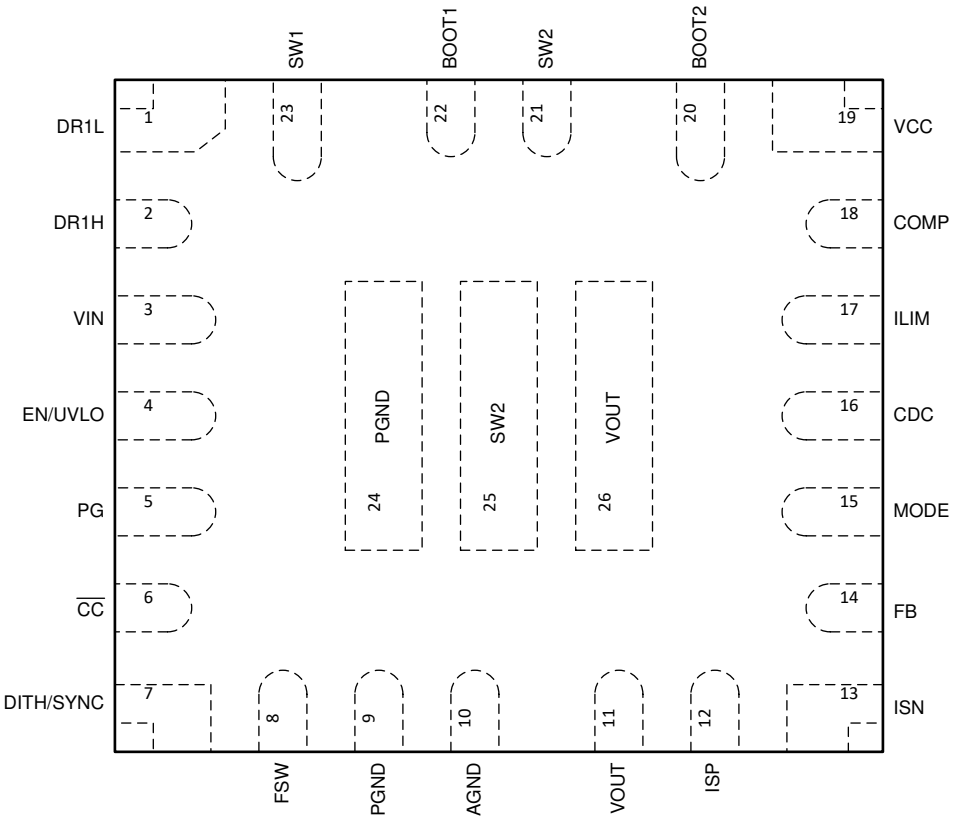

Figure 4-2. TPS552882-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the *TPS55288-Q1 36-V, 16-A Buck-Boost Converter with I²C Interface* and *TPS552882-Q1 36-V, 16-A Buck-Boost Converter* data sheets.
- Configuration as shown in the *Application and Implementation* found in the *TPS55288-Q1 36-V, 16-A Buck-Boost Converter with I²C Interface* and *TPS552882-Q1 36-V, 16-A Buck-Boost Converter* data sheets.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DR1L	1	Possible device damage	A
DR1H	2	No output voltage	B
VIN	3	The device does not operate. Power supply is short.	B
EN/UVLO	4	Loss of ENABLE functionality. The device remains in shutdown mode.	B
SCL	5	For the TPS55288-Q1, there is no output voltage.	B
PG		For the TPS552882-Q1, this is the correct output voltage. Loss of power-good indication functionality	C
SDA	6	For the TPS55288-Q1, there is no output voltage.	B
$\overline{CC}$		For TPS552882-Q1, this is the correct output voltage. Loss of constant current output indication functionality	C
DITH/SYNC	7	Correct output voltage. Loss of DITH/SYNC functionality	C
FSW	8	Possible device damage	A
PGND	9	No effect	D
AGND	10	The internal circuit can be disturbed.	C
VOUT	11	The device remains in hiccup output short circuit protection mode.	B
ISP	12	The device remains in hiccup output short circuit protection mode.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ISN	13	No output voltage	B
FB/INT	14	For the TPS55288-Q1, when internal feedback is used, this pin always indicates low even in the normal condition. When external feedback is used, OVP is triggered.	B
FB		For the TPS552882-Q1, OVP is triggered.	B
MODE	15	For the TPS55288-Q1, the device always works in FPWM mode with I^2C target address 74H, but no output voltage with I^2C target address 75H.	B
		For the TPS552882-Q1, the device remains in FPWM mode and internal VCC source. Loss of PFM mode and external VCC source functionality.	C
CDC	16	For the TPS55288-Q1, there is no effect when internal CDC compensation is used, but loss of the cable voltage drop compensation and the output voltage is overcompensated when external CDC compensation is used.	C
		For the TPS552882-Q1, there is loss of the cable voltage drop compensation functionality and the output voltage is overcompensated.	B
ILIM	17	Potential damage to inductor and chip	A
COMP	18	The output voltage is out of regulation. If in FPWM, the converter works in minimum t_{ON}. If in PFM, there is no switching.	B
VCC	19	The device does not operate. VCC is short.	B
BOOT2	20	No output voltage	B
SW2	21	Possible device damage	A
BOOT1	22	No output voltage	B
SW1	23	Possible device damage	A
PGND	24	No effect	D
SW2	25	Possible device damage	A
VOUT	26	The device remains in hiccup output short circuit protection mode.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DR1L	1	Correct output voltage. Efficiency is lower.	C
DR1H	2	No output voltage	B
VIN	3	The device does not work and there is no output voltage.	B
EN/UVLO	4	No output voltage. Loss of ENABLE functionality	B
SCL	5	For the TPS55288-Q1, there is no output voltage.	B
PG		For the TPS552882-Q1, this is the correct output voltage. Loss of power-good indication functionality	C
SDA	6	For the TPS55288-Q1, there is no output voltage.	B
$\overline{CC}$		For the TPS552882-Q1, this is the correct output voltage. Loss of constant current output indication functionality	C
DITH/SYNC	7	Correct output voltage. Loss of DITH/SYNC functionality	C
FSW	8	No output voltage	B
PGND	9	Possible device damage	A
AGND	10	Possible device damage	A
VOUT	11	Possible device damage	A
ISP	12	No output voltage	B
ISN	13	The output voltage is out of regulation.	B
FB/INT	14	For the TPS55288-Q1, there is a loss of the FAULT indicator function when internal feedback is used. OVP is triggered when external feedback is used.	B
FB		For the TPS552882-Q1, OVP is triggered.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE	15	For the TPS55288-Q1, the device always works in PFM mode with I^2C target address 75H and external VCC source. No output with I^2C target address 74H.	B
		For the TPS552882-Q1, the device remains in PFM mode and external VCC source. Loss of FPWM mode and internal VCC source functionality	C
CDC	16	Loss of CDC functionality and no cable voltage drop compensation	C
ILIM	17	The output current capability decreases.	B
COMP	18	Output voltage is out of regulation.	B
VCC	19	Possible device damage	A
BOOT2	20	Efficiency is lower.	B
SW2	21	Possible device damage	A
BOOT1	22	Possible device damage	A
SW1	23	Possible device damage	A
PGND	24	Possible device damage	A
SW2	25	Possible device damage	A
VOUT	26	Possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
DR1L	1	DR1H	No output voltage	B
DR1H	2	VIN	Possible device damage	A
VIN	3	EN/UVLO	The EN/UVLO pin is damaged if V_{IN} is higher than 20 V.	A
EN/UVLO	4	SCL	For the TPS55288-Q1, the SCL pin is damaged if EN/UVLO is higher than 6 V.	A
		PG	For the TPS552882-Q1, the PG pin is damaged if EN/UVLO is higher than 6 V.	A
SCL	5	SDA	For the TPS55288-Q1, there is no output voltage.	B
PG		$\overline{CC}$	For the TPS552882-Q1, this is the correct output voltage. Loss of PG and CC functionality	C
SDA	6	DITH/SYNC	For the TPS55288-Q1, this is the correct output voltage. Loss of DITH/SYNC functionality	C
$\overline{CC}$			For the TPS552882-Q1, this is the correct output voltage. Loss of CC and DITH/SYNC functionality	C
DITH/SYNC	7	FSW	Possible device damage	A
FSW	8	PGND	Possible device damage	A
PGND	9	AGND	The internal circuit can be disturbed.	C
AGND	10	VOUT	The device remains in hiccup output short circuit protection mode and the internal circuit can be disturbed.	B
VOUT	11	ISP	Output current limit accuracy is affected.	C
ISP	12	ISN	Correct output voltage. Loss of output current limit functionality	C
ISN	13	FB/INT	For the TPS55288-Q1, the FB/INT pin damaged if ISN is higher than 6 V.	A
		FB	For the TPS552882-Q1, output voltage equals 1.2 V.	B
FB/INT	14	MODE	For the TPS55288-Q1, no output voltage when internal feedback is used. When external feedback is used, OVP is triggered.	B
FB			For the TPS552882-Q1, OVP is triggered.	B
MODE	15	CDC	Loss of CDC functionality and output voltage is out of regulation.	B
CDC	16	ILIM	Incorrect current limit setting and CDC compensation	B
ILIM	17	COMP	Output voltage is out of regulation.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	18	VCC	OVP is triggered.	B
VCC	19	BOOT2	The VCC pin is damaged if BOOT2 is higher than 6 V.	A
BOOT2	20	SW2	Efficiency is lower because the boost HFET is always off.	C
SW2	21	BOOT1	Possible device damage	A
BOOT1	22	SW1	Output voltage is out of regulation.	B
SW1	23	DR1L	Possible device damage if SW1 is higher than 6 V	A
PGND	24	SW2	Potential device damage	A
SW2	25	VOUT	Possible device damage	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DR1L	1	The DR1L pin is damaged if supply voltage is higher than 6 V.	A
DR1H	2	Possible device damage	A
VIN	3	No effect	D
EN/UVLO	4	The EN/UVLO pin is damaged if supply voltage is higher than 20 V.	A
SCL	5	For the TPS55288-Q1, the SCL pin is damaged if supply voltage is higher than 6 V.	A
PG		For the TPS552882-Q1, the PG pin is damaged if supply voltage is higher than 6 V.	A
SDA	6	For the TPS55288-Q1, the SDA pin is damaged if supply voltage is higher than 6 V.	A
$\overline{CC}$		For the TPS552882-Q1, the CC pin is damaged if supply voltage is higher than 6 V.	A
DITH/SYNC	7	The DITH/SYNC pin is damaged if supply voltage is higher than 6 V.	A
FSW	8	The FSW pin is damaged if supply voltage is higher than 6 V.	A
PGND	9	The device does not operate. Power supply is short.	B
AGND	10	The device does not operate. Power supply is short.	B
VOUT	11	The VOUT pin is damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
ISP	12	The ISP pin is damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
ISN	13	The ISN pin damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A
FB/INT	14	For the TPS55288-Q1, the FB/INT pin is damaged if supply voltage is higher than 6 V.	A
FB		For the TPS552882-Q1, the FB pin is damaged if supply voltage is higher than 6 V.	A
MODE	15	The MODE pin is damaged if supply voltage is higher than 6 V.	A
CDC	16	The CDC pin is damaged if supply voltage is higher than 6 V.	A
ILIM	17	The ILIM pin is damaged if supply voltage is higher than 6 V.	A
COMP	18	The COMP pin is damaged if supply voltage is higher than 6 V.	A
VCC	19	The VCC pin is damaged if supply voltage is higher than 6 V.	A
BOOT2	20	The BOOT2 pin is damaged if supply voltage is higher than 31 V.	A
SW2	21	The SW2 pin is damaged if supply voltage is higher than 25 V and internal power FETs are damaged.	A
BOOT1	22	Possible device damage	A
SW1	23	Damage to internal power FETs	A
PGND	24	The device does not operate. Power supply is short.	B
SW2	25	The SW2 pin is damaged if supply voltage is higher than 25 V and internal power FETs are damaged.	A
VOUT	26	The VOUT pin damaged if supply voltage is higher than 25 V. The output voltage is equal to the supply voltage.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2022) to Revision A (October 2022)	Page
• Removed reference of FMD	5

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