Functional Safety Information

TPS22954-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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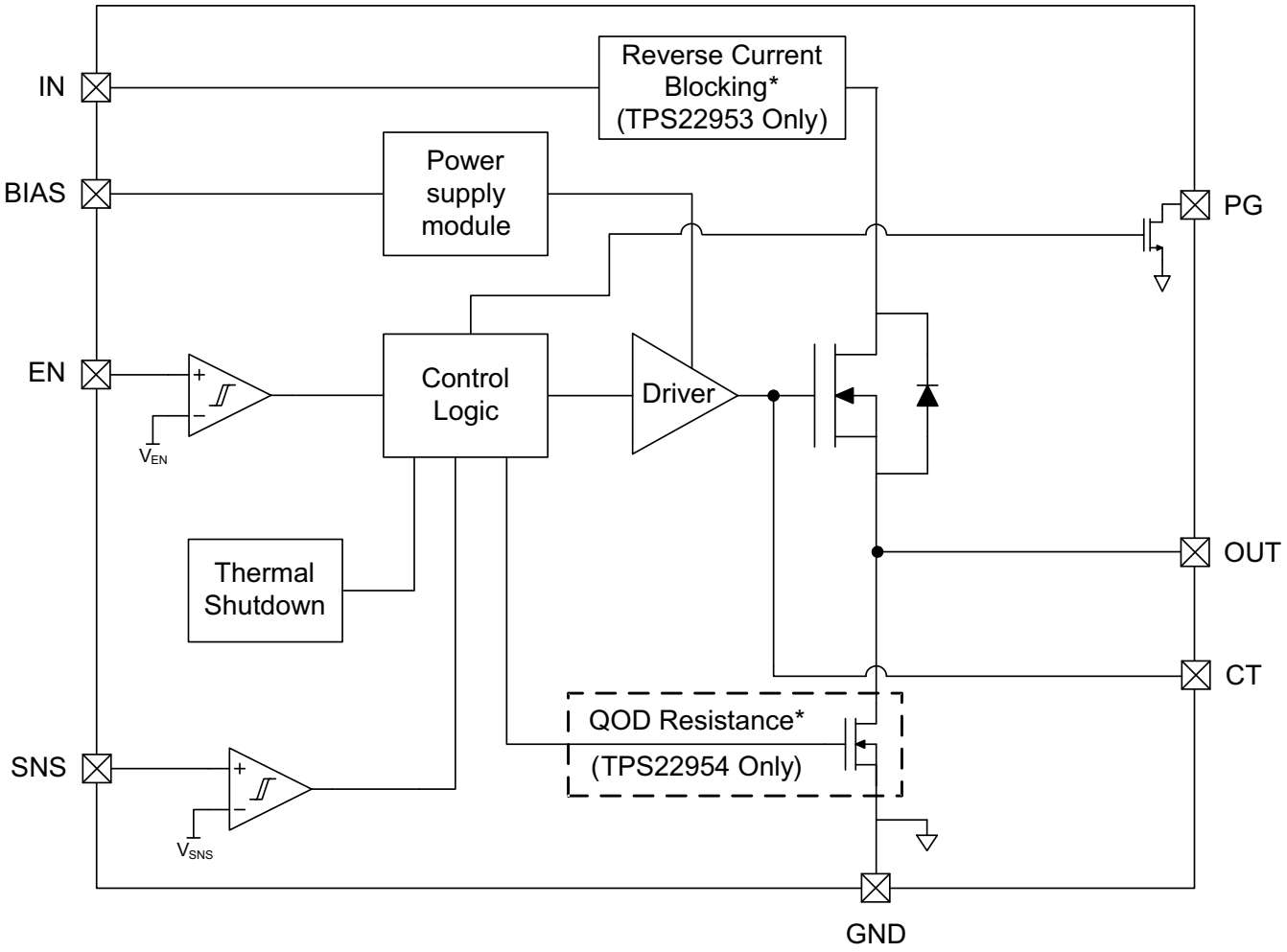
1 Overview

This document contains information for the TPS22954-Q1 (DQC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



(*) Only active when the switch is disabled.

Figure 1-1. Functional Block Diagram

The TPS22954-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS22954-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	3
Package FIT rate	3

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS22954-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT to GND	40
VOUT open or Hi-Z	20
VOUT outside specification (voltage or rise time)	30
QOD short to GND	5
Pin to pin short (any two pins)	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS22954-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (see Table 4-5)
- Pin short-circuited to supply (see Table 4-6)

Table 4-3 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The absolute maximum ratings for the device are not exceeded.

Figure 4-1 shows the TPS22954-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS22954-Q1 datasheet.

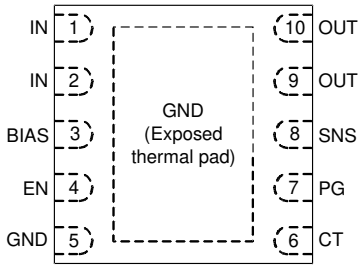


Figure 4-1. Pin Diagram (Top View)

Table 4-2. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input. Bypass this input with a ceramic capacitor to GND.
2			
3	BIAS	I	Bias pin and power supply to the device.
4	EN	I	Active high switch enable or disable input. Also acts as the input UVLO pin. Use external resistor divider to adjust the UVLO level. Do not leave floating.
5	GND	—	Device ground.
6	CT	O	V_{OUT} slew rate control. Place ceramic cap from CT to GND to change the V_{OUT} slew rate of the device and limit the inrush current. CT capacitor must be rated to 25V or higher.
7	PG	O	Power good. This pin is open drain which pulls low when the voltage on EN or SNS (or both) is below the respective VIL level.
8	SNS	I	Sense pin. Use external resistor divider to adjust the power good level. Do not leave floating.
9	OUT	O	Switch output.
10			

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	The power supply is shorted.	D
	2		
BIAS	3	There is no power supply to the device. The device does not pass through voltage to the VOUT pin.	B
EN	4	The device is disabled.	D
GND	5	This is the GND pin. The device operates as normal.	D
CT	6	Grounding this pin prevents the device from turning on and potentially damages the device.	A
PG	7	Open drain output, is not pulled up if connected to ground.	B
SNS	8	$V_{IH,SNS}$ is set to 0V, and the PG pin does not function properly.	B
OUT	9	If the device is enabled, the device does not limit the power supply current and is damaged.	A
	10		

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	There is no power supply to the device. The device does not pass through voltage to the VOUT pin.	D
	2		
BIAS	3	There is no power supply to the device. The device does not pass through voltage to the VOUT pin.	B
EN	4	The ON pin potentially floats high or low, the state of the output is unknown.	B
GND	5	There is no GND connection to the device. The device is not functional.	B
CT	6	Opening this pin quickens the output rise time if a CT capacitor is attached.	C
PG	7	The power-good signal is disconnected from the system.	D
SNS	8	The $V_{IH,SNS}$ setting and the state of the PG pin are unknown.	B
OUT	9	The output does not deliver the voltage to the load.	D
	10		

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	BIAS	A stronger supply powers the IN and BIAS pins. The operation of the device is potentially affected, however, there is no damage to the device.	B
	2			
BIAS	3	EN	The device is enabled if the BIAS power supply is above the ON threshold (V_{IH}).	D
EN	4	GND	The device is disabled.	D
CT	6	PG	Connecting these pins prevents the device from turning on and potentially damages the device.	A
PG	7	SNS	The PG pin threshold varies, there is no damage to the device.	B
SNS	8	OUT	The $V_{IH,SNS}$ is set to VOUT.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	The device operates normally, as expected.	D
	2		
EN	3	The device is enabled if the power supply is above the ON threshold (V_{IH}).	D
BIAS	4	The device operates normally, as expected.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	5	The power supply is shorted.	D
CT	6	Biasing the CT pin can potentially damage the device.	A
PG	7	The PG pin potentially pulls too much current from the supply and damages the device.	A
SNS	8	The $V_{IH,SNS}$ is set to the supply voltage.	B
OUT	9	The power MOSFET is shorted. Disabling the device no longer blocks power to the VOUT pin.	B
	10		

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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