Functional Safety Information

TPSM82866A and TPSM82864A Pin Failure Mode Analysis (Pin FMA)

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Trademarks

1 Overview

This document contains the Pin failure mode analysis (pin FMA) information for the TPSM82866A and TPSM82864A (B0QFN package).

Figure 1-1 shows the device functional block diagram for reference.

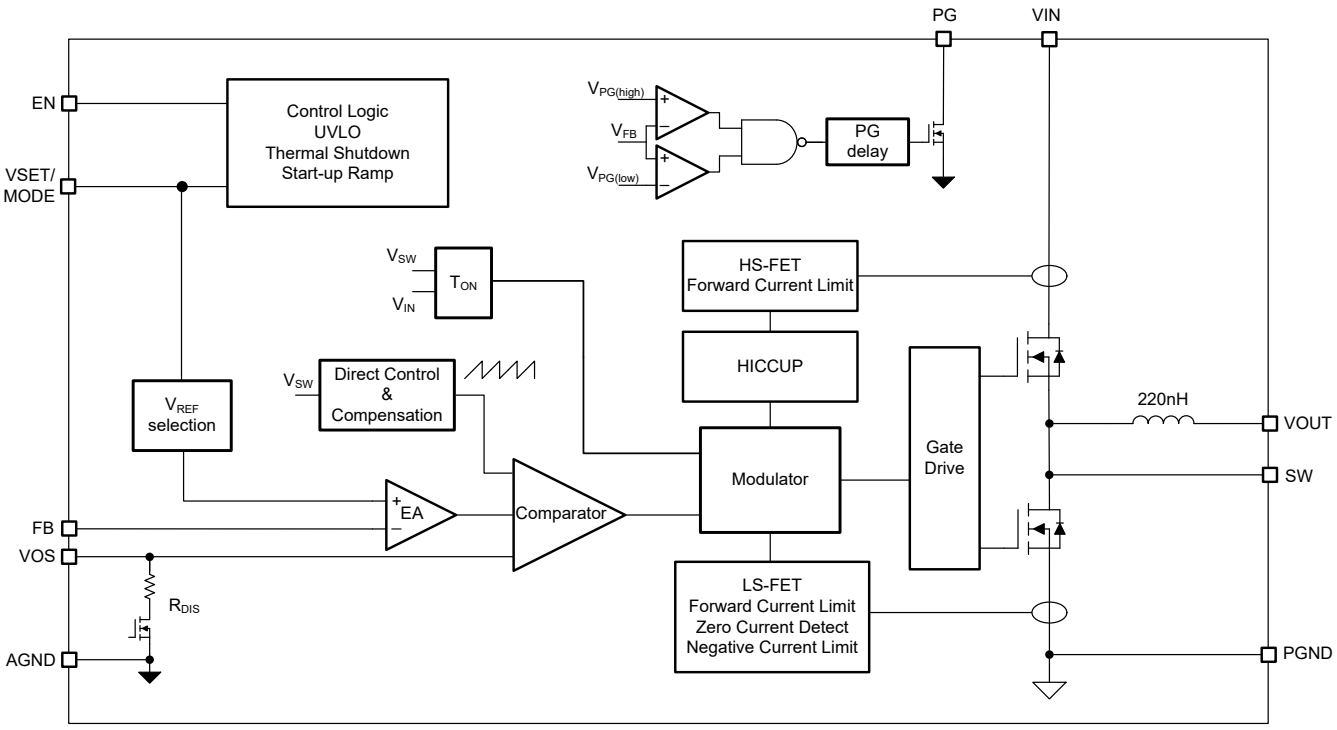

Figure 1-1. Functional Block Diagram

The TPSM8286xA was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSM8286xA. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 2-2)
- Pin open-circuited (see Table 2-3)
- Pin short-circuited to an adjacent pin (see Table 2-4)
- Pin short-circuited to VIN (see Table 2-5)

Table 2-2 through Table 2-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 2-1.

Table 2-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 2-1 shows the TPSM8286xA pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPSM8286xA data sheet.

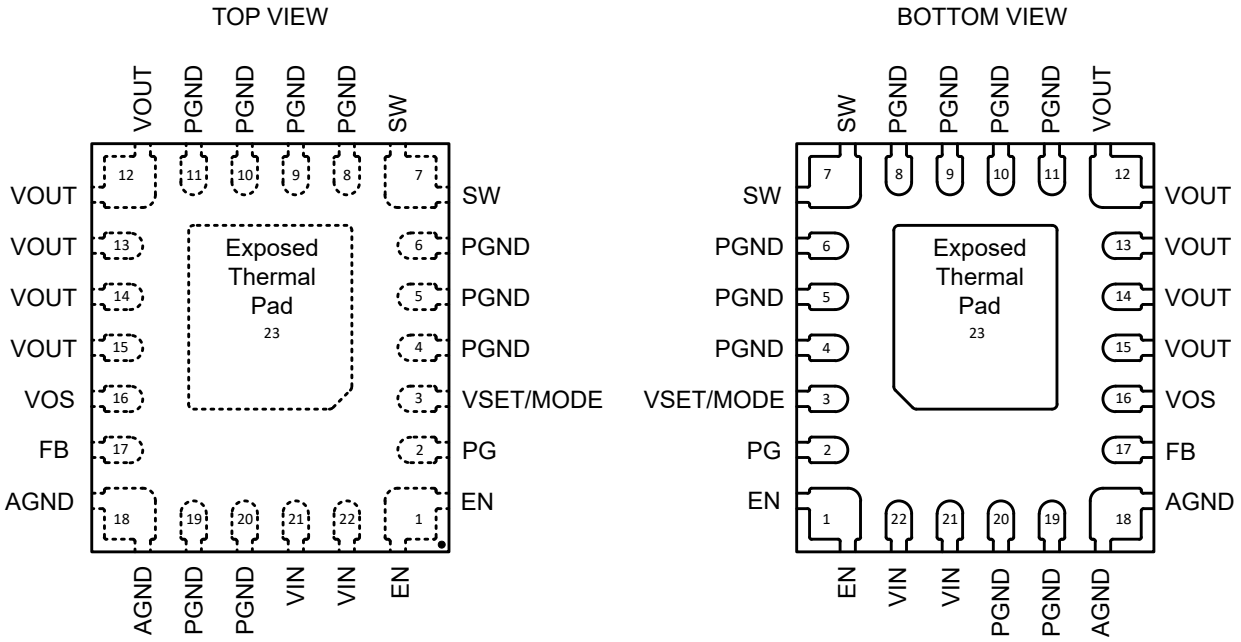

Figure 2-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in the typical application, please refer to the *Typical Application* on the first page in the TPSM8286xA data sheet.

Table 2-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	The device will not be enabled.	B
PG	2	Loss of PG functionality	B
VSET/ MODE	3	Intended functionality for the adjustable output voltage configuration in power save mode. For the fixed output voltage configuration, the output voltage will be regulated to 0.6 V.	B
PGND	4, 5, 6, 8, 9, 10, 11, 19, 20	Intended functionality	D
SW	7	Potential device damage	A
VOUT	12, 13, 14, 15	No output voltage	B
VOS	16	No output voltage	B
FB	17	Output voltage will not be regulated. The device will enter 100% mode.	B
AGND	18	Intended functionality	D
VIN	21, 22	The device is not functional.	A

Table 2-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Undetermined state of the pin. The device may or may not be enabled.	B
PG	2	Loss of PG functionality	B
VSET/ MODE	3	Will operate in forced PWM mode. If configured for the fixed output voltage configuration, the output voltage will be regulated to 0.6 V.	B
PGND	4, 5, 6, 8, 9, 10, 11, 19, 20	Redundant pin. If one of the pins are open, there is no functionality loss but there is a potential impact on device performance.	C
SW	7	Intended functionality	D
VOUT	12, 13, 14, 15	Redundant pin. If one of the pins are open, there is no functionality loss but there is a potential impact on device performance.	C
VOS	16	Output voltage regulation will be worse.	C
FB	17	The device is not functional. Open loop operation	B
AGND	18	The device is not functional.	B
VIN	21, 22	Redundant pin. If one of the pins are open, there is no functionality loss but there is a potential impact on device performance.	C

Table 2-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	PG	2	Loss of EN and PG functionality. Potential device damage	A
PG	2	VSET/ MODE	3	Intended functionality for the adjustable output voltage configuration in power save mode. For the fixed output voltage configuration, the output voltage will be regulated to 0.6 V. If configured for forced PWM mode operation, there is potential device damage.	A
VSET/ MODE	3	PGND	4	Intended functionality for the adjustable output voltage configuration in power save mode. For the fixed output voltage configuration, the output voltage will be regulated to 0.6 V. If configured for forced PWM mode operation, the device is not functional.	A
PGND	6	SW	7	Potential device damage	A
PGND	11	VOUT	12	No output voltage	B
VOUT	15	VOS	16	Intended functionality	D
VOS	16	FB	17	Intended functionality for the fixed output voltage configuration. For the adjustable output voltage configuration, the output voltage will be regulated to 0.6 V.	B
FB	17	AGND	18	Output voltage will not be regulated. The device will enter 100% mode.	B
AGND	18	PGND	19	Intended functionality	D
PGND	20	VIN	21	The device is not functional.	A
VIN	22	EN	1	Loss of EN functionality	B

Table 2-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Loss of EN functionality	B
PG	2	Loss of PG functionality. Potential device damage	A
VSET/ MODE	3	Intended functionality for the adjustable output voltage configuration in forced PWM mode. For the fixed output voltage configuration, the output voltage will be regulated to 0.6 V.	B
PGND	4, 5, 6, 8, 9, 10, 11, 19, 20	The device is not functional.	A
SW	7	Potential device damage	A
VOUT	12, 13, 14, 15	Potential device damage	A
VOS	16	Potential device damage	A
FB	17	Output voltage will not be regulated. If configured in forced PWM mode, there is potential device damage.	A
AGND	18	The device is not functional.	A
VIN	21, 22	Intended functionality	D

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