Functional Safety Information

LM708x0-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for LM708x0-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

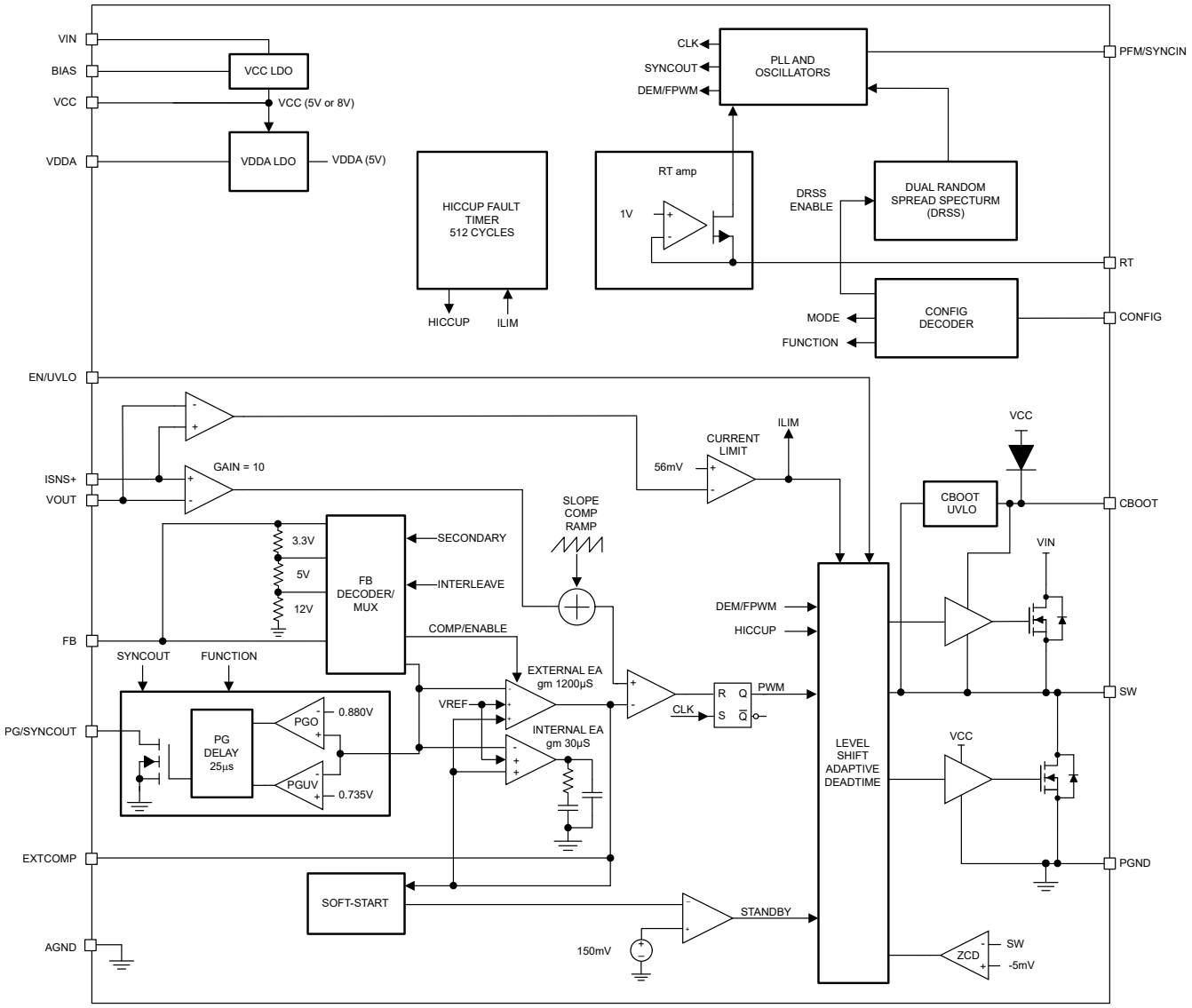

Figure 1-1. Functional Block Diagram

LM708x0-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM708x0-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
	LM70880-Q1	LM70860-Q1	LM70840-Q1
Total component FIT rate	34	29	26
Die FIT rate	11	7	5
Package FIT rate	23	22	21

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from Table 11
- LM70880 power dissipation: 2.6W
- LM70860 power dissipation: 1.75W
- LM70840 power dissipation: 1.25W
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Device	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog and mixed HV > 50V supply	LM70880-Q1	30 FIT	75°C
5	CMOS, BICMOS ASICs Analog and mixed HV > 50V supply	LM70860-Q1	30 FIT	75°C
5	CMOS, BICMOS ASICs Analog and mixed HV > 50V supply	LM70840-Q1	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM708x0-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW No output	50
SW output not in specification - voltage or timing	40
SW power FET stuck on	5
PGOOD false trip or fails to trip	5

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM708x0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM708x0-Q1 pin diagram. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the LM708x0-Q1 data sheet.

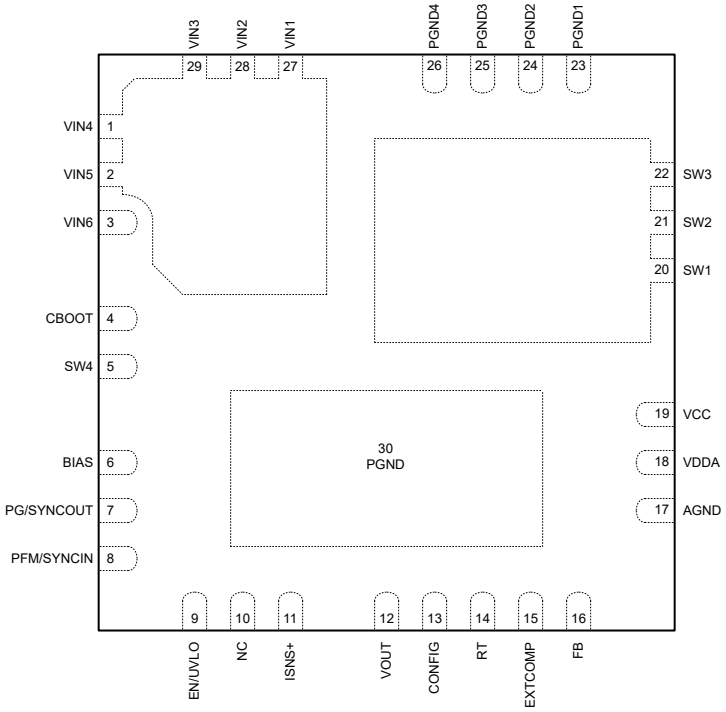

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application Circuit is used per the LM708x0-Q1 data sheet
  - PG is pulled up to VOUT

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1-3	VOUT = 0V	B
CBOOT	4	VOUT = 0V, VCC regulator loaded to Current Limit	B
SW	5	VOUT = 0V, high-side FET shorted from VIN to GND	A
BIAS	6	VOUT = expected VOUT, internal VCC regulator provides bias voltage	D
PGOOD	7	VOUT = expected VOUT	D
PFM/SYNC	8	VOUT = expected VOUT, no synchronization possible and is in FPWM mode	C
EN/UVLO	9	VOUT = 0V, enters shutdown mode	B
NC	10	N/A	D
ISNS+	11	VOUT = 0V, HO damaged	A
VOUT	12	Current limit reached, VOUT = 0V and enters hiccup mode	B
CONFIG	13	Expected VOUT, spread spectrum and multiphase mode disabled	C
RT	14	VOUT = expected VOUT, FSW at maximum causing maximum power dissipation	C
EXTCOMP	15	VOUT = 0V	B
FB	16	Internal FB MODE, VOUT = expected VOUT	D
		External FB MODE VOUT = VIN	A
AGND	17	AGND is GND, VOUT = expected VOUT	D
VDDA	18	VOUT = 0V, no switching, loaded VCC output	B
VCC	19	VOUT = 0V, no switching, loaded VCC output	B
SW	20-22	VOUT = 0V, high-side FET shorted from VIN to GND	A
PGND	23-26	PGND is GND, VOUT = expected VOUT	D
VIN	27-29	VOUT = 0V	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1-3	VOUT = expected VOUT, part works through VIN on pins 27-29	D
CBOOT	4	VOUT = 0V	B
SW	5	VOUT = expected VOUT, part works through SW on pins 20-22	D
BIAS	6	VCC working off internal VCC regulator	D
PGOOD	7	If in single mode, PGOOD has no effect on operation	D
		If in multiphase primary mode, the secondary detects no clock input and shuts down	B
PFM/SYNC	8	VOUT = expected VOUT	C
EN/UVLO	9	Device state in indeterminate	B
NC	10	VOUT = expected VOUT	D
ISNS+	11	OPEN current sense pin blocks current limit and causes VOUT oscillations	A
VOUT	12	VOUT = 0V	B
CONFIG	13	CONFIG is used during start up, VOUT = expected VOUT	D
RT	14	RT regulates to 500mV but internal oscillator does not function	B
EXTCOMP	15	VOUT oscillates, if VOUT oscillates to VIN, damage can occur if VIN > 60V	A
FB	16	If external FB mode, VOUT is indeterminate	B
		If Internal FB mode, VOUT operates normally	D
AGND	17	VOUT is indeterminate	D
VDDA	18	Poor noise immunity	D
VCC	19	VOUT = expected VOUT until damage occurs	A
SW	20-22	VOUT = 0V	B
PGND	23-26	VOUT is indeterminate	B
VIN	27-29	VOUT = expected VOUT, part works through VIN on pins 1-3	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	1	NC	No impact	D
NC	2	CNFG	No impact	D
CNFG	3	RT	VOUT = expected VOUT with erratic switching	B
RT	4	EXTCOMP	COMP cannot regulate down due to clamping by internal RT	B
EXTCOMP	5	FB	External FB mode: COMP regulates to 0.8V and output is unregulated, VOUT = indeterminate	B
			Internal FB mode: COMP rises up to VDDA, VOUT = VIN	A
FB	6	AGND	External FB mode: VOUT = VIN	A
			Internal FB mode: VOUT = expected VOUT	D
AGND	7	VDDA	VDDA is grounded, VOUT = 0V	B
VDDA	8	VCC	VOUT = expected VOUT	D
VCC	9	PGND	VCC is grounded, VOUT = 0V	B
PGND	10	LO	VOUT = 0V, VCC is loaded by the LO driver	B
LO	11	VIN	VOUT = 0V, the driver is damaged if VIN > 6.5V	A
VIN	12	HO	VOUT = VIN	A
HO	13	SW	VOUT = 0V	B
SW	14	CBOOT	VOUT = 0V	B
CBOOT	15	VCCX	VOUT < 5V	A
VCCX	16	PG	PG pulldown can damage, VOUT = expected VOUT	A
PG	17	PFM/SYNC	VOUT = expected VOUT	C
PFM/SYNC	18	EN	VOUT = expected VOUT	A
EN	19	ISNS+	EN is high-voltage rated, VOUT = expected VOUT, if VOUT > 1V If VOUT < 1V, the device is disabled	B
ISNS+	20	VOUT	Current limit is disabled since the current limit resistor is shorted VOUT cannot regulate since current mode feedback is shorted	A
VOUT	21	NC	No impact	D
NC	22	NC	No impact	D
NC	23	NC	No impact	D
NC	24	NC	No impact	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1-3	No impact	D
CBOOT	4	If VIN < 6.5V, VOUT = expected VOUT, erratic switching	C
		If VIN > 6.5V, exceeds max ratings and CBOOT pin is damaged, HO bias damage	A
SW	5	VOUT=VIN, excess current from VIN through low-side FET	B
BIAS	6	If VIN < 40V, VOUT = expected VOUT	D
		If VIN > 40V, exceeds maximum ratings and the pin VCC is damaged, VOUT = 0V	A
PGOOD	7	If VIN < 6.5V, VOUT = expected, PG possibly forced high exceeding the PG pulldown SOA	B
		If VIN > 6.5V, exceeds maximum ratings and pin PG is destroyed, VOUT = expected VOUT	B
PFM/SYNC	8	If VIN < 6.5V, VOUT = expected VOUT	D
		If VIN > 6.5V, exceeds maximum ratings and pin PFM/SYNC is destroyed VOUT = expected VOUT	D
EN/UVLO	9	Part is always be enabled, VOUT = expected VOUT	C
NC	10	No impact	D
ISNS+	11	if VIN < 6.5V, VOUT = VIN	B
		If VIN > 60V, exceeds maximum ratings and pin ISNS+ is damaged. VOUT = VIN	A
VOUT	12	If VIN < 6.5V, VOUT = VIN	D
		If VIN > 60V, exceeds maximum ratings and pin VOUT is damaged, VOUT = VIN	A
CONFIG	13	If VIN < 6.5V, VOUT = expected VOUT	B
		If VIN > 6.5V, exceeds maximum ratings and pin CONFIG is destroyed	A
RT	14	If VIN < 6.5V, VOUT= 0V as frequency goes to 0Hz	B
		If VIN > 6.5V, exceeds maximum ratings and pin RT is destroyed	A
EXTCOMP	15	This brings VCC up to VIN, VOUT = VIN	A
FB	16	If VIN > 16V (fixed version) or 5.5V (adjustable version) damage occurs,VOUT = 0V	B
AGND	17	VIN shorts to GND, VOUT = 0V	A
VDDA	18	If VIN < 6.5V, no impact	D
		If VIN > 6.5V, exceeds maximum ratings and pin VDDA is damaged	A
VCC	19	If VIN < 12V, no impact	D
		If VIN > 12V, exceeds maximum ratings and pin VCC is damaged	A
SW	20-22	VOUT = VIN, excess current from VIN through low-side FET	B
PGND	23-26	VIN shorts to GND. VOUT = 0V	A
VIN	27-29	No impact	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2024) to Revision A (August 2024) **Page**

- Updated the functional block diagram image.....2
- Added dissipation numbers for all three options instead of just lead option.....3
- Updated the pin diagram image.....5

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265