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1 Overview

This document contains information for TPS628523HA-Q1 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

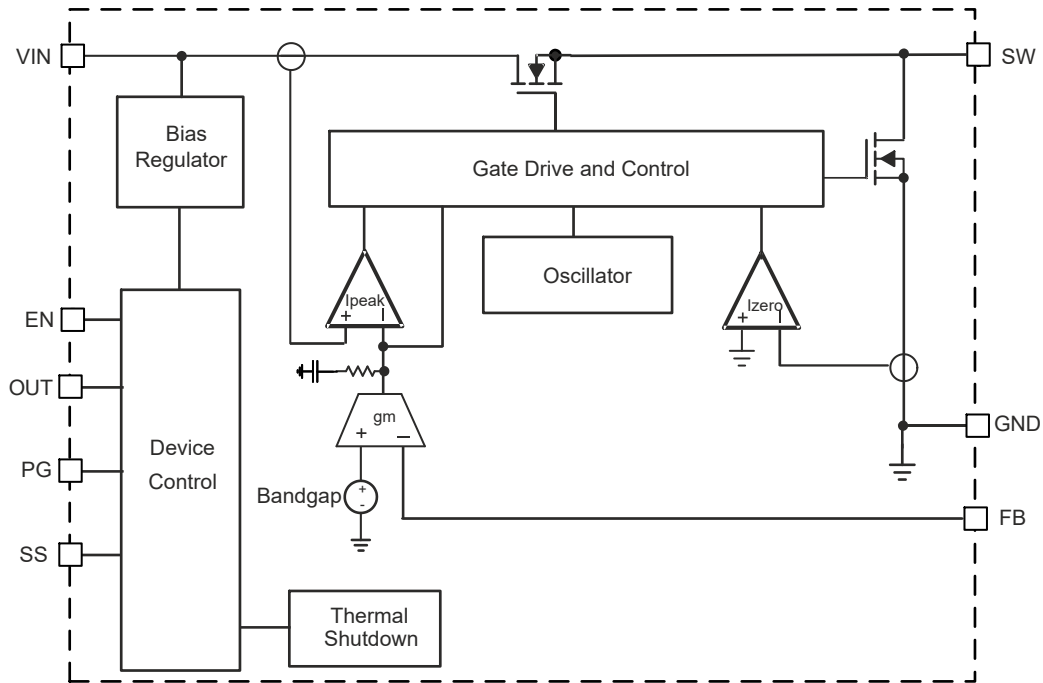


Figure 1-1. Functional Block Diagram

TPS628523HA-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS628523HA-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-1](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	8
Die FIT Rate	6
Package FIT Rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 422mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T

Table	Category	Reference FIT Rate	Reference Virtual T _j
5	CMOS, BICMOS Digital, analog/ mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_j (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS628523HA-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35%
SW output not in specification - voltage or timing	45%
SW power HS or LS FET stuck on	10%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS628523HA-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VIN (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Table 4-1](#) shows the TPS628523HA-Q1 pin diagram. For a detailed description of the device pins, please refer to the 'Pin Configuration and Functions' section in the TPS628523HA-Q1 data sheet.

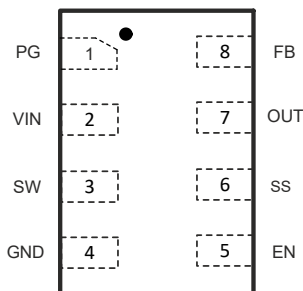


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in the typical application. Please refer to the 'Simplified Schematics' on the first page in the TPS628523HA-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PG	1	No device damage, but loss of functionality	B
VIN	2	Device does not power up	B
SW	3	Potential device damage that affects functionality	A
GND	4	No device damage, no impact to functionality	D
EN	5	Device is disabled. No device damage, but loss of functionality	B
SS	6	Output voltage will not ramp up. No device damage, but loss of functionality	B
OUT	7	No device damage, but performance degradation	C
FB	8	Open loop operation and device performance degradationC	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PG	1	False PG indication	B
VIN	2	Device does not power up	B
SW	3	Device not functional; open loop operation	B
GND	4	Potential device damage	A
EN	5	Undetermined device operation; device might power up or not	B
SS	6	SS time given by internal min SS time	C
OUT	7	No device damage but performance degradation	C
FB	8	Device not functional; open loop operation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PG	1	VIN	No device damage, but performance degradation. False PG indication	C
VIN	2	SW	Potential device damage	A
SW	3	GND	Potential device damage	A
EN	5	SS	Loss of functionality	B
SS	6	OUT	Loss of functionality	B
OUT	7	FB	No device damage, but performance degradation.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class PG
PG	1	No device damage, but loss of functionality. False PG indication	B
VIN	2	Intended functionality	D
SW	3	Potential device damage	A
GND	4	Device not functional	B
EN	5	Device always enabled. No device damage, but loss of functionality in case of EN=0	B
SS	6	SS time given by internal min SS time	C
OUT	7	No device damage, but performance degradation	C
FB	8	Device not functional; Open loop operation	B

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