Functional Safety Information

TL1963A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TL1963A-Q1 (KTT package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

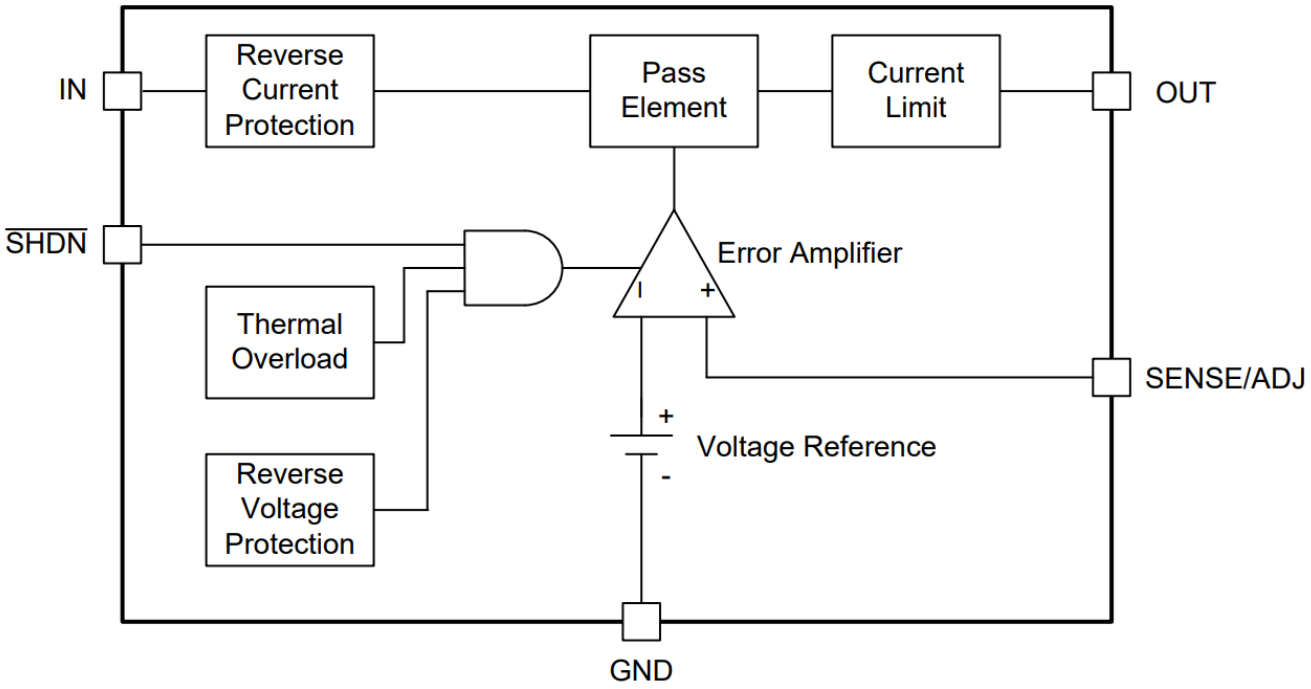

Figure 1-1. Functional Block Diagram

The TL1963A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TL1963A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	101
Die FIT rate	4
Package FIT rate	97

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 750mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator ≤ 1 Watt - (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TL1963A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	10
VOUT not in specification - voltage or timing	35
VOUT low (no output)	50
Short circuit on any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TL1963A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)

Table 4-2 through Table 4-4 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TL1963A-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TL1963A-Q1 data sheet.

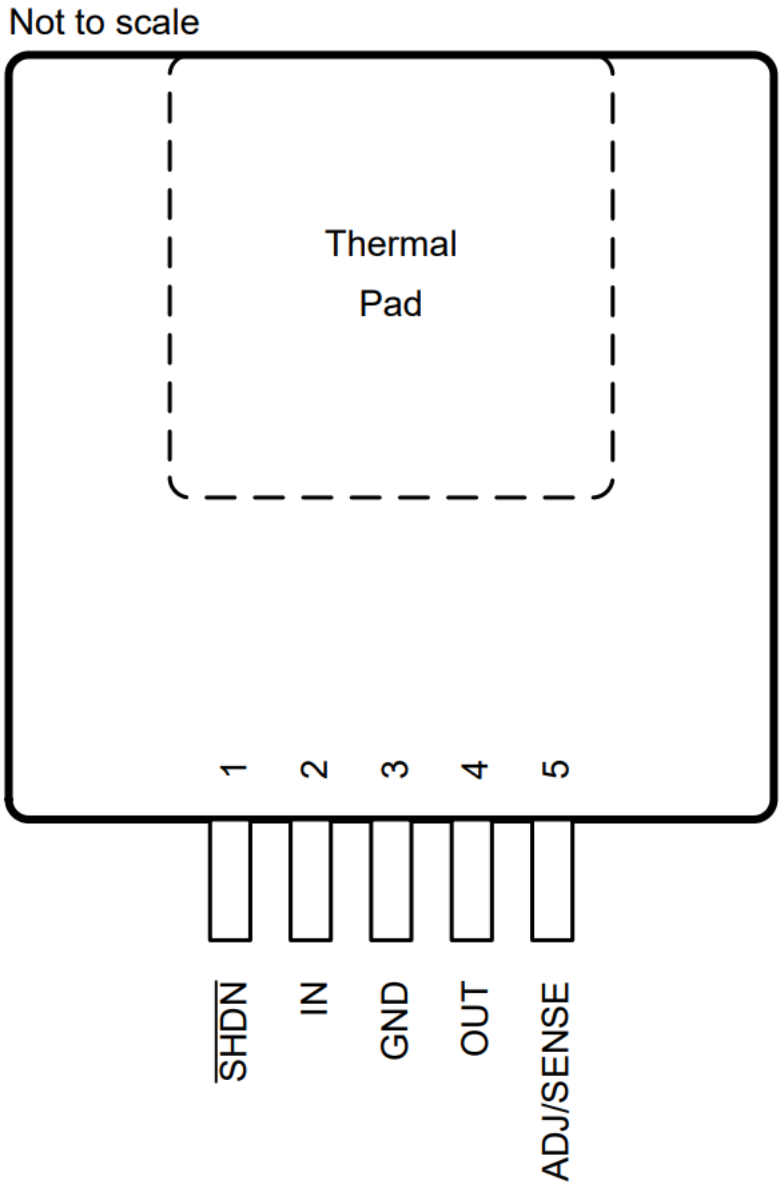

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{SHDN}}$	1	Output is off when pin is pulled low.	B
IN	2	No input to the device, potential damage to upstream supply.	B
GND	3	No effect.	D
OUT	4	Output voltage is at, or near, ground. The device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B
ADJ/SENSE	5	Input to device error amplifier is grounded, leading to output following input.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{SHDN}}$	1	The device is in the low-power shutdown state if left floating.	B
IN	2	There is no input to the device. Output is high impedance.	B
GND	3	There is no current loop for internal biasing and the device cannot function.	B
OUT	4	Load is disconnected from output.	B
ADJ/SENSE	5	Input to device error amplifier is floating, leading to an undesired output.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{SHDN}}$	1	IN	Device is left enabled. Shutdown functionality is lost and power sequencing for application is impacted.	C
IN	2	GND	There is no input to the device. Output is grounded. Potential damage to upstream supply.	B
GND	3	OUT	Output voltage is at, or near, ground. The device is in current limit. The device can cycle in and out of thermal shutdown depending on power dissipation.	B
OUT	4	ADJ/SENSE	ADJ - Output is set to reference voltage. SENSE - No effect.	B/D
ADJ/SENSE	5	$\overline{\text{SHDN}}$	Signal on the shutdown pin causes an undesirable output.	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265