Functional Safety Information

ISO7741Tx-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the ISO7741Tx-Q1 devices (ISO7741FTADWRQ1, ISO7741TADWRQ1, ISO7741FTBDWRQ1, and ISO7741TBDWRQ1) in the 16-DW SOIC to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

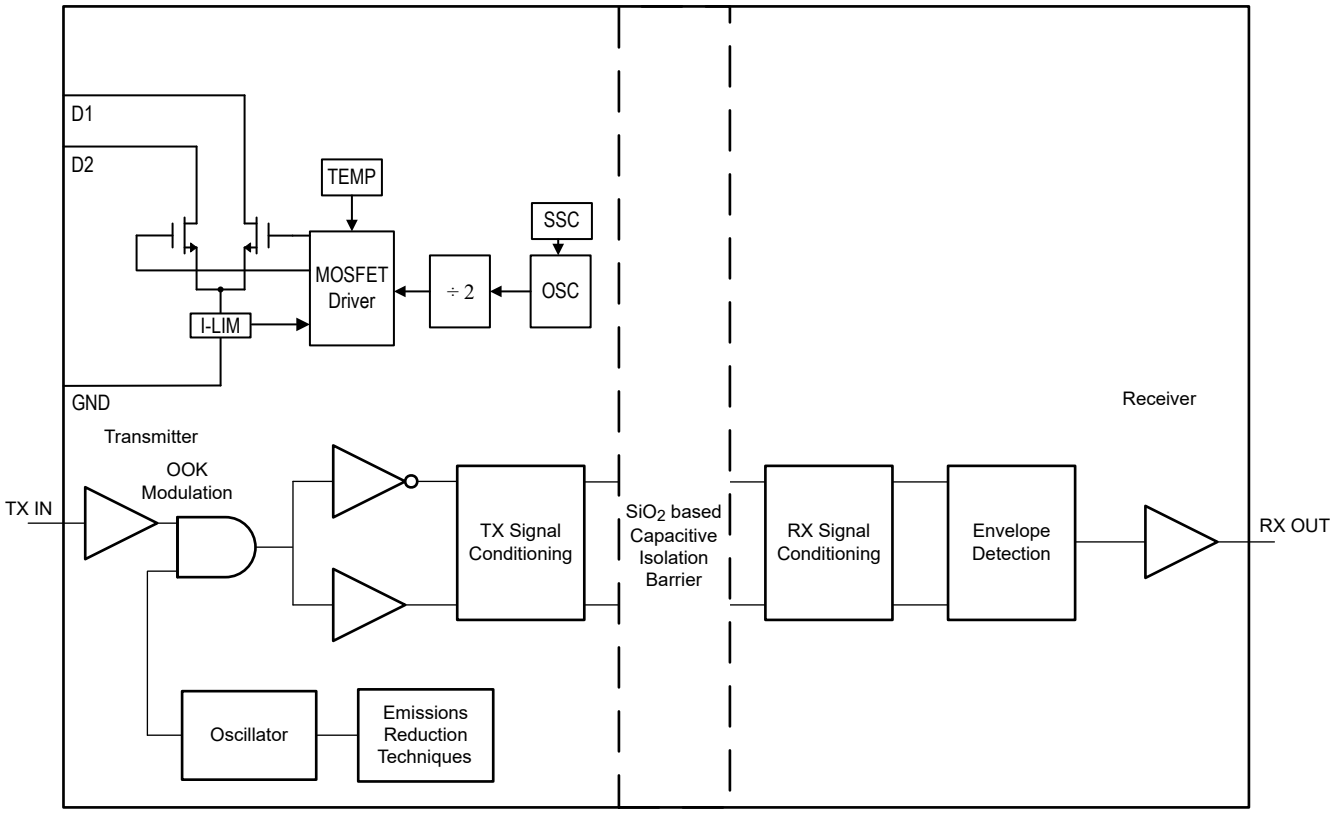

Figure 1-1. Functional Block Diagram

The ISO7741Tx-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 16-DW SOIC Package

This section provides functional safety failure in time (FIT) rates for the 16-DW SOIC package of the ISO7741Tx-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	30
Die FIT rate	4
Package FIT rate	26

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 401mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISO7741Tx-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
D1 FET, D2 FET, or both FETs stuck OFF	16
D1 FET, D2 FET, or both FETs stuck ON	12
D1 FET, D2 FET, or both FETs output not in timing or voltage specification	7
D1 FET, D2 FET or both FETs output undetermined	2
OUTx state undetermined	22
OUTx not in timing or voltage specification	19
OUTx stuck to default state	16
OUTx stuck high	3
OUTx stuck low	3

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO7741Tx-Q1 (16-DW SOIC). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The external transformer for the push-pull driver is connected with a winding between D1 and V_{CC1} and the second winding is connected between D2 and V_{CC1}.
- For short-to-ground analysis, the ground referenced for the short is the ground on that side of the isolation barrier.
- For short-to-supply analysis, the supply referenced for the short is the supply on that side of the isolation barrier.
- The default output state for OUTx outputs are high for ISO7741TADWRQ1 and ISO7741TBDWRQ1 and low for ISO7741FTADWRQ1 and ISO7741FTBDWRQ1.
- The switching frequency for the A, 160kHz, or B, 420kHz, versions of the ISO7741Tx-Q1 device does not impact the pinFMA.
- The signal drivers to any or all input channels, INx, do not have enough current sourcing capability to provide regular operating current of the device if the input signal current is conducted into the V_{CCx} supply of the device through an ESD diode on the INx pin if the V_{CCx} pin on the input pin side of the device is floating.

4.1 16-DW SOIC Package

Figure 4-1 shows the ISO7741Tx-Q1 pin diagram for the 16-DW SOIC package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISO7741Tx-Q1 data sheet.

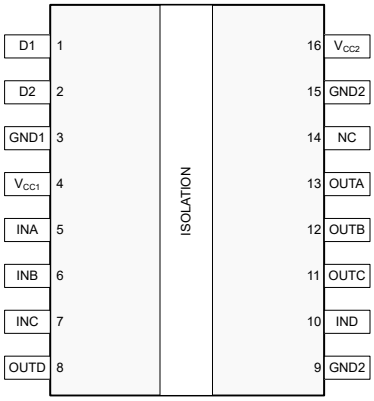

Figure 4-1. Pin Diagram (16-DW SOIC) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D1	1	D1 pin shorted to ground creates short circuit path between V_{CC1} and ground through transformer winding, causing high current to flow and possible damage to transformer or device. Output voltage out of target operating point.	A
D2	2	D2 pin shorted to ground creates short circuit path between V_{CC1} and ground through transformer winding, causing high current to flow and possible damage to transformer or device. Output voltage out of target operating point.	A
GND1	3	Device continues to function as expected. Normal operation.	D
V_{CC1}	4	No power to device side-1 (supply input shorted to ground). No switching action of D1/D2 and isolated output voltage does not build up. OUTA/OUTB/OUTC outputs are at default logic state. OUTD output state is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is possible.	A
INA	5	Input signal shorted to ground, so OUTA output is stuck low. Communication from INA to OUTA is corrupted.	B
INB	6	Input signal shorted to ground, so OUTB output is stuck low. Communication from INB to OUTB is corrupted.	B
INC	7	Input signal shorted to ground, so OUTC output is stuck low. Communication from INC to OUTC is corrupted.	B
OUTD	8	OUTD output shorted to ground. Data communication from IND to OUTD is corrupted. Device damage is possible if IND is driven high for an extended period of time.	A
GND2	9	Device continues to function as expected. Normal operation.	D
IND	10	Input signal shorted to ground, so OUTD output is stuck low. Communication from IND to OUTD is corrupted.	B
OUTC	11	OUTC output shorted to ground. Data communication from INC to OUTC is corrupted. Device damage is possible if INC is driven high for an extended period of time.	A
OUTB	12	OUTB output shorted to ground. Data communication from INB to OUTB is corrupted. Device damage is possible if INB is driven high for an extended period of time.	A
OUTA	13	OUTA output shorted to ground. Data communication from INA to OUTA is corrupted. Device damage is possible if INA is driven high for an extended period of time.	A
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	Device continues to function as expected. Normal operation.	D
V_{CC2}	16	No power to the device on side-2. State of OUTA/OUTB/OUTC outputs are undetermined. OUTD output is at default state.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D1	1	With D1 open, one primary transformer winding does not store energy. Output voltage out of target operating point.	B
D2	2	With D2 open, one primary transformer winding does not store energy. Output voltage out of target operating point.	B
GND1	3	No power to device side-1 (missing ground return). No switching action of D1/D2 and isolated output voltage does not build up. OUTA/OUTB/OUTC outputs are at default logic state. OUTD output is undetermined.	B
V_{CC1}	4	No power to device side-1 (supply is open). No switching action of D1/D2 and isolated output voltage does not build up. OUTA/OUTB/OUTC outputs are at default logic state. OUTD output is undetermined or through internal ESD diode on INA/INB/INC pin the device can power up if any IN is driven to logic high. If IN has current sourcing capability to provide regular operating current of device, ESD diode conducts that current and device damage is plausible.	B
INA	5	No communication to INA channel is possible. OUTA output at default state.	B
INB	6	No communication to INB channel is possible. OUTB output at default state.	B
INC	7	No communication to INC channel is possible. OUTC output at default state.	B
OUTD	8	State of OUTD output undetermined. Data communication from IND to OUTD is corrupted.	B
GND2	9	Device gets return ground through pin15. Normal operation.	D
IND	10	No communication to IND channel is possible. OUTD output at default state.	B
OUTC	11	State of OUTC output is undetermined. Data communication from INC to OUTC is corrupted.	B
OUTB	12	State of OUTB output is undetermined. Data communication from INB to OUTB is corrupted.	B
OUTA	13	State of OUTA output is undetermined. Data communication from INA to OUTA is corrupted.	B
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	Device gets return ground through pin 9. Normal operation.	D
V_{CC2}	16	No power to the device on side-2 (supply is open). State of OUTA/OUTB/OUTC outputs are undetermined. OUTD output at default state.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
D1	1	D2	With D1 shorted to D2, there is incorrect current flow in the primary transformer windings. Output voltage out of target operating point.	A
D2	2	GND	D2 pin shorted to ground creates short circuit path between V_{CC1} and ground through transformer winding, causing high current to flow and possible damage to transformer or device. Output voltage out of target operating point.	A
GND1	3	V_{CC1}	No power to device side-1 (supply input shorted to ground). No switching action of D1/D2 and isolated output voltage does not build up. OUTA/OUTB/OUTC outputs are at default logic state. OUTD output state is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is possible.	A
V_{CC1}	4	INA	Input signal shorted to supply, so OUTA output is stuck high. Communication from INA to OUTA is corrupted.	B
INA	5	INB	Communication corrupted for either or both channels.	B
INB	6	INC	Communication corrupted for either or both channels.	B
INC	7	OUTD	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTD	8	-	Not considered, corner pin.	-
GND2	9	IND	Input signal shorted to ground, so OUTD output is stuck low. Communication from IND to OUTD is corrupted.	B
IND	10	OUTC	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTC	11	OUTB	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTB	12	OUTA	Communication corrupted for either or both channels. With opposite logic state on both channels, high current can flow between supply and ground and cause possible device damage.	A
OUTA	13	NC	Device continues to function as expected. Normal operation.	D
NC	14	GND2	Device continues to function as expected. Normal operation.	D
GND2	15	V_{CC2}	No power to the device on side-2 (supply is shorted to ground). State of OUTA/OUTB/OUTC outputs are undetermined. OUTD output at default state.	B
V_{CC2}	16	-	Not considered corner pin.	-

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D1	1	D1 stuck high. Makes potential difference between one transformer winding zero. When D1 FET switches are on, high current flows from supply to ground and device damage is possible. Isolated output supply out of intended set-point.	A
D2	2	D2 stuck high. Makes potential difference between one transformer winding zero. When D2 FET switches on, high current flows from supply to ground and device damage is possible. Isolated output supply out of intended set-point.	A
GND1	3	No power to device side-1 (supply input shorted to ground). No switching action of D1/D2 and isolated output voltage does not build up. OUTA/OUTB/OUTC outputs are at default logic state. OUTD output state is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise device damage is possible.	A
V_{CC1}	4	No effect. Normal operation.	D
INA	5	Input signal shorted to supply, so OUTA output is stuck high. Communication from INA to OUTA is corrupted.	B
INB	6	Input signal shorted to supply, so OUTB output is stuck high. Communication from INB to OUTB is corrupted.	B
INC	7	Input signal shorted to supply, so OUTB output is stuck high. Communication from INB to OUTB is corrupted.	B
OUTD	8	OUTD stuck high. Data communication from INC to OUTC is lost. Device damage is possible if IND is driven low for an extended period of time.	A
GND2	9	Can create a potential difference between pin9 and pin15, causing high current to flow in the device and device damage is possible.	A
IND	10	Input signal shorted to supply, so OUTD output is stuck high. Communication from IND to OUTD is corrupted.	B
OUTC	11	OUTC shorted to supply (high). Communication from INC to OUTC is corrupted. If INC is low for extended duration, OUTC shorted to supply causes high current and can possibly damage the device.	A
OUTB	12	OUTB shorted to supply (high). Communication from INB to OUTB is corrupted. If INB is low for an extended duration, OUTB shorted to supply causes high current and can possibly damage the device.	A
OUTA	13	OUTA shorted to supply (high). Communication from INA to OUTA is corrupted. If INA is low for extended duration, OUTA shorted to supply causes high current and can possibly damage the device.	A
NC	14	Device continues to function as expected. Normal operation.	D
GND2	15	Shorting pin 15 to supply can create potential difference between pin9 and pin15, causing high current to flow in the device and device damage is possible.	A
V_{CC2}	16	Device continues to function as expected. Normal operation.	D

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