

UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
2.1 VSON-12 Package.....	3
3 Failure Mode Distribution (FMD)	4
4 Pin Failure Mode Analysis (Pin FMA)	5
4.1 VSON-12 Package.....	5
5 Revision History	7

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 (VSON-12 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

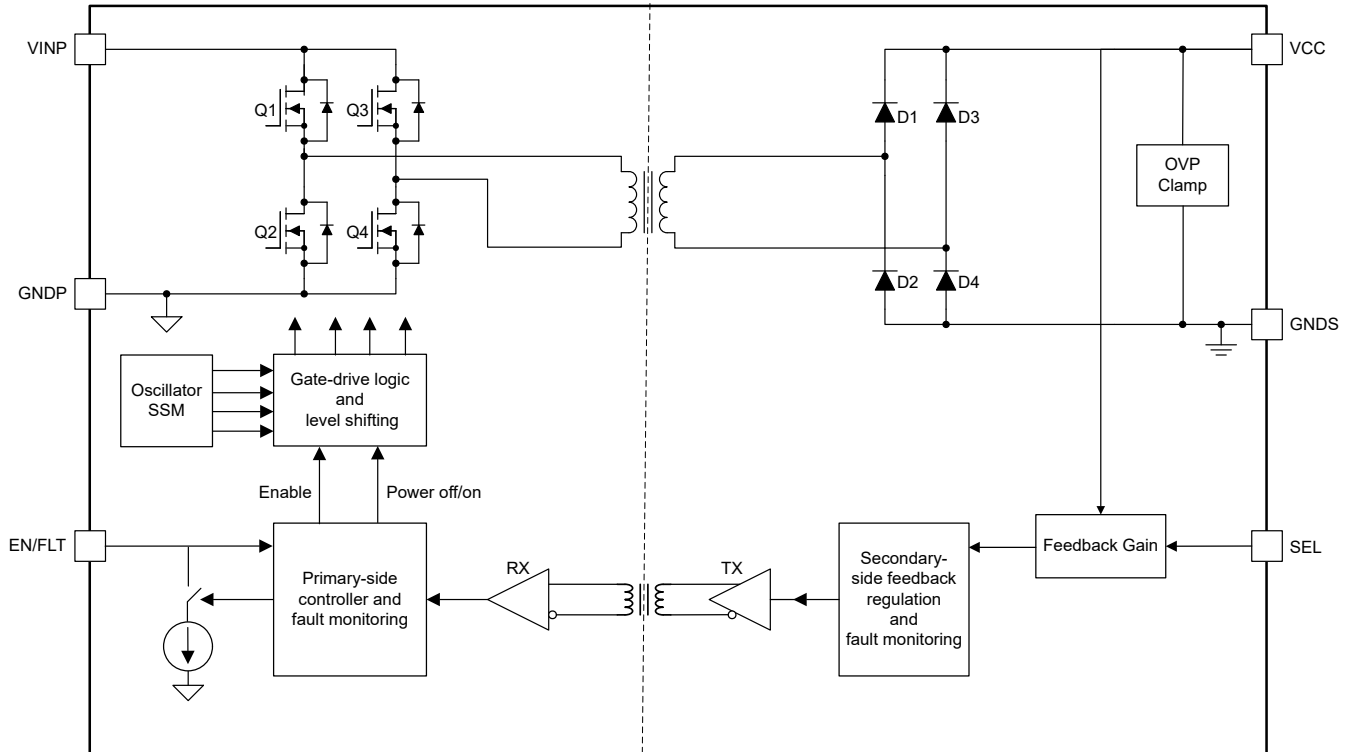


Figure 1-1. Functional Block Diagram

The UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON-12 Package

This section provides functional safety failure in time (FIT) rates for the VSON-12 package of UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	Power Dissipation	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	0.5W	13
	1W	18
	1.23W	20
Die FIT rate	0.5W	4
	1W	8
	1.23W	10
Package FIT rate	0.5W	9
	1W	10
	1.23W	10

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 0.5W, 1W, and 1.23W
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VCC has no power	38
VCC accuracy and ripple not meeting specifications	30
FAULT reporting not working	14
No effect	18

The FMD in [Table 3-1](#) excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 (VSON-12 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is configured according to the *Typical Application* in the *Application and Implementation* section of the data sheet
- VINP is considered the supply pin for primary-side pins
- GNDP is considered the ground for primary-side pins
- VCC is considered the supply pin for secondary-side pins
- GNDS is considered the ground for secondary-side pins
- Primary-side pins only short to primary-side pins. Secondary side-pins only short to secondary-side pins.

4.1 VSON-12 Package

[Figure 4-1](#) shows the UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 pin diagram for the VSON-12 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the UCC33420, UCC33420-Q1, UCC33020, and UCC33020-Q1 data sheets.

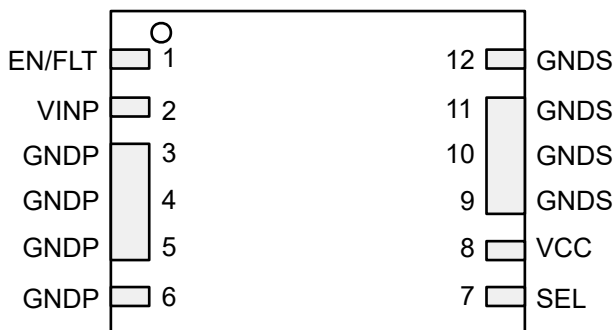


Figure 4-1. Pin Diagram (VSON-12) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	Device is disabled. No output.	B
VINP	2	Device has no input. No output.	B
GNDP	3	No effect. Normal operation.	D
GNDP	4	No effect. Normal operation.	D
GNDP	5	No effect. Normal operation.	D
GNDP	6	No effect. Normal operation.	D
SEL	7	Output is set to 5.5V.	C
VCC	8	Output is shorted. No output.	B
GNDS	9	No effect. Normal operation.	D
GNDS	10	No effect. Normal operation.	D
GNDS	11	No effect. Normal operation.	D
GNDS	12	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	EN/FLT is an undetermined state. Output can be random.	B
VINP	2	Device has no input. No output.	B
GNDP	3	No effect. Normal operation.	D
GNDP	4	No effect. Normal operation.	D
GNDP	5	No effect. Normal operation.	D
GNDP	6	No effect. Normal operation.	D
SEL	7	SEL pin is at an undetermined state. Output voltage can change between 5V and 5.5V randomly.	C
VCC	8	Output OVP is triggered. No output.	B
GNDS	9	No effect. Normal operation.	D
GNDS	10	No effect. Normal operation.	D
GNDS	11	No effect. Normal operation.	D
GNDS	12	No effect. Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	VINP	Device is always enabled and cannot be turned off.	C
VINP	2	GNDP	Device has no input. No output.	B
GNDP	3	GNDP	No effect. Normal operation.	D
GNDP	4	GNDP	No effect. Normal operation.	D
GNDP	5	GNDP	No effect. Normal operation.	D
GNDP	6	N/A	Not considered. Corner pin.	D
SEL	7	VCC	Output is set to 5V only.	C
VCC	8	GNDP	Output is shorted. No output.	B
GNDP	9	GNDP	No effect. Normal operation.	D
GNDP	10	GNDP	No effect. Normal operation.	D
GNDP	11	GNDP	No effect. Normal operation.	D
GNDP	12	N/A	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/FLT	1	Device is always enabled and cannot be turned off.	C
VINP	2	No effect. Normal operation.	D
GNDP	3	Device has no input. No output.	B
GNDP	4	Device has no input. No output.	B
GNDP	5	Device has no input. No output.	B
GNDP	6	Device has no input. No output.	B
SEL	7	Output is set to 5V only.	C
VCC	8	No effect. Normal operation.	D
GNDP	9	Output is shorted. No output.	B
GNDP	10	Output is shorted. No output.	B
GNDP	11	Output is shorted. No output.	B
GNDP	12	Output is shorted. No output.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated