Functional Safety Information

ISO6421
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ISO6421 (D-8 SOIC and DWV-8 Wide-SOIC packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

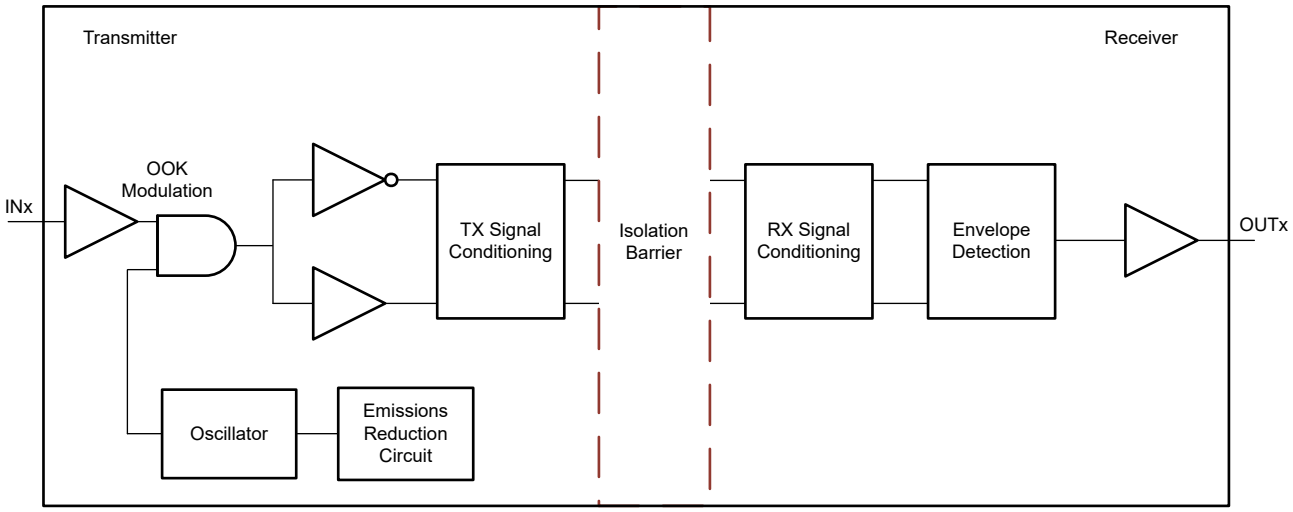

Figure 1-1. Functional Block Diagram

The ISO6421 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D-8 SOIC Package

This section provides functional safety failure in time (FIT) rates for the D-8 SOIC package of the ISO6421 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	3
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 142mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DWV-8 Wide-SOIC Package

This section provides functional safety failure in time (FIT) rates for the DWV-8 Wide-SOIC package of the ISO6421 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	3
Package FIT rate	15

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 142mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ISO6421 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx state is undetermined	23
OUTx is stuck to default state	41
OUTx is stuck to non-default state	10
OUTx is not in timing or voltage specification	10
OUTx is stuck high	8
OUTx is stuck low	8

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the ISO6421 (D-8 SOIC and DWV-8 Wide-SOIC packages). See the following sections for pin FMA by package. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to supply

The pin FMA by pinout (see following sections) indicates how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- For short-to-ground analysis, the ground referenced for the short is the ground on that side of the isolation barrier.
- For short-to-supply analysis, the supply referenced for the short is the supply on that side of the isolation barrier.
- The default output levels for the outputs of OUTx are:
  - High for: ISO6421
  - Low for: ISO6421F

4.1 D-8 SOIC and DWV-8 Wide-SOIC Packages

Figure 4-1 shows the ISO6421 pin diagram for the D-8 SOIC and DWV-8 Wide-SOIC packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the ISO6421 datasheet.

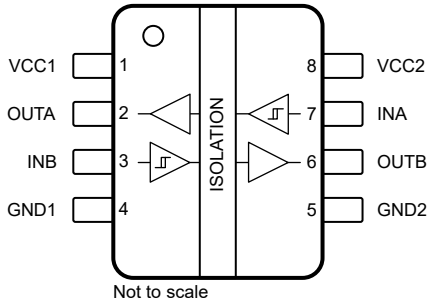

Figure 4-1. Pin Diagram (D-8 SOIC and DWV-8 Wide-SOIC Packages)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	Short-Circuited to Ground (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The output state of OUTA is undetermined. The output of OUTB is at the default logic state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
VCC1	1	Open-Circuited	The device has no power on side-1 (the supply input is open). The output state of OUTA is undetermined. The output of OUTB is at the default logic state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
VCC1	1	Short-Circuited to Pin2 (OUTA)	The output of OUTA is stuck high. Communication through channel A is corrupted. Device damage is possible if INA is driven low for an extended period of time.	A
VCC1	1	Short-Circuited to Supply (Side-1)	The device continues to function as expected. Normal operation.	D
OUTA	2	Short-Circuited to Ground (Side-1)	The output of OUTA is shorted to ground. Communication through channel A is corrupted. Damage to the device is possible if INA is driven high for an extended period of time.	A
OUTA	2	Open-Circuited	The output state of OUTA is undetermined. Communication through channel A is corrupted.	B
OUTA	2	Short-Circuited to Pin3 (INB)	Communication is corrupted for either channel or both channels. With opposite logic states on both channels, high current can flow between signals on INB, supply, and ground in OUTA, and potentially cause damage to the device.	A
OUTA	2	Short-Circuited to Supply (Side-1)	The output of OUTA is stuck high. Communication through channel A is corrupted. Device damage is possible if INA is driven low for an extended period of time.	A
INB	3	Short-Circuited to Ground (Side-1)	The input signal is shorted to ground, so the output of OUTB is stuck low. Communication through channel B is corrupted.	B
INB	3	Open-Circuited	Communication through channel B is not possible. The output of OUTB is at the default state (weak internal pullup or pulldown to the default state).	B
INB	3	Short-Circuited to Pin4 (GND1)	The input signal is shorted to ground, so the output of OUTB is stuck low. Communication through channel B is corrupted.	B
INB	3	Short-Circuited to Supply (Side-1)	The input signal is shorted to supply, so the output of OUTB is stuck high. Communication through channel B is corrupted.	B
GND1	4	Short-Circuited to Ground (Side-1)	The device continues to function as expected. Normal operation.	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
GND1	4	Open-Circuited	There is no power to the device on side-1 (ground is open). The output of OUTA is undetermined. The output of OUTB is at the default logic state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
GND1	4	Short-Circuited to Pin5 (N/A)	Not applicable (N/A), corner pin.	N/A
GND1	4	Short-Circuited to Supply (Side-1)	The device has no power on side-1 (the supply input is shorted to ground). The output of OUTB is at the default logic state. The output state of OUTA is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
GND2	5	Short-Circuited to Ground (Side-2)	The device continues to function as expected. Normal operation.	D
GND2	5	Open-Circuited	There is no power to the device on side-2 (ground is open). The output of OUTB is undetermined. The output of OUTA is at the default logic state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
GND2	5	Short-Circuited to Pin6 (OUTB)	The output of OUTB is shorted to ground. Communication through channel B is corrupted. Damage to the device is possible if INB is driven high for an extended period of time.	A
GND2	5	Short-Circuited to Supply (Side-2)	The device has no power on side-2 (the supply input is shorted to ground). The output of OUTB is undetermined. The output of OUTA is at the default logic state. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
OUTB	6	Short-Circuited to Ground (Side-2)	The output of OUTB is shorted to ground. Communication through channel B is corrupted. Damage to the device is possible if INB is driven high for an extended period of time.	A
OUTB	6	Open-Circuited	The output state of OUTB is undetermined. Communication through channel B is corrupted.	B
OUTB	6	Short-Circuited to Pin7 (INA)	Communication is corrupted for either channel or both channels. With opposite logic states on both channels, high current can flow between signals on INA, supply, and ground in OUTB, and potentially cause device damage.	A
OUTB	6	Short-Circuited to Supply (Side-2)	The output of OUTB is stuck high. Communication through channel B is corrupted. Device damage is possible if INB is driven low for an extended period of time.	A
INA	7	Short-Circuited to Ground (Side-2)	The input signal is shorted to ground, so the output of OUTA is stuck low. Communication from INA to OUTA is corrupted.	B
INA	7	Open-Circuited	Communication through channel A is not possible. The output of OUTA is at the default state (weak internal pullup or pulldown to the default state).	B
INA	7	Short-Circuited to Pin8 (VCC2)	The input signal is shorted to supply, so the output of OUTA is stuck high. Communication through channel A is corrupted.	B
INA	7	Short-Circuited to Supply (Side-2)	The input signal is shorted to supply, so the output of OUTA is stuck high. Communication through channel A is corrupted.	B
VCC2	8	Short-Circuited to Ground (Side-2)	No power to the device on side-2 (the supply input is shorted to ground). The output of OUTA is at the default logic state. The output state of OUTB is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A
VCC2	8	Open-Circuited	The device has no power on side-2 (the supply input is open). The output of OUTA is at the default logic state. The output state of OUTB is undetermined. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, device damage is possible.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground, Open-Circuited, Short-Circuited to Adjacent Pin, and Short-Circuited to Supply (continued)

Pin Name	Pin Number	Potential Failure Mode	Description of Potential Failure Effects	Failure Effect Class
VCC2	8	Short-Circuited to Pin1 (N/A)	Not applicable (N/A), corner pin.	N/A
VCC2	8	Short-Circuited to Supply (Side-2)	The device continues to function as expected. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

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