Functional Safety Information

SN74CBTLV3245A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for SN74CBTLV3245A-Q1 (TSSOP (20), VSSOP (20), and VQFN (20) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

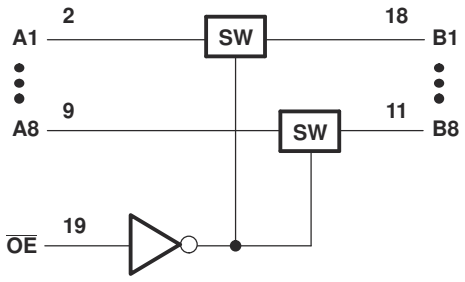

Figure 1-1. Functional Block Diagram

SN74CBTLV3245A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TSSOP (20), VSSOP (20), and VQFN (20) packages of the SN74CBTLV3245A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)	
	TSSOP (20) | VSSOP (20)	VQFN (20)
Total component FIT rate	13	12
Die FIT rate	5	5
Package FIT rate	8	7

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 100mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, analog, mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74CBTLV3245A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Switch channel stuck on	5
Switch channel stuck off	5
Switch functional out of specification leakage	45
Switch out of specification voltage or timing	45

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74CBTLV3245A-Q1 (TSSOP (20), VSSOP (20), and VQFN (20) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx.
  Series resistors are sized to limit the input currents into the analog inputs to <10mA in all circumstances, for example, in cases where the device is not powered and an input signal is applied.
- The device is the only target on the SPI bus.

4.1 TSSOP (20), VSSOP (20), and VQFN (20) Packages

Figure 4-1 and Figure 4-2 shows the SN74CBTLV3245A-Q1 pin diagram for the TSSOP (20), VSSOP (20), and VQFN (20) packages. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN74CBTLV3245A-Q1 datasheet.

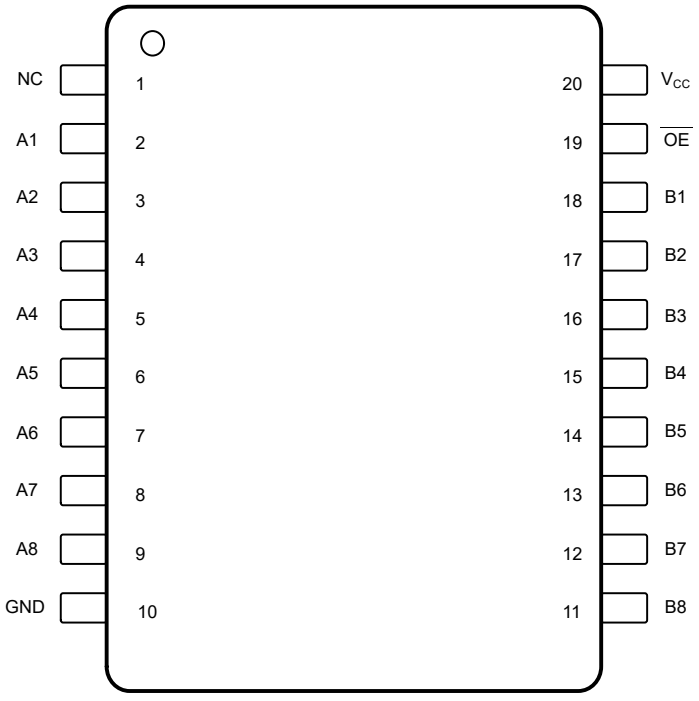

Figure 4-1. Pin Diagram (DGS, and PW Package 20-Pin VSSOP, and TSSOP Packages)

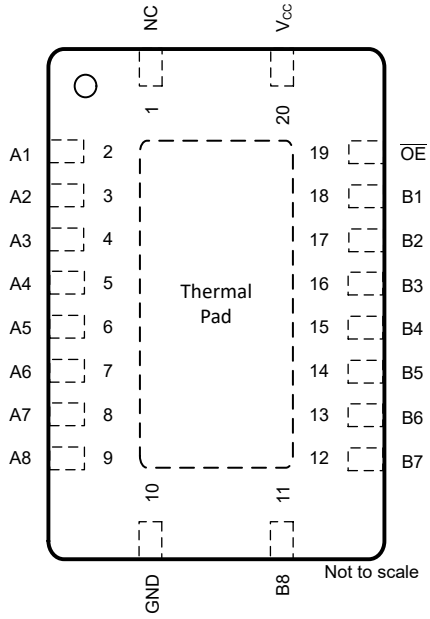

Figure 4-2. Pin Diagram (RKS Package 20-Pin VQFN Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect to the device. The pin is not connected.	D
A1	2	There is corruption of the signal passed on to the B1 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A2	3	There is corruption of the signal passed on to the B2 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A3	4	There is corruption of the signal passed on to the B3 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A4	5	There is corruption of the signal passed on to the B4 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A5	6	There is corruption of the signal passed on to the B5 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A6	7	There is corruption of the signal passed on to the B6 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A7	8	There is corruption of the signal passed on to the B7 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
A8	9	There is corruption of the signal passed on to the B8 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
GND	10	There is no effect to the device. The device operates normally.	D
B8	11	There is corruption of the signal passed on to the A8 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
B7	12	There is corruption of the signal passed on to the A7 pins. If there is no limiting resistor in the switch path, damage to the device is possible.	A
B6	13	There is corruption of the signal passed on to the A6 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
B5	14	There is corruption of the signal passed on to the A5 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
B4	15	There is corruption of the signal passed on to the A4 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	B
B3	16	There is corruption of the signal passed on to the A3 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
B2	17	There is corruption of the signal passed on to the A2 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
B1	18	There is corruption of the signal passed on to the A1 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
/OE	19	The /OE pin is stuck low. The pin can no longer disable the device without powering down.	B
VCC	20	The device is not powered. The device not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect to the device. The pin is not connected.	D
A1	2	There is corruption of the signal passed on to the B pin.	B
A2	3	There is corruption of the signal passed on to the B pin.	B
A3	4	There is corruption of the signal passed on to the B pin.	B
A4	5	There is corruption of the signal passed on to the B pin.	B
A5	6	There is corruption of the signal passed on to the B pin.	B
A6	7	There is corruption of the signal passed on to the B pin.	B
A7	8	There is corruption of the signal passed on to the B pin.	B
A8	9	There is corruption of the signal passed on to the B pin.	B
GND	10	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
B8	11	There is corruption of the signal passed on to the A pin.	B
B7	12	There is corruption of the signal passed on to the A pin.	B
B6	13	There is corruption of the signal passed on to the A pin.	B
B5	14	There is corruption of the signal passed on to the A pin.	B
B4	15	There is corruption of the signal passed on to the A pin.	B
B3	16	There is corruption of the signal passed on to the A pin.	B
B2	17	There is corruption of the signal passed on to the A pin.	B
B1	18	There is corruption of the signal passed on to the A pin.	B
/OE	19	Control of the /OE pin is lost. The pin cannot disable switch. The pin defaults to switches disabled.	B
VCC	20	The device is not powered. The device is not functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	1	A1	The no connect pin is electrically floating. There is no effect to the device.	D
A1	2	A2	Corruption of the signal passed on to the B1 pin is possible.	B
A2	3	A3	Corruption of the signal passed on to the B2 pin is possible.	B
A3	4	A4	Corruption of the signal passed on to the B3 pin is possible.	B
A4	5	A5	Corruption of the signal passed on to the B4 pin is possible.	B
A5	6	A6	Corruption of the signal passed on to the B5 pin is possible.	B
A6	7	A7	Corruption of the signal passed on to the B6 pin is possible.	B
A7	8	A8	Corruption of the signal passed on to the B7 pin is possible.	B
A8	9	GND	There is corruption of the signal passed on to the B8 pin. If there is no limiting resistor in the switch path, damage to the device is possible.	A
GND	10	B8	This pin is not considered. This is a corner pin.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
B8	11	B7	Corruption of the signal passed on to the A8 pin is possible.	B
B7	12	B6	Corruption of the signal passed on to the A7 pin is possible.	B
B6	13	B5	Corruption of the signal passed on to the A6 pin is possible.	B
B5	14	B4	Corruption of the signal passed on to the A5 pin is possible.	B
B4	15	B3	Corruption of the signal passed on to the A4 pin is possible.	B
B3	16	B2	Corruption of the signal passed on to the A3 pin is possible.	B
B2	17	B1	Corruption of the signal passed on to the A2 pin is possible.	B
B1	18	/OE	Corruption of the signal passed on to the A1 pin is possible. The switch state is undefined.	A
/OE	19	VCC	The /OE pin is stuck high. The pin can no longer enable the device.	B
VCC	20	NC	The no connect pin is electrically floating. There is no effect to the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
NC	1	There is no effect to the device. This pin is not connected.	D
A1	2	There is corruption of the signal passed on to the B1 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A2	3	There is corruption of the signal passed on to the B2 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A3	4	There is corruption of the signal passed on to the B3 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A4	5	There is corruption of the signal passed on to the B4 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A5	6	There is corruption of the signal passed on to the B5 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A6	7	There is corruption of the signal passed on to the B6 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A7	8	There is corruption of the signal passed on to the B7 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
A8	9	There is corruption of the signal passed on to the B8 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
GND	10	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
B8	11	There is corruption of the signal passed on to the A8 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B7	12	There is corruption of the signal passed on to the A7 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B6	13	There is corruption of the signal passed on to the A6 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B5	14	There is corruption of the signal passed on to the A5 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B4	15	There is corruption of the signal passed on to the A4 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B3	16	There is corruption of the signal passed on to the A3 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B2	17	There is corruption of the signal passed on to the A2 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
B1	18	There is corruption of the signal passed on to the A1 pin. If there is no limiting resistor in the switch path, then damage to the device is possible.	A
/OE	19	The /EN pin is stuck high. The pin can no longer enable the device.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	20	There is no effect to the device. The device operates normally.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

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