TEXAS INSTRUMENTS

DAC8541EVM

User's Guide

August 2002 *Data Acquisition*

SLAU085A

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the DAC8541 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

Chapter 1—EVM Overview

Chapter 2—Physical Description

Chapter 3—EVM Operation

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Data Sheets:	**Literature Number**:
DAC8541	SLAS353
REF02	SBVS003A
OPA627	PDS-998H

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Chapter 1

EVM Overview

This chapter gives a general overview of the DAC8541EVM and describes some of the factors that must be considered in using this module.

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1.1 Features

This EVM features the DAC8541 digital-to-analog converter. The DAC8541EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality of the high resolution, single-channel, parallel input DAC. This EVM features a parallel interface to communicate to any host processor base system.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply range for the digital section of this EVM is from 1.8 V to 5.5 V connected to the J8-2 or J7-2 terminal and is referenced to ground through the J8-1 or J7-1 terminal. The dc power requirements for the analog section of this EVM range from 2.7 V to 5.5 V and connect through J9-6 or J6-4 terminal and are referenced to ground through the J9-5 or J6-2 terminal.

A dc source of ±15 V supply is required to provide the rails for the external output op-amp provided for output signal conditioning, boost capacitive load drive, or DAC bipolar mode operation. The 15-V supply connects through the J6-1 or J9-2 terminal, and the -15 V supply connects through the J6-3 or J9-4 terminal. The ±15-V supply is referenced to ground through the J6-2 or J9-3 terminal.

Caution

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

1.2.2 Reference Voltage

A 5-V precision reference voltage is provided to supply the $V_{REF(H)}$ through REF02, U3, via jumper W2 by shorting pins 1 and 2. An adjustable 100 kΩ potentiometer, R5, is installed in series with 20 kΩ, R4, to allow the user to adjust the reference voltage to its desired settings. TP2 and TP3 are provided as well as J4-20, to allow the user to connect an external reference source not to exceed 5 V dc.

The REF02 precision reference derives its power of ±15 V supply through J6 or J9 terminal. The 15 V connects through the J6-1 or J9-2 terminal, while the -15 V connects through the J6-3 or J9-4 terminal. They are both referenced to ground through the J6-2 or J9-1.

The $V_{REF(L)}$ input is normally tied to AGND, unless some minor adjustment to the offset of the DAC is needed.

Caution

When applying an external voltage reference through TP2 or J4-20, make sure that it does not exceed 5 V maximum. Otherwise, this damages U1 part, DUT.

1.3 EVM Basic Functions

The DAC8541EVM is a functional evaluation platform to test certain functional characteristics of the DAC8541 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, DSP, or some sort of a waveform generator.

The 20-pin headers, J1, J2, and J3, are provided to channel in the necessary control signals and data needed to interface a microprocessor/microcontroller, TI's DSP starter kit, or waveform generator to the DAC8541 EVM, through a custom cable.

A specific adapter card is also available for most of TI's DSP starter kit. Make sure to specify the DSP that is used to interface with the right adapter card. Call or email TI for more information regarding the adapter card.

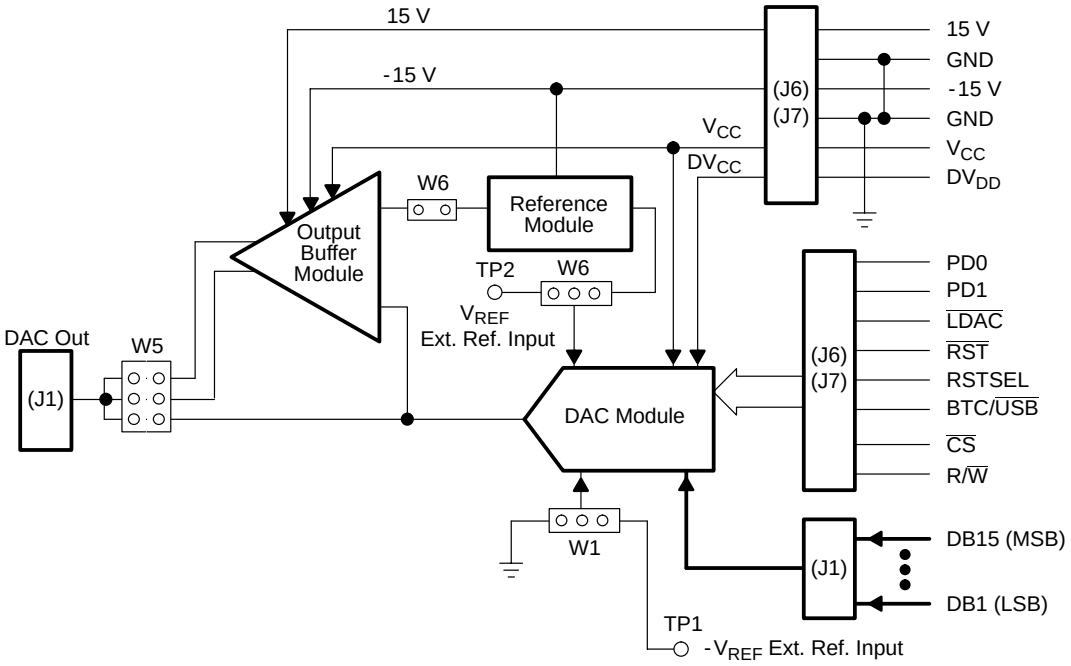
A precision reference voltage provided onboard, can be adjusted to the user's preference through the R5 potentiometer. This sets the effective range of the DAC's output signal.

The output of the DAC can be monitored through two different access points which are as follows: a BNC connector (J5, if installed), and a header through pin 2 of J4. The 6-pin header, W5, provides different levels of the DAC output, but requires the output op-amp, U2, to be configured correctly first for the desired waveform characteristic. Shorting pins 1 and 2 of W5 allows the user to monitor the raw output of the DAC.

A bipolar mode of operation is integrated into the EVM board through the output op-amp, U2. This option to operate in bipolar mode yields a rail-to-rail output voltage range of 5 V maximum. This is the default configuration mode of the EVM when it ships from the factory.

A block diagram of the EVM is shown in Figure 1-1.

Figure 1-1. DAC8541EVM Block Diagram



Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The DAC8541EVM is constructed on two-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 99,06 mm (3.90 inch) × 104, 14 mm (4.10 inch), and the board thickness is 1,57 mm (0.062 inch). Figures 2-2 through 2-4 show the individual artwork layers.

Figure 2-1. Layer One (Top Silkscreen)

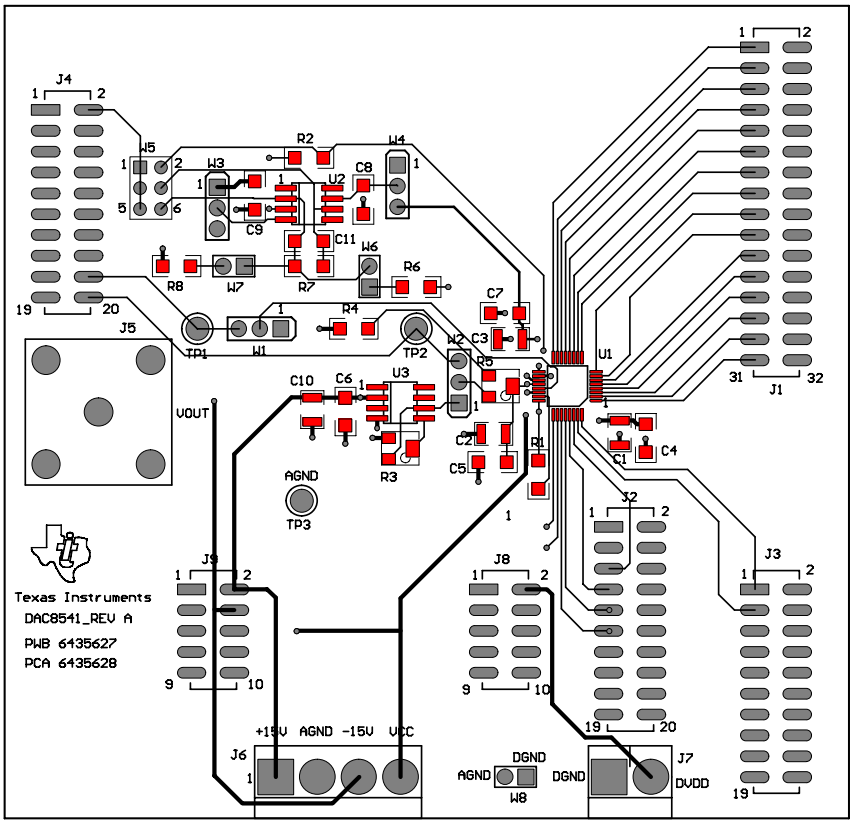


Figure 2-2. Layer Two (Bottom Layer)

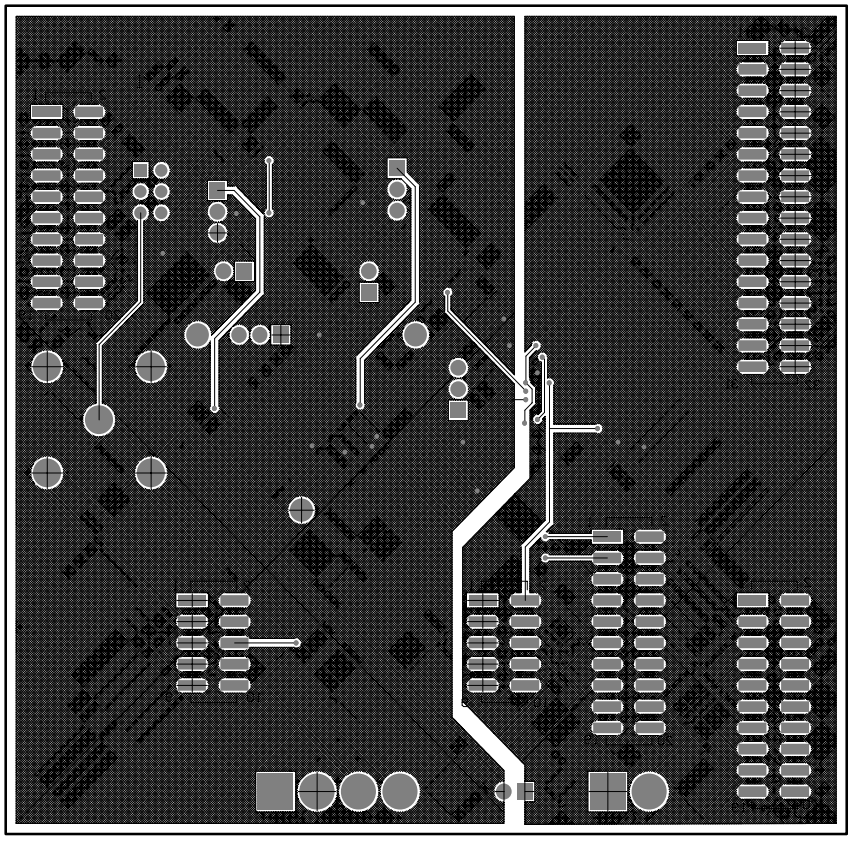
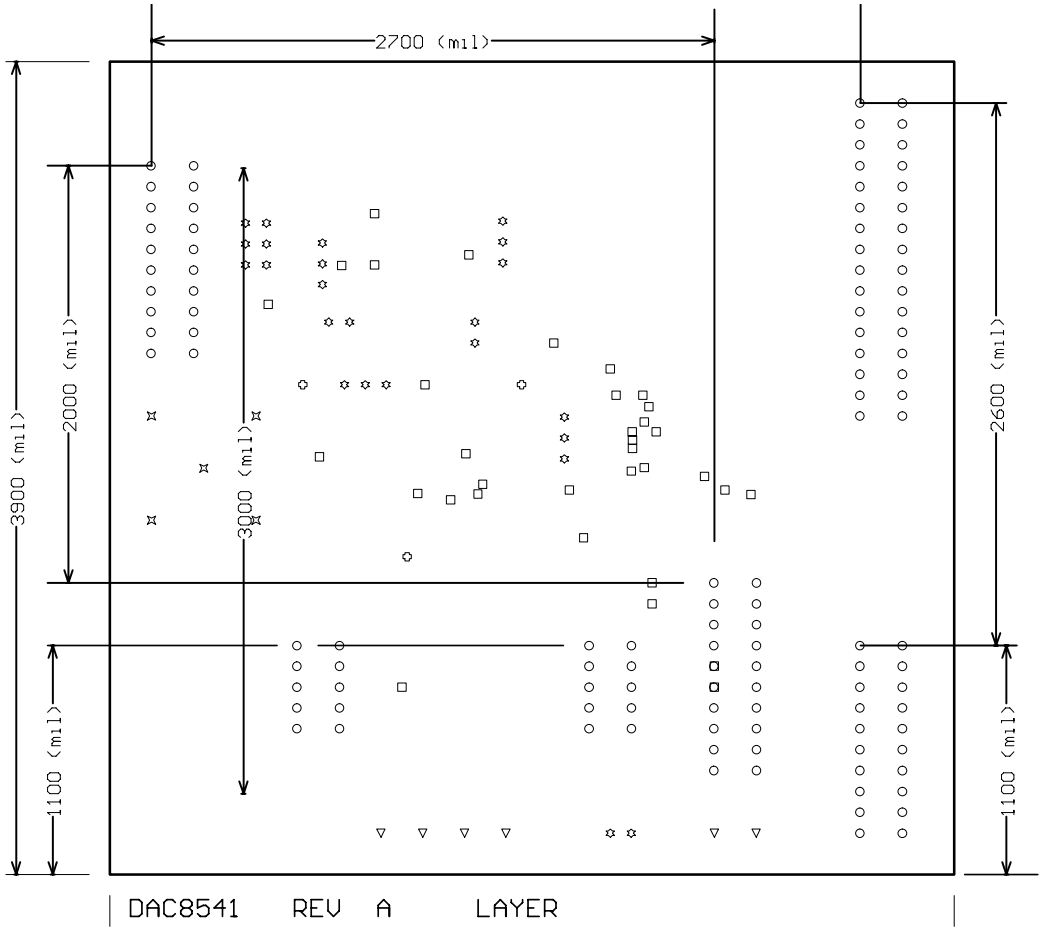


Figure 2-3. Drill Drawing



2.2 Bill of Materials

Table 2-1. Parts Lists

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	1	R2	Panasonic	ERJ-8GEY0R00V	0 Ω, 1/4 W, 1206 chip resistor
2	2	C8, C9	Panasonic	ECUV1H103KBM	0.01 μF, 1206 multilayer ceramic capacitor
3	4	C4, C5, C6, C7	Panasonic	ECJ3VB1C104K	0.01 μF, 1206 multilayer ceramic capacitor
4	1	C11	Panasonic	ECUV1H102JCH	1 nF, 1206 multilayer ceramic capacitor
5	3	W6, W7, W8	Samtec	TSW-102-07-L-S	2 position jumper_0.1 ” spacing
6	4	W1, W2, W3, W4	Samtec	TSW-103-07-L-S	3 position jumper_0.1 ” spacing
7	2	J8, J9	Samtec	IPT1-105-01-S-D-VS	5X2X0.1 10-pin 3A isolated power header
8	3	R6, R7, R8	Panasonic	ERJ-8ENF1002V	10 kΩ, 1/4 W 1206 chip resistor
9	1	R3	Bourns	3214W-103E	10 kΩ, BOURNS_32X4W series 5T Pot
10	4	C1, C2, C3, C10	Kemet	C1210C106K8PAC	10 μF, 1206 multilayer ceramic X5R capacitor
11	1	R4	Panasonic	ERJ-8ENF2002V	20 kΩ, 1/4 W 1206 chip resistor
12	3	J2, J3, J4	Samtec	TSM-110-01-S-DV-M	10X2X0.1 20-pin 0.025”” sq SMT terminal strips
13	1	J1	Samtec	TSM-116-01-S-DV-M	16X2X0.1 32-pin 0.025”” sq SMT terminal strips
14	1	R1	Panasonic	ERJ-8GEYJ330V	33 Ω, 1/4 W, 1206 chip resistor
15	1	R5	Bourns	3214W-104E	100 kΩ, BOURNS_32X4W series 5T Pot
16	1	J5 (see Note)	AMP (Tyco)	227699-2	PCB mounted BNC—amphenol
17	1	U1	Texas Instruments	DAC8541	16-bit, 32-TQFP DAC
18	1	J7	Lumberg	KRMZ2	2-pin terminal screw connector
19	1	J6	Lumberg	KRMZ4	4-pin terminal screw connector
20	1	U2	Texas Instruments	OPA627AU	8-SOP (D) precision op amp
21	1	U3	Texas Instruments	REF02AU	5 V, 8-SOP (D) precision voltage reference
22	3	TP1, TP2, TP3	Cambion	180-7337-02-05	Turret terminal test point
23	1	W5	Samtec	TSW-103-07-L-D	3X2X0.1 6-pin IDC header
24	3	P2, P3, P4 (see Note)	Samtec	SSW-110-22-S-D-VS-P	20 pin 0.025”” sq SMT socket
25	1	P1 (see Note)	Samtec	SSW-116-22-S-D-VS-P	32 pin 0.025”” sq SMT socket
26	2	P8, P9 (see Note)	Samtec	IPS1-105-01-S-D-VS	3A isolated power socket

Note: P1, P2, P3, P4, P8, and P9 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC board opposite the J designated counterpart. Example, J1 is installed on the topside while P1 is installed in the bottom side opposite of J1.
J5 is an optional output terminal and is not installed.

Chapter 3

EVM Operation

This chapter covers the operation of the DAC8541EVM and provides guidance to the user in evaluating the onboard DAC and interfacing the EVM to a specific host processor.

For information about its parallel interface and other related topics, refer to the DAC8541 data sheet, TI literature number SLAS353.

The EVM board is factory-tested and configured to operate in the bipolar output mode.

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3.2 Host Processor Operation 3-2

3.3 Jumper Setting Reference 3-6

3.1 Factory Default Setting

The EVM board is set as default from the factory to the configuration below to operate in bipolar mode through U2.

Table 3-1. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	$V_{REF(L)}$ tied to AGND
W2	1-2	Adjustable onboard $V_{REF(H)}$ is supplied by U3.
W3	1-2	Negative supply rail of U2 is tied to -15 V.
W4	1-2	Positive supply rail of U2 is tied to 15 V.
W5	3-4	DAC output signal is directed to J5 and J4-2 output terminals.
W6	Close	Midscale for bipolar operation is set to $V_{REF(H)}$.
W7	Open	U2 is set for 2x gain for bipolar mode of operation.
W8	Close	AGND and DGND are tied together.

3.2 Host Processor Operation

The host processor drives the DAC, so the DAC's proper operation depends on the successful configuration between the host processor and the EVM board, and of course a properly written code to run the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 and J3 header connectors for control signals, and J1 header connector for the data input. The output can be monitored through the J5 BNC connector (if installed) or J4 header connector. An interface adapter card is also available for specific DSP starter kits as mentioned in Chapter 1.

The EVM incorporates four different options for the DAC output through an external operational amplifier, U2. This requires some jumper setting configuration, particularly around the op-amp (U2) circuitry, and other required equipment. Each option is discussed individually.

The raw output of the DAC can be probed through W5 pin 2 so that it can be compared with the output of U2 if necessary. The output terminals J5 and J4-2 can be used to monitor the raw output of the DAC by shorting pins 1 and 2 of W5.

3.2.1 Unity Gain Output

The buffered output should closely match the raw output of the DAC with some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by desoldering R7 and C11 and replacing it with the desired values. You can also simply get rid of R7 and C11 altogether and just solder a 0 Ω resistor in replacement of R7, if desired.

Table 3-2 shows the jumper setting relating to the unity gain configuration of the output buffer.

Table 3-2. Unity Gain Output Jumper Settings

Reference	Jumper Position	Function
W3	2-3	Negative rail of the op amp tied to analog GND
W4	Don't care	Positive rail of the op amp can be supplied by 15 V or V_{CC}
W5	3-4	Buffered output of DAC is channeled to the output terminals
W6	Open	Disconnect $V_{REF(H)}$ from negative input of op amp
W7	Open	Disconnect negative input of op amp from GND

3.2.2 Output Gain of Two

This configuration allows the output of the DAC to have a gain of two which is particularly useful when the EVM is operating at 3.3 V and there is a need for the DAC output to maintain a 5 V peak level. The output gain of two configuration that can be implemented on this EVM should not exceed the effective range of $2 \times V_{REF(H)}$.

The reference voltage must be set such that the output voltage range of the DAC does not exceed the positive rail supply of the op amp, U2, as well. Otherwise the output of the op amp, U2, is clipped.

V_{CC} can be used also to supply the positive rail of the op amp by shorting pins 1 and 2 of W4. With this configuration, the effective output of the op amp is at a maximum of V_{CC}. The reference voltage must also be set to $V_{CC}/2$. Table 3-3 shows the proper jumper settings for the 2× gain output of the DAC.

Table 3-3. Gain of Two Output Jumper Settings

Reference	Jumper Position	Function
W3	2-3	Negative rail of the op amp tied to analog GND
W4	1-2	Positive rail supply of the op amp tied to 15 V
W5	3-4	Amplifier output of DAC is channeled to the output terminals
W6	Open	Disconnect $V_{REF(H)}$ from negative input of op amp
W7	Close	Configures op amp for a 2× gain output

3.2.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirements. However, all op-amps under certain conditions may become unstable depending on the op-amp configuration, gain, and load value. These are just a few factors that can affect op-amps stability performance that should be considered when implementing.

In unity gain, the OPA627 op amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor would even improve the capacitive load drive capability.

Table 3-4 shows the jumper setting configuration for a capacitive load drive.

Table 3-4. Capacitive Load Drive Output Jumper Settings

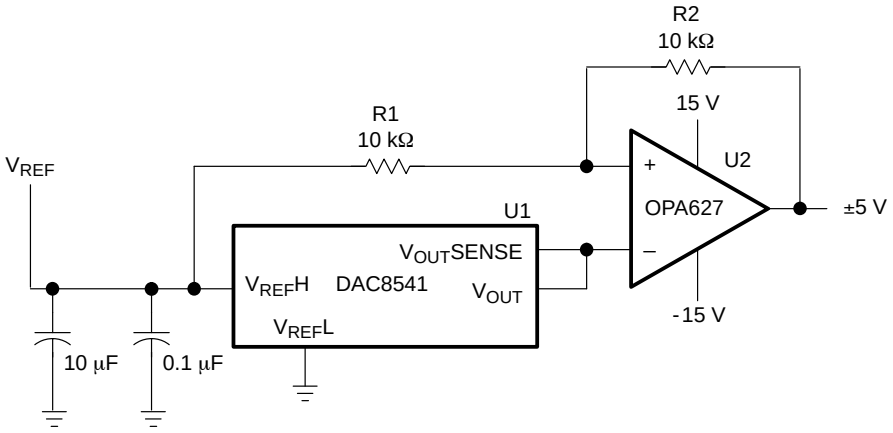
Reference	Jumper Position	Function
W3	2-3	Negative rail of the op amp tied to analog GND
W4	1-2	Positive rail supply of the op amp tied to 15 V
W5	3-4	Capacitive load drive output of DAC is channeled to the output terminals
W6	Open	Disconnect $V_{REF(H)}$ from negative input of op amp
W7	Open	Disconnect R8 (see Note)

Note: If there is a need to incrementally adjust the capacitive load output, replace R8 with a capacitor with the desired capacitance value and CLOSE W7.

3.2.4 Bipolar Operation Using the DAC8541 (Default Mode)

Although the DAC8541 is designed for single-supply operation, the bipolar output of operation is implemented using the circuit shown in Figure 3-1. The output of the circuit gives an output voltage range of $\pm V_{REF(H)}$. The rail-to-rail operation at the amplifier output is achievable using an OPA627 as the output amplifier.

Figure 3-1. Bipolar Operation With the DAC8541



The bipolar configuration is accomplished by following the correct jumper settings according to Table 3-5.

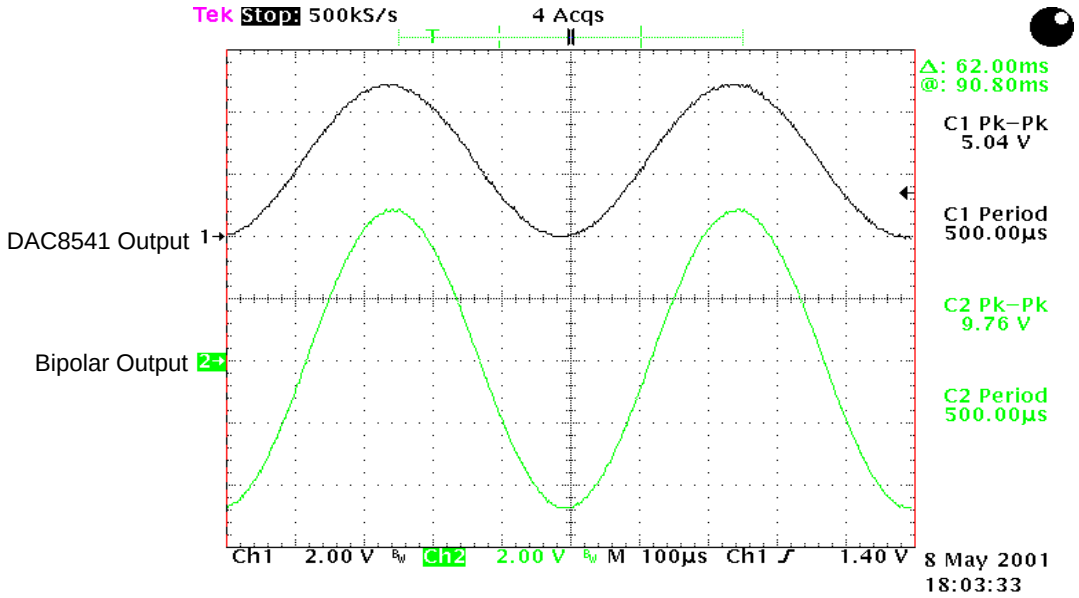
Table 3-5. Bipolar Operation Output Jumper Settings

Reference	Jumper Position	Function
W3	1-2	Negative rail supply of the op amp tied to -15 V
W4	1-2	Positive rail supply of the op amp tied to 15 V
W5	Close	Bipolar output of DAC is channeled to the output terminals
W6	Close	Connect $V_{REF(H)}$ to the negative input of op amp for negative biasing
W7	Open	Disconnect R8

An example in Figure 3-2 shows the sinusoidal signal in channel 1 being amplified within the range of $\pm V_{REF(H)}$ shown in channel 2. The reference voltage, $V_{REF(H)}$, is set to 5 V, which is then supplied to the negative input of U2 to bias the circuit to its negative rail. This provides an output of ±5 V with

0000h corresponding to a -5 V output and FFFFh corresponding to a 5 V output when BTC/$\overline{USB}$ = 0. If BTC/$\overline{USB}$ = 1, 8000h corresponds to -5 V output and 7FFFh corresponds to 5 V output. Bipolar zero is given by the code 0000h applied to the DAC.

Figure 3-2. DAC8541 Bipolar Output of Operation

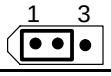
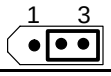
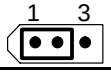
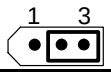
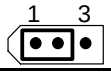
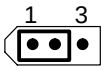
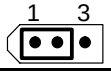
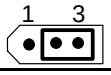
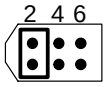
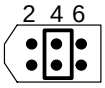
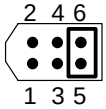


Similarly, adjusting the $V_{REF(H)}$ voltage to any desired value less than 5 V produces a voltage output range of $\pm V_{REF(H)}$.

3.3 Jumper Setting Reference

The illustrations in Table 3-6 shows the function of each jumper on the DAC8541EVM.

Table 3-6. Jumper Setting Function

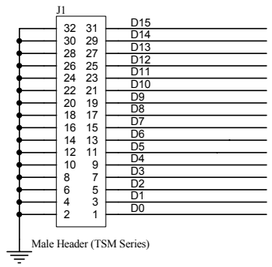
Reference	Jumper Setting	Function
W1		$V_{REF(L)}$ tied to AGND
		Enables $V_{REF(L)}$ to be supplied by an external source of reference voltage through TP1
W2		Enables the onboard adjustable reference to supply voltage for $V_{REF(H)}$
		Enables $V_{REF(H)}$ to be supplied by an external source of reference voltage through TP2
W3		Negative supply rail of op amp, U2, is -15 V for bipolar application
		Negative supply rail of op amp, U2, is tied to AGND for unipolar application
W4		Positive supply rail of op amp, U2, is 15 V.
		Positive supply rail of op amp, U2, is V_{CC}.
W5		Routes the raw output of the DAC8531 to J4-2 and J5 output terminals
		Routes the output of U2 to J4-2 and 51 output terminals. Used for unipolar and bipolar modes of operation.
		Routes the output of U2 to J4-2 and J5 output terminals. Used for capacitive load driving.
W6		Disconnects $V_{REF(H)}$ from the negative input terminal of U2
		Allows $V_{REF(H)}$ to be routed to the negative input terminal of U2 for bipolar operation
W7		Disconnects the negative terminal of U2 to AGND and disables 2× gain
		Configures U2 for a 2× gain output in unipolar mode
W8		Separate AGND and DGND from EVM board
		Connect AGND and DGND of EVM board

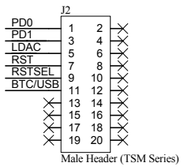
Legend:  Indicates the corresponding pins that are shorted or closed.

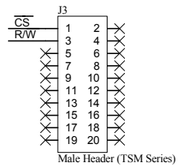
3.4 Schematic Diagram

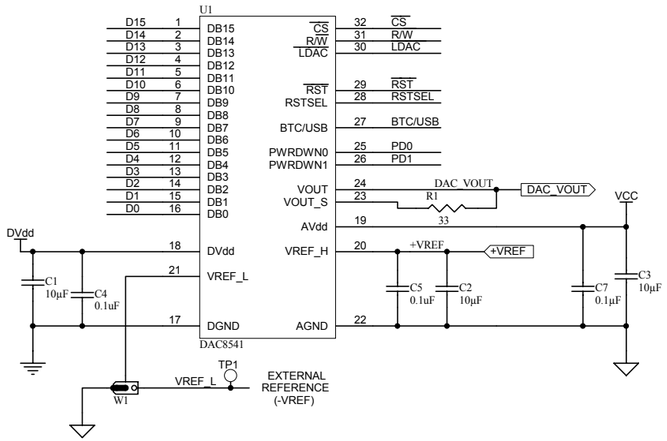
This section contains the schematic diagram for the DAC8541EVM.

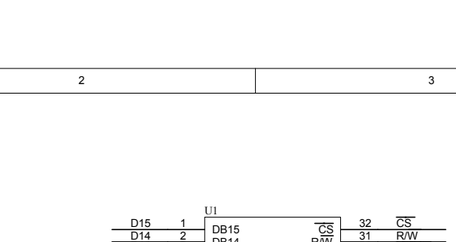
Revision History		
REV	ECN Number	Approved

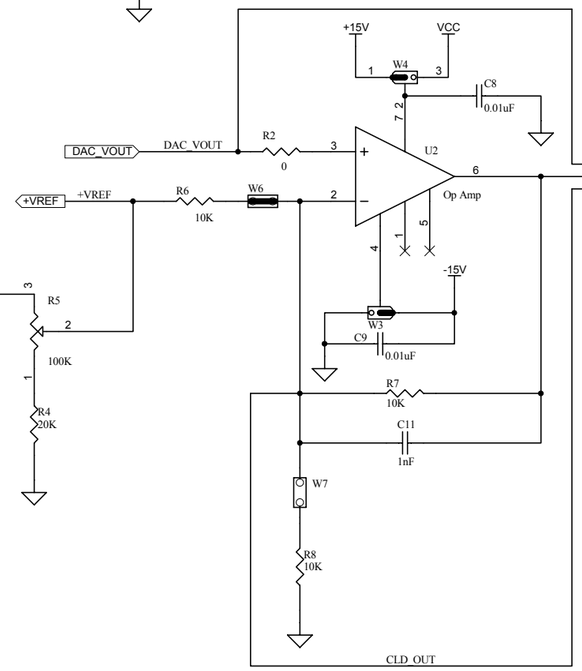


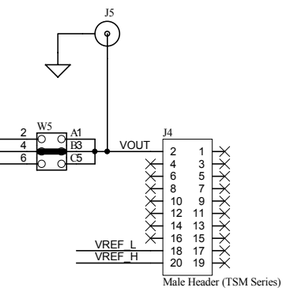


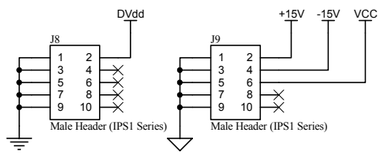


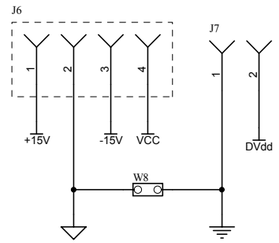












TEXAS INSTRUMENTS
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Title: DAC8541			
Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6435625		REV: A
Drawn By:			
FILE: DAC8541.Sch	DATE: 16-Feb-2004	SIZE:	SHEET: 1 OF: