TEXAS INSTRUMENTS

DAC8574 Evaluation Module

User's Guide

June 2003 *Data Acquisition - Digital/Analog Converters*

SLAU109

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It is important to operate this EVM within the input and output voltage ranges described in the EVM user's guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the DAC8574 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

Chapter 1 —EVM Overview

Chapter 2—PCB Design and Performance

Chapter 3—EVM Operation

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Data Sheets:	**Literature Number:**
DAC8574	SLAS377A
REF02	SBVS-003A
OPA627	PDS-998H
OPA2132	PDS-1309B

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Contents

Figures

Tables

Chapter 1

EVM Overview

This chapter gives a general overview of the DAC8574 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

Topic **Page**

1.1 Features

This EVM features the DAC8574 digital-to-analog converter (DAC). The DAC8574 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the high resolution, quad-channel, and serial I^2C™ input DAC. This EVM features a serial I^2C interface to communicate with any host microprocessor or TI DSP base system.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply requirement for the digital section (V_{DD}) of this EVM is typically 5 V connected to the J5-1 or via J6-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J5-2 and J6-5 terminal. The dc power supply requirements for the analog section of this EVM are as follows; the V_{CC} and V_{SS} ranges from 15.75 V to -15.75 V maximum and connects through J1-3 and J1-1 respectively, or through J6-1 and J6-2 terminals. The 5 VA connects through J5-3 or J6-3 and the 3.3 VA connects through J6-8. All of the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The device under test, U1, analog power supply can be powered by either 5 VA or 3.3 VA by selecting the proper position of jumper W1. This allows the DAC8574 analog section to operate in either supply power while the I/O and digital section is powered by 5 V, V_{DD}.

The V_{CC} supply source is mainly used to provide the positive rail of the external output op-amp, U2, the reference chip, U3 and the reference buffer, U8. The negative rail of the output op-amp, U2, can be selected between V_{SS} and AGND via W5 jumper. The external op-amp is installed as an option to provide output signal conditioning or boost capacitive load drive and for other output mode requirement desired.

Caution

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The 5-V precision voltage reference is provided to supply the external voltage reference for the DAC through REF02, U3, via jumper W4 by shorting pins 1 and 2. The reference voltage goes through an adjustable 100 kΩ potentiometer, R11, in series with 20 kΩ, R10, to allow the user to adjust the reference voltage to its desired settings. The voltage reference is then buffered through U8A as seen by the device under test. The test points TP1, TP2 and TP5 are also provided, as well as J4-18 and J4-20, to allow the user to connect other external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed 5-V dc.

The REF02 precision reference is powered by V_{CC} (15 V) through J1-3 or J6-1 terminal.

Caution

When applying an external voltage reference through TP1 or J4-20, make sure that it does not exceed 5 V maximum. Otherwise, this can permanently damage the DAC8574, U1, device under test.

1.3 EVM Basic Functions

The DAC8574 EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8574 DAC. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TI DSP, or some sort of a waveform generator.

The headers J2 and P2 are the connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8574 EVM using a custom built cable.

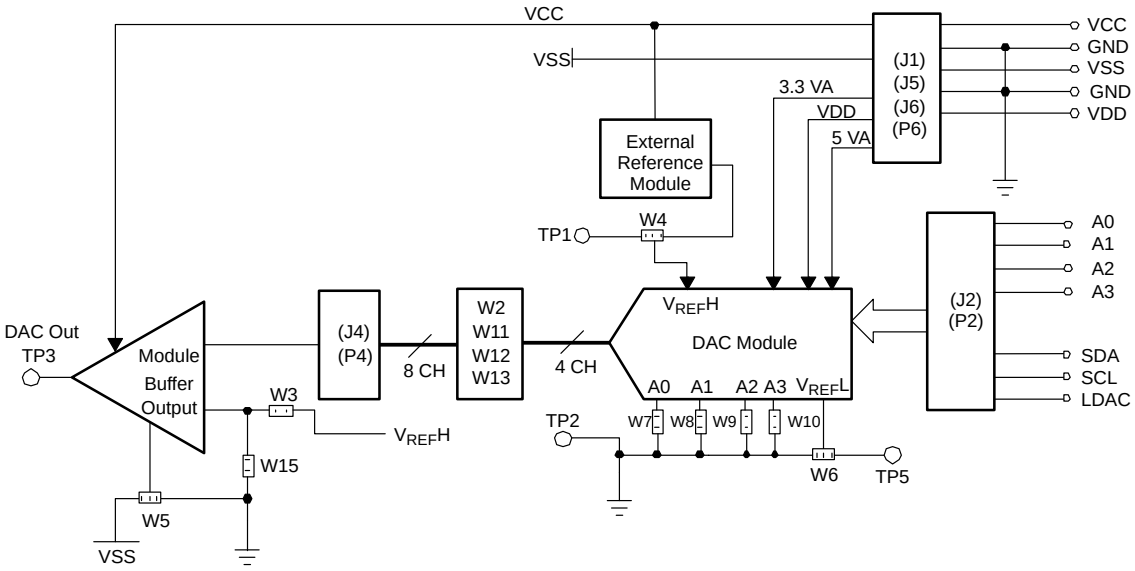
A specific adapter interface card is also available for most of TI's DSP starter kit (DSK) and the card model depend on the type of the TI DSP starter kit to be used. Make sure to specify the DSP that is used to interface with to acquire the right adapter interface card. In addition, there is also an MSP430 based platform (HPA449) that uses the MSP430F449 microprocessor, which this EVM can connect to and interface with. For more details or information regarding the adapter interface card or the HPA449 platform, please call Texas Instruments Inc. or email us at dataconvapps@list.ti.com.

The DAC outputs can be monitored through the selected pins of J4 header connector. All the outputs can be switched through their respective jumpers W2, W11, W12 and W13, for the reason of stacking. Stacking allows a total of eight DAC channels to be used provided that the I^2C address is unique for each EVM board stacked.

In addition, the option of selecting one DAC output that can be fed to the noninverting side of the output op-amp, U2, is also possible by using a jumper across the selected pins of J4. The output op-amp, U2, must first be configured correctly for the desired waveform characteristic, refer to Section 3 of this user's guide.

A block diagram of the EVM is shown in Figure 1-1.

Figure 1-1. EVM Block Diagram



Chapter 2

PCB Design and Performance

This chapter describes the layout design of the PCB, thereby, describing the physical and mechanical characteristics of the EVM. This section also shows the resulting performance of the EVM, which can be compared to the device specification listed in the data sheet. The list of components used on the module is also included in this section.

Topic **Page**

2.1 PCB Layout

The DAC8574 EVM is designed to preserve the performance quality of the DAC, device under test, as specified in the data sheet. Carefully analyzing the EVM's physical restrictions and the given or known elements that contributes to the EVM's performance degradation is the key to a successful design implementation. These obvious attributes that diminish the performance of the EVM can be taken care of during the schematic design phase, by properly selecting the right components and building the circuit correctly. The circuit must include adequate bypassing, identifying and managing the analog, and digital signals and knowing or understanding the components mechanical attributes.

The obscure part of the design is the layout process where lack of knowledge and inexperience can easily present a problem. The main concern here is primarily with the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and must be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane can do the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces, but use the biggest possible trace width allowable in the design. These design practices discussed can be seen in the following figures presented on the following pages.

The DAC8574 EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) X 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figures 2-1 through 2-6 show the individual artwork layers.

Figure 2-1. Top Silkscreen

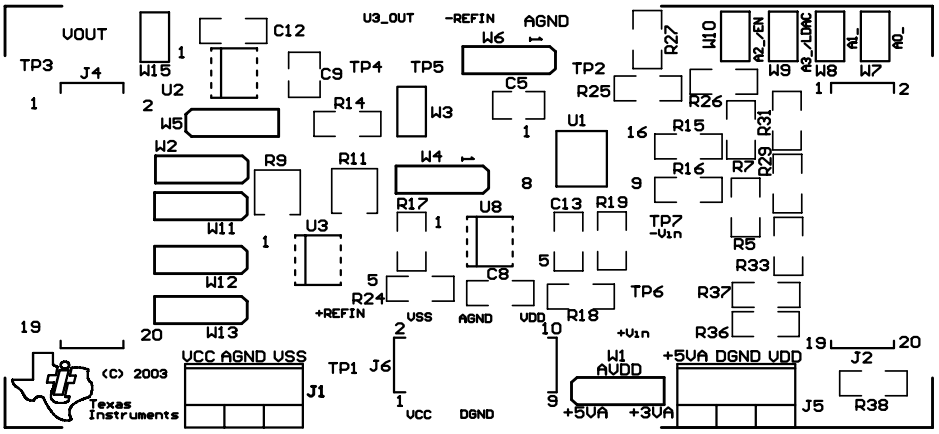


Figure 2-2. Layer 1 (Top Signal Plane)

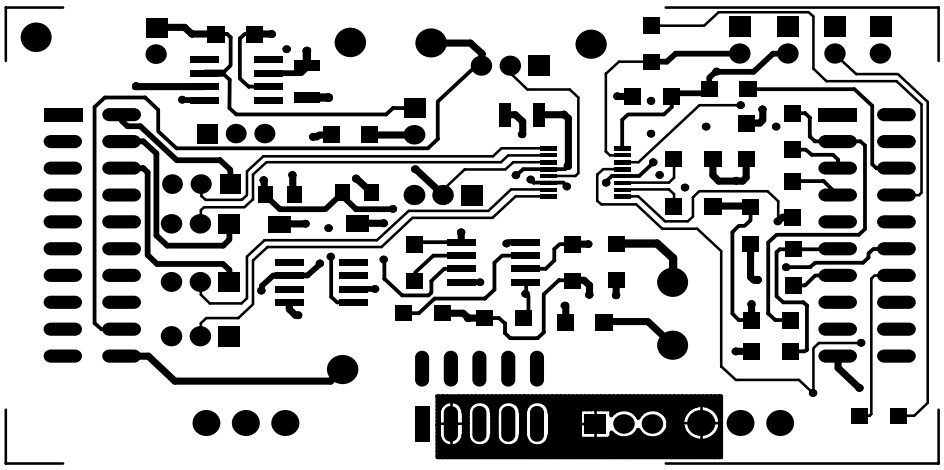


Figure 2-3. Layer 2 (Ground Plane)

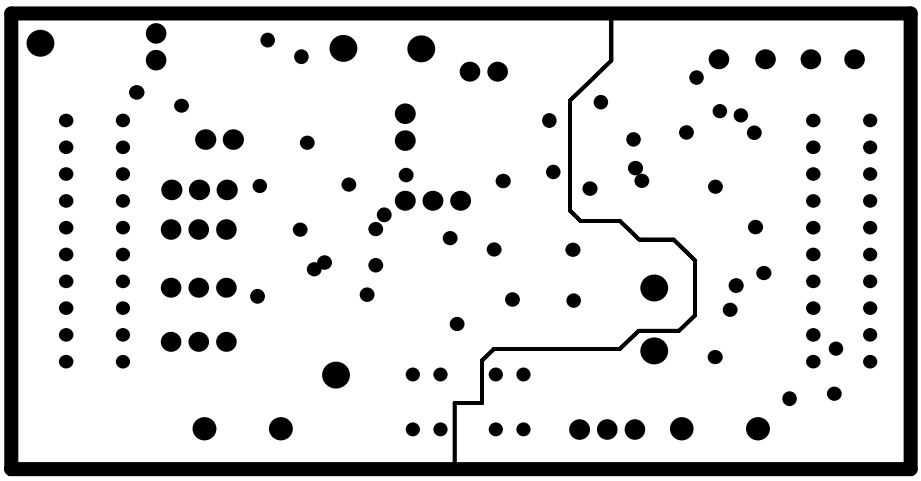


Figure 2-4. Layer 3 (Power Plane)

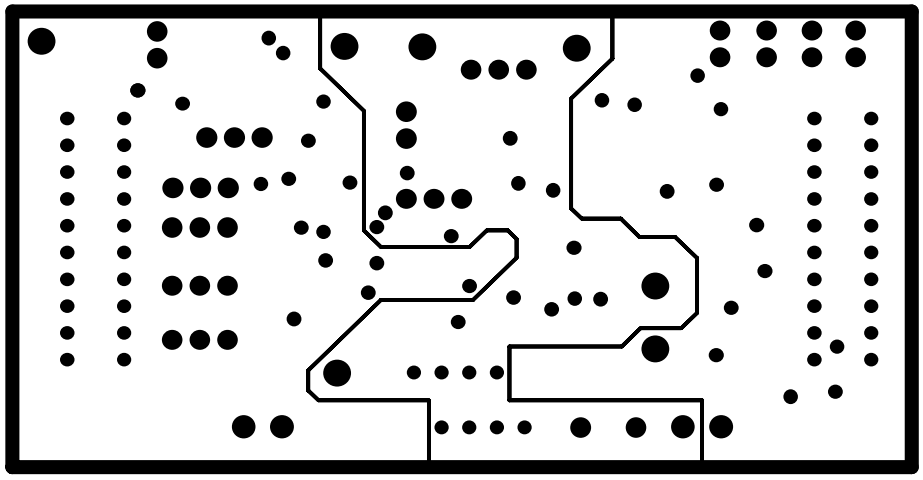


Figure 2-5. Layer 4 (Bottom Signal Plane)

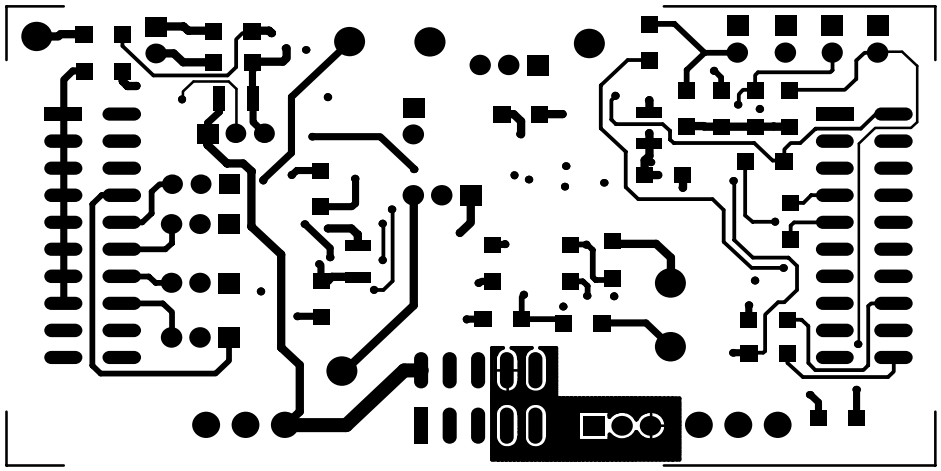


Figure 2-6. Bottom Silkscreen

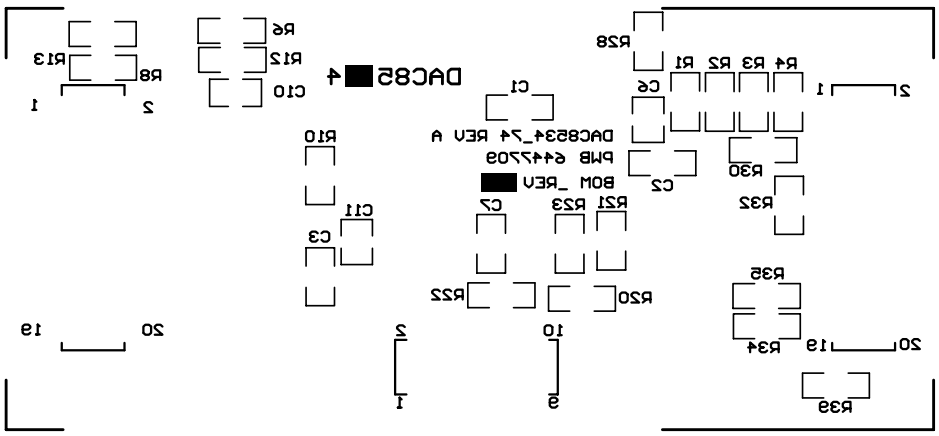
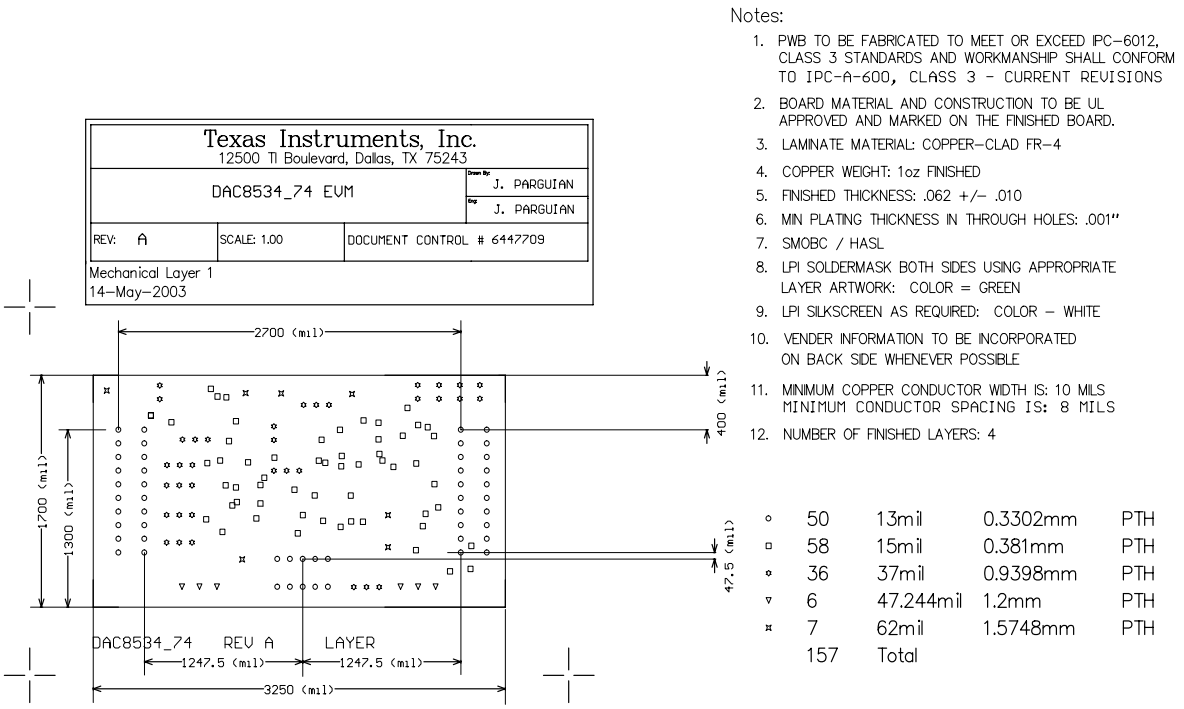


Figure 2-7. Drill Drawing



2.2 EVM Performance

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LABVIEW software. The EVM board is tested for all codes of 65535 and the device under test (DUT) is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL results and is shown in Figure 2-9.

The parameters and results of the DAC8574 EVM characterization test can be seen in Figure 2-8.

Figure 2-8. DAC8574 EVM Test Parameters and Results

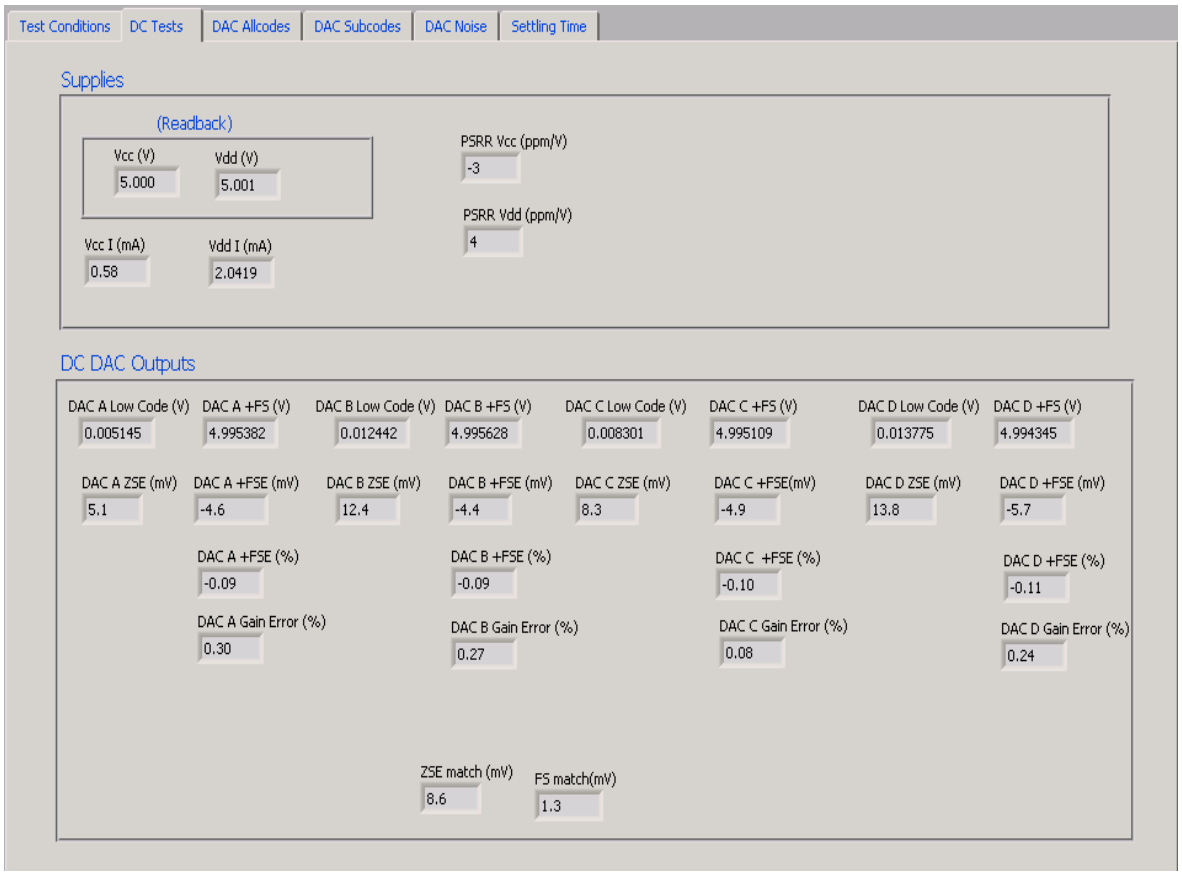


Figure 2-9. INL and DNL Characterization Graph of DAC A

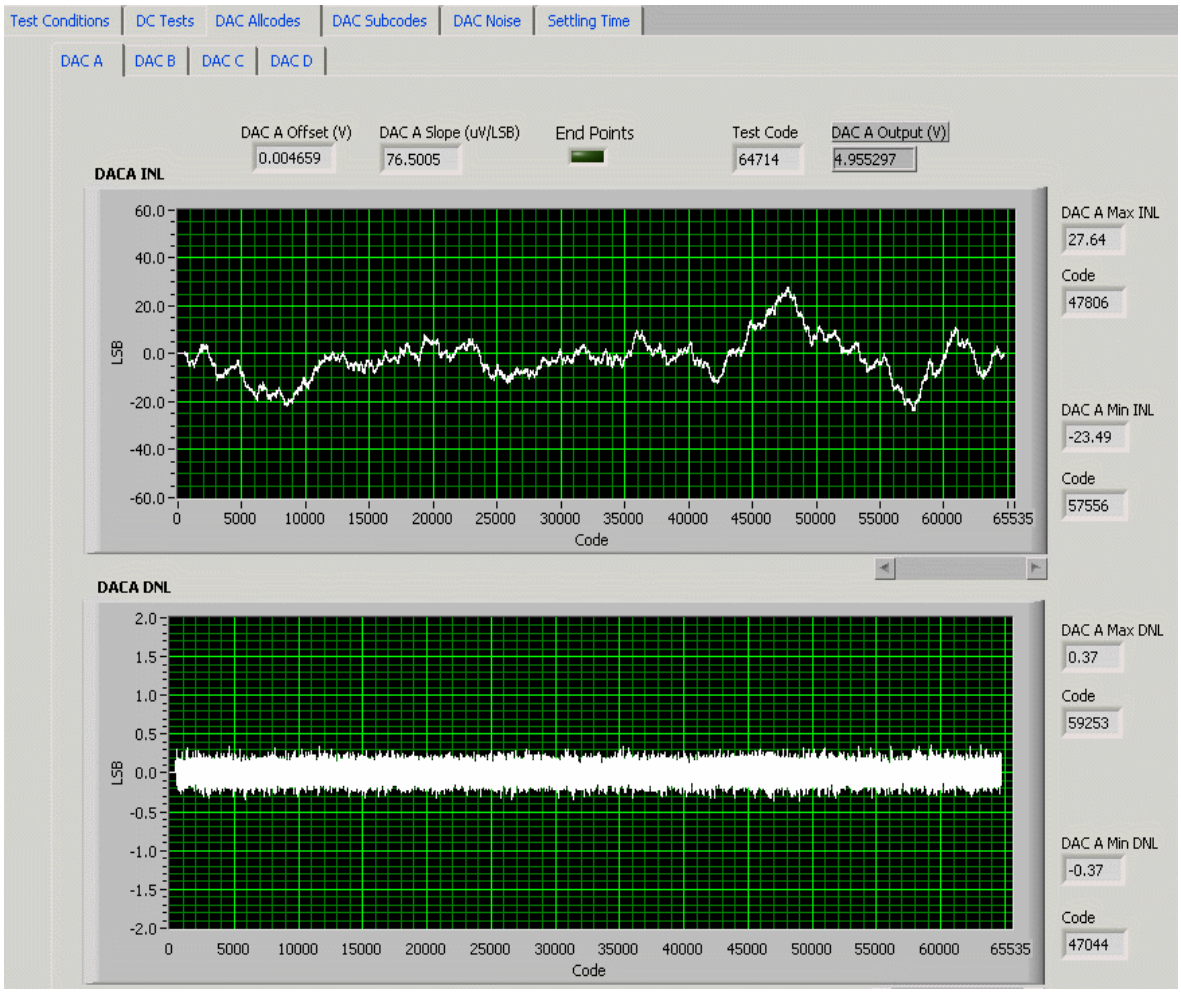


Figure 2-10. INL and DNL Characterization Graph of DAC B

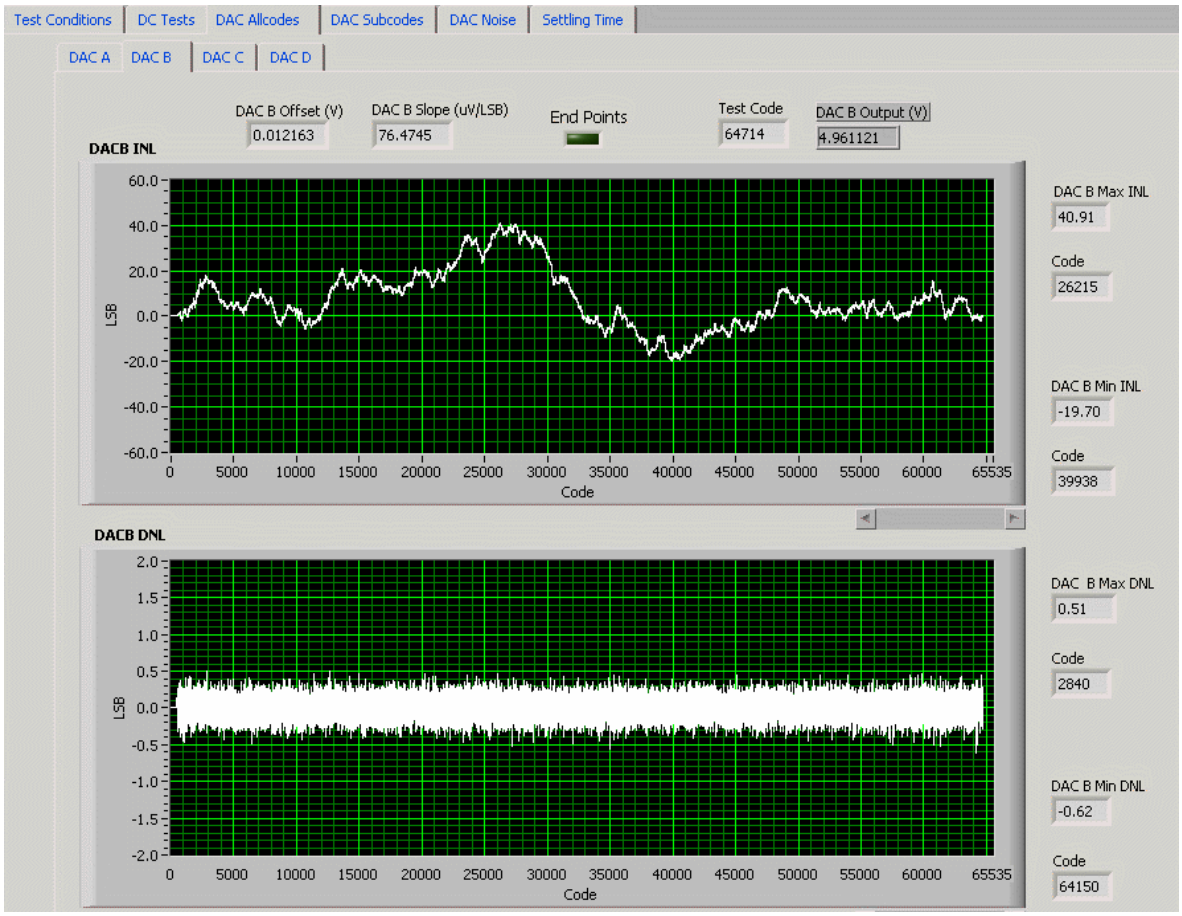


Figure 2-11. INL and DNL Characterization Graph of DAC C

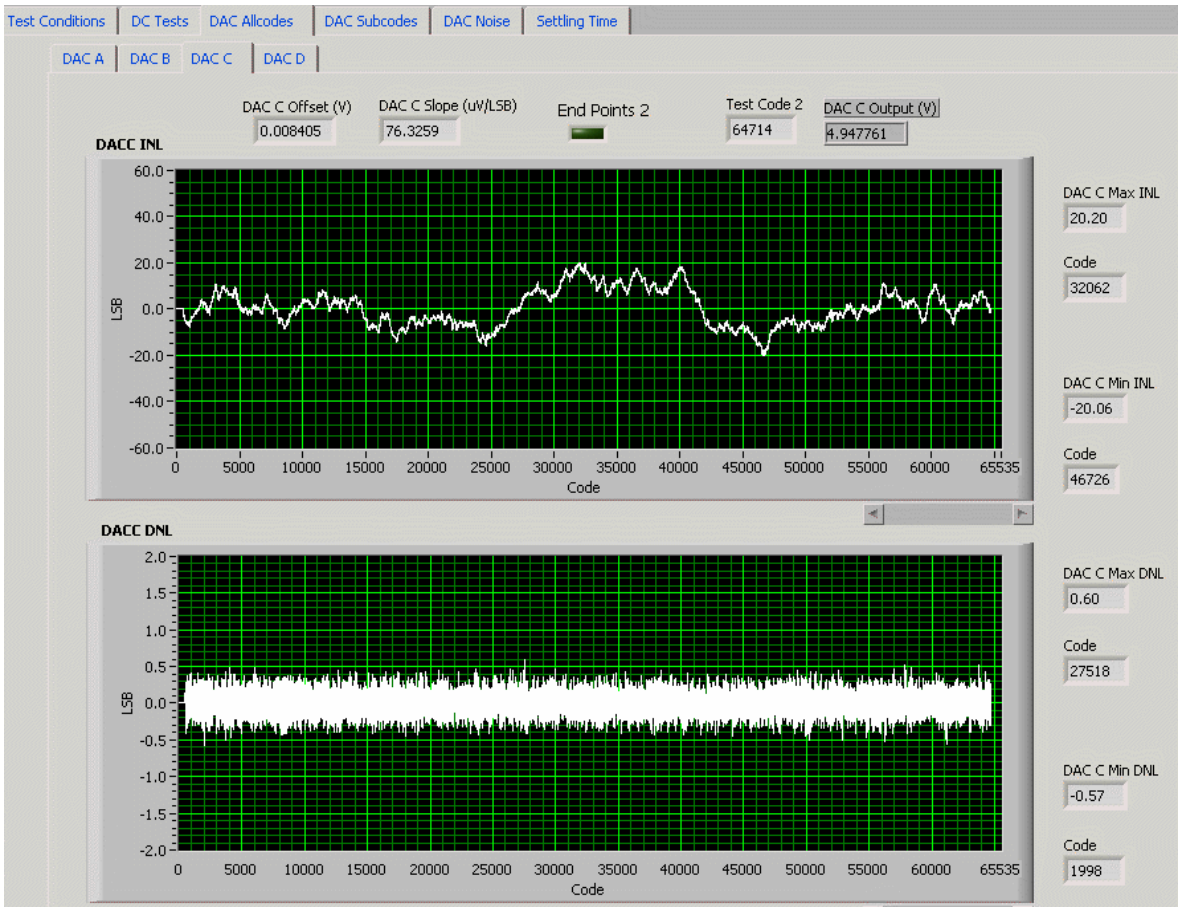
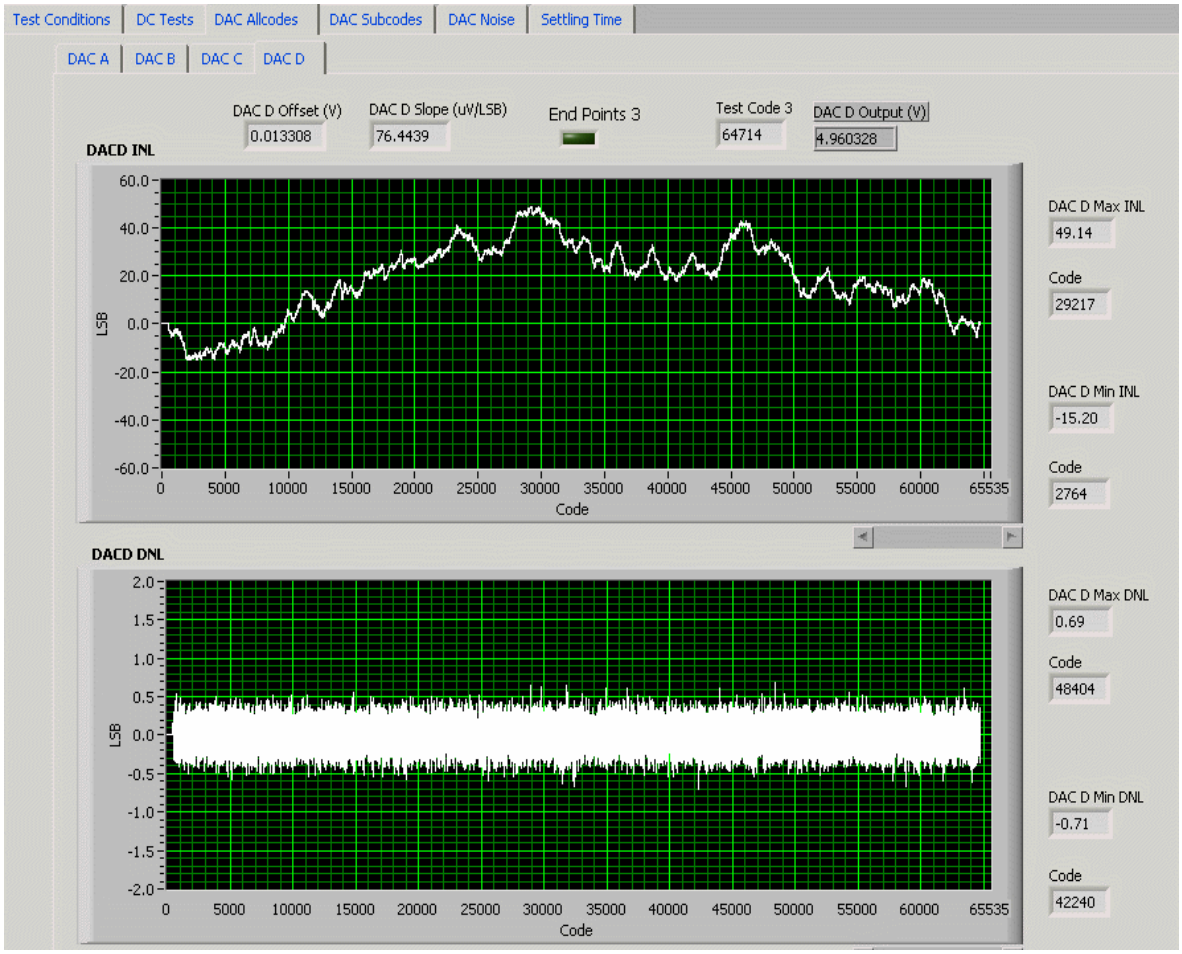


Figure 2-12. INL and DNL Characterization Graph of DAC D



2.3 Bill of Materials

Table 2-1. Parts List

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	2	C9 C10	Panasonic	ECUV1H105JCH	1 µF, 1206 Multilayer ceramic capacitor
2	4	C1 C2 C3 C7	Panasonic	ECJ3VB1C104K	0.1 µF, 1206 Multilayer ceramic capacitor
3	1	C12	Panasonic	ECUV1H102JCH	1 nF, 1206 Multilayer ceramic capacitor
4	3	C5 C6 C11	Kemet	C1210C106K8PAC	10 µF, 1210 Multilayer ceramic X5R capacitor
5	17	R8 R17 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39	Panasonic	ERJ-8GEY0R00V	0 Ω, 1/4W 1206 Chip resistor
6	2	R15 R16	Panasonic	ERJ-8GEYJ431V	430 Ω, 1/4W 1206 Chip resistor
7	1	R13	Panasonic	ERJ-8GEYJ101V	100 Ω, 1/4W 1206 Chip resistor
8	1	R10	Panasonic	ERJ-8ENF2002V	20 kΩ, 1/4W 1206 Chip resistor
9	6	R1 R2 R3 R4 R5 R7	Panasonic	ERJ-8GEYJ302V	3 kΩ, 1/4W 1206 Chip resistor
10	3	R6 R12 R14	Panasonic	ERJ-8ENF1002V	10 kΩ, 1/4W 1206 Chip resistor
11	1	R9	Bourns	3214W-203E	20 kΩ, BOURNS_32X4W Series 5T Pot
12	1	R11	Bourns	3214W-104E	100 kΩ, BOURNS_32X4W Series 5T Pot
13	1	J6	Samtec	TSM-105-01-T-DV	5X2X0.1, 10-pin 3A isolated power socket
14	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10X2X.1, 20 pin 0.025”sq SMT socket
15	2	J1 J5	On-Shore Technology	ED555/3DS	3-Pin terminal connector
16	1	U1	Texas Instruments	DAC8574IPW	16 Bit, quad voltage output, serial input I^2C DAC, TSSOP-16
17	1	U2	Texas Instruments	OPA627AU	8-SOP(D) precision op amp
18	1	U3	Texas Instruments	REF02AU	+5V, 8-SOP(D) precision voltage reference
19	1	U8	Texas Instruments	OPA2132UA	8-SOP(D) dual precision op amp
20	7	TP1 TP2 TP3 TP4 TP5 TP6 TP7	Mill-max	2348-2-01-00-00-07-0	Turret terminal test point
21	2	P2 P4 (see Note)	Samtec	SSW-110-22-S-D-VS-P	20 Pin 0.025”sq SMT terminal strips
22	1	P6 (see Note)	Samtec	SSW-105-F-D-VS-K	3A Isolated 10-pin power header
23	6	W3 W7 W8 W9 W10 W15	Molex	22-03-2021	2 Position jumper_ 0.1” spacing
24	8	W1 W2 W4 W5 W6 W11 W12 W13	Molex	22-03-2031	3 Position Jumper_ 0.1” spacing

Note: P2, P4 & P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.

Chapter 3

EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

Refer to the DAC8574 data sheet (SLAS377A), for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

Topic **Page**

3.1 Factory Default Setting

The EVM board is set to its default configuration from the factory as described in Table 3-1 to operate in gain of 2 configuration (0 V to +10-V) mode of operation.

Table 3-1. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	Analog supply for the DAC8574 is +5VA.
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	OPEN	$V_{REF}H$ is not routed to the inverting input of the op amp.
W4	1-2	Onboard external buffered reference U3 is routed to $V_{REF}H$.
W5	1-2	Negative supply rail of U2 op-amp is supplied with V_{SS}.
W6	1-2	$V_{REF}L$ is tied to AGND.
W7	CLOSE	A0 pin is tied to DGND.
W8	CLOSE	A1 pin is tied to DGND.
W9	CLOSE	A3 pin is tied to DGND.
W10	CLOSE	A2 pin is tied to DGND.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
W15	CLOSE	Output op amp, U2, is configured for a gain of 2.
J4	1-2	DAC output A ($V_{OUT}A$) is connected to the noninverting input of the output op-amp, U2.

3.2 Host Processor Interface

The host processor basically drives the DAC, so the DAC's proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for the specific TI DSP starter kit as well as an MSP430 based microprocessor as mentioned in chapter 1 of this manual. Using the interface card alleviates the tedious task of building customize cables and allows easy configuration of a simple evaluation system.

The DAC8574 interfaces with any host processor capable of handling I^2C protocols or the popular TI DSP. For more information regarding the DAC8574 data interface, refer to the data sheet (SLAS377A).

3.3 EVM Stacking

The stacking of EVMs is possible if there is a need to evaluate two DAC8574s to yield a total of eight channel outputs. A maximum of two EVMs are allowed since the output terminal, J4, dictates the number of DAC channels that can be connected without colliding. Table 3-2 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2, W11, W12 and W13.

Table 3-2. DAC Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
	2-3	DAC output A ($V_{OUT}A$) is routed to J4-10.
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
	2-3	DAC output B ($V_{OUT}B$) is routed to J4-12.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
	2-3	DAC output C ($V_{OUT}C$) is routed to J4-14.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
	2-3	DAC output D ($V_{OUT}D$) is routed to J4-16.

In order to allow exclusive control of each EVM that are stacked together, each DAC8574 EVM must have its own unique I^2C address. This is accomplished by configuring the address jumpers W7 through W10 (refer to the data sheet for I^2C addressing).

The LDAC signal can be shared to have a synchronous DAC output update and is hardware driven by GPIO0. If controlling the LDAC through software is desired, the GPIO0 signal must be set low through software or the J2 pin 2 can be pin strapped to DGND.

3.4 The Output Op-Amp

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation since the odd numbered pins (J4-1 to J4-15) are tied together. The output op-amp is set to a gain of 2 configuration by default. Nevertheless, the raw outputs of the DAC can be probed through the even pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into any interface card. In addition, it provides easy access for monitoring up to eight DAC channels when stacking two EVMs together, refer to Section 3.3 above.

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC8574, though it may present some slight distortion because of the feedback resistor and capacitor. Users can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R7 and C11 and replacing it with the desired values. You can also simply get rid of R7 and C11 altogether, and just solder a 0-Ω resistor in replacement of R7, if desired.

Table 3-3 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 3-3. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	OPEN	OPEN	Disconnect $V_{REF}H$ from the inverting input of the op-amp.
W5	2-3	1-2	Supplies V_{SS} to the negative rail of op-amp or ties it to AGND.
W15	OPEN	OPEN	Disconnect negative input of op-amp from AGND.

3.4.2 Output Gain of Two

There are two types of configurations that yield a gain of two output depending on the setup of the jumpers W3 and W15. These configurations allow the user to choose whether the DAC output has $V_{REF}H$ as an offset or not.

Table 3-4 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 3-4. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Close	Close	Inverting input of the output op-amp, U2, is connected to $V_{REF}H$ for use as its offset voltage with a gain of 2. W15 jumper must be open.
	Open	Open	$V_{REF}H$ is disconnected from the inverting input of the output op-amp, U2. W15 jumper must be close.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op-amp, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Close	Close	Configures op-amp, U2, for a gain of 2 output without a voltage offset. W3 jumper must be open.
	Open	Open	Inverting input of the op-amp, U2, is disconnected from AGND. W3 jumper must be close.

3.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all op-amps under certain conditions may become unstable depending on the op-amp configuration, gain, and load value. These are just few factors that can affect op-amps stability performance and must be considered when implementing.

In unity gain, the OPA627 op-amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and adding a load resistor would even improve the capacitive load drive capability.

Table 3-5 shows the jumper setting configuration for a capacitive load drive.

Table 3-5. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Close	Close	$V_{REF}H$ is disconnected from the inverting input of the output op-amp, U2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op-amp, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Close	Open	Capacitive load drive output of DAC is routed to pin 1 of W15 jumper and maybe used as the output terminal.

3.5 Optional Signal Conditioning Op-Amp (U8B)

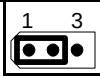
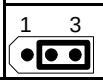
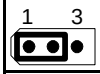
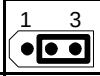
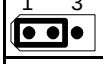
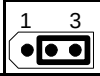
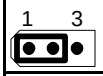
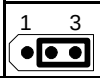
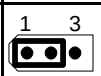
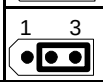
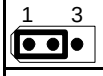
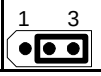
One part of the dual package op-amp, OPA2132 (U8), is used for reference buffering (U8A) while the other is unused. This unused op-amp (U8B) is left for whatever op-amp circuit application the user desires to implement. The 1206 footprint for the resistors and capacitors surrounding the U8B op-amp are not populated and made available for easy configuration. TP6 and TP7 test points are not installed either so it is up to the user on how to connect the ± input signals to this op-amp. No test point has been made available for the output due to space restriction, but a wire can be simply soldered to the output of the op-amp via unused component pads that connects to it.

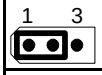
Once the op-amp circuit is realized the configuration becomes easy by simply populating the corresponding components that matches the circuit designed and leaving all other unused component footprints unpopulated.

3.6 Jumper Setting

Table 3-6 shows the function of each specific jumper setting of the EVM.

Table 3-6. Jumper Setting Functions

Reference	Jumper Setting	Function
W1		+5-V analog supply is selected for AV_{DD}.
		+3.3-V analog supply is selected for AV_{DD}.
W2		Routes $V_{OUT}A$ to J4-2.
		Routes $V_{OUT}A$ to J4-10.
W3		Disconnects $V_{REF}H$ to the inverting input of the output op-amp, U2
		Connects $V_{REF}H$ to the inverting input of the output op-amp, U2
W4		Routes the adjustable, buffered, onboard +5-V reference to the $V_{REF}H$ input of the DAC8574.
		Routes the user supplied reference from TP1 or J4-20 to the $V_{REF}H$ input of the DAC8574.
W5		Negative supply rail of the output op-amp, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output op-amp, U2, is tied to AGND for unipolar operation.
W6		$V_{REF}L$ is tied to AGND.
		Routes the user supplied negative reference from TP2 or J4-18 to the $V_{REF}L$ input of the DAC8574. This voltage should be within the range of 0V to $V_{REF}H$.
W7		A0 pin is set high through pullup resistor, R4. A0 can be driven by GPIO5.
		A0 pin is set low.
W8		A1 pin is set high through pullup resistor, R3. A1 can be driven by GPIO4.
		A1 pin is set low.
W9		A3 pin is set high through pullup resistor, R2. A3 can be driven by GPIO1.
		LDAC pin is set low and DAC update is accomplished via software.
W10		A2 pin is set high through pullup resistor, R1. A2 can be driven by GPIO3.
		A2 pin is set low.
W11		Routes $V_{OUT}B$ to J4-4.
		Routes $V_{OUT}B$ to J4-12.

Reference	Jumper Setting	Function
W12		Routes $V_{OUT}C$ to J4-6.
		Routes $V_{OUT}C$ to J4-14.
W13		Routes $V_{OUT}D$ to J4-8.
		Routes $V_{OUT}D$ to J4-16.
W15		Disconnects the inverting input of the output op amp, U2, from AGND.
		Connects the inverting input of the output op amp, U2, to AGND for gain of 2.

Legend:  Indicates the corresponding pins that are shorted or closed.

3.7 Schematic

The schematic is located on the following page.

Revision History		
REV	ECN Number	Approved

VDD
+5VA
+3.3VA
W1
AVDD
R1 10K
R2 10K
R3 10K
R4 10K
R5 3K
R7 3K
C1 0.1µF
C5 10µF
C6 10µF
C2 0.1µF
GPIO0 R25 0 (LDAC)
GPIO1 R26 0 (A3)
GPIO2 R27 0 (EN)
GPIO3 R28 0 (A2)
GPIO4 R38 0 (A1)
GPIO5 R39 0 (A0)
W10 W9 W8 W7
SDI R15 440/0
SCLK R16 440/0
FSX (SYNC) R29 0
GPIO0 (LDAC) R30 0
U1
AVDD
IO_V/DVDD
VrefH
VrefL
A3/LDAC
A2/EN
A1
A0
SDA/Din
SCL/SCLK
LDAC/SYNC
GND
VoutA
VoutB
VoutC
VoutD
DAC7574/8534/8574
OUT_A
OUT_B
OUT_C
OUT_D
W2
W11
W12
W13
OUT_A1
OUT_A2
OUT_B1
OUT_B2
OUT_C1
OUT_C2
OUT_D1
OUT_D2
-REFin
+REFin
J4
OUTPUT HEADER
U2_+IN
R8 0
W3
U2_-IN
R14 10K
VrefH
VCC
C9 1µF
U2
Op Amp
U2_OUT
R13 100
TP3
VOUT
VSS
W5
C10 1µF
R6 10K
C12 1nF
W15
R12 10K
U3
TRIM OUT
V+ TEMP
NC NC
NC GND NC
REF02AU(8)
Tantalum C11 10µF
C3 0.1µF
R9 20K
R11 100K
R10 20K
TP4
C7 0.1µF
U8A
OPA2227UA
R17 0
W4
W6
TP1
TP5
TP2
+REFin
-REFin
EXTERNAL REFERENCE
NOTE: Voltage range of -REFin input should not exceed 0 - VrefH.
VrefH
VrefL
TP6 +Vin
TP7 -Vin
R18 NI
R19 NI
R20 NI
R21 NI
R22 NI
R23 NI
R24 NI
C8 NI
C13 NI
U8B
OPA2227UA
J2
Serial Header
GPIO0 (LDAC)
GPIO1 (A3)
GPIO2 (EN)
GPIO3 (A2)
GPIO4 (A1)
GPIO5 (A0)
SCL
SDA
R31 0 CLKX
R32 0 FSX
R33 0 DX
0 DR
DX R36 0
SDI R34 0
SCLK R35 0
CLKX R37 0
+3.3VD +1.8VD +5VA VCC VSS -5VA +3.3VA VDD
J6
J1
VSS VCC
J5
VDD +5VA

VCC = +15V Analog
VDD = +2.7V to +5.0V Digital
VSS = 0V to -15V Analog

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Engineer: J. PARGUIAN	DOCUMENTCONTROL # 6447711		REV: A
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