AMC1311EVM Users Guide

The AMC1311 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide reinforced galvanic isolation of up to 7000 V_{PEAK} per DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01.

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Trademarks

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1 Introduction

For use in high-resolution voltage measurement applications, the high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

Throughout this document, the abbreviation EVM and the term evaluation module are synonymous with the AMC1311EVM.

1.1 Features

- Full-featured Evaluation Module for the AMC1311 single-channel precision isolation amplifier.
- Screw terminals for easy access to analog inputs and outputs.
- Transformer and rectifiers to provide an isolated 5-V source to VDD1.
- Differential to Single-ended output option.

2 Analog Interface

The analog input to the AMC1311 is routed from a three-wire screw terminal screw at J1.1 which provides access to the VINP terminal. A test point, TP1 is also provided along with pads for 1206 size user installed series resistors R1, R2 and R3 to create a voltage divider circuit for the input to the AMC1311. The analog input is referenced to J1.2 or TP2.

2.1 Analog Input

The default analog input to the AMC1311EVM board is comprised of R4 and C3 which form a simple anti-aliasing filter with a corner frequency of 723 Hz. The input circuit for the AMC1311 is shown in Figure 1. Using a signal generator or other voltage source, the user can apply an input signal directly to J1 pin 1. The maximum voltage input to the AMC1311 via J1.1 is 2 V referenced to J1.2 or TP2.

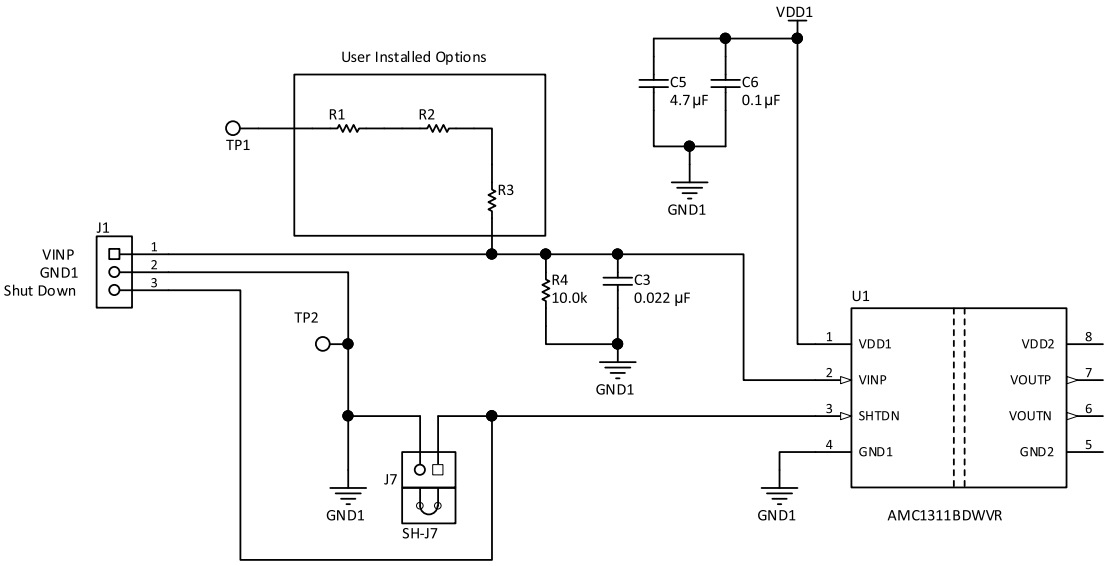

Figure 1. AMC1311EVM Schematic – Analog Input Section

With user installed resistor options R1 through R3, an external voltage source can be applied between TP1 and GND1 via J1.2 or TP2. As depicted in Figure 1, with R4 installed as 10 kΩ, resistors R1 through R3 can be chosen according to Equation 1:

$$R1 + R2 + R3 = \frac{V_{TP1} - V_{INP}}{V_{INP}} \; x \; R4 \tag{1}$$

2.2 Shutdown

The AMC1311 features a shutdown option which is an active high input. Shunt jumper SH-J7 is installed by default and allows for normal operation of the AMC1311 device. When the shunt jumper is removed, the AMC1311 enters into a low power mode by means of an internal pullup resistor for battery or other power sensitive applications. For external shutdown operation, J1.3 provides access to the SHTDN pin when shunt SH-J7 is removed.

2.3 Analog Output

The analog output from the AMC1311EVM board is a fully differential signal centered at 1.44 V. The differential output of U1 is available on the two screw terminals of J2 as shown below in Figure 2. U4 and U5 provide the user with a single-ended version of the analog output on J6 pin 1. U5 is designed to provide bias voltage to the difference amplifier configuration of U4. The single ended output provides unity gain with an output voltage swing from 0.5 V to 2.5 V. If a different bias voltage is desired, the shunt on J8 can be moved to cover pins 2-3 and an external voltage source may be applied to TP4 referenced to GND2 via TP3.

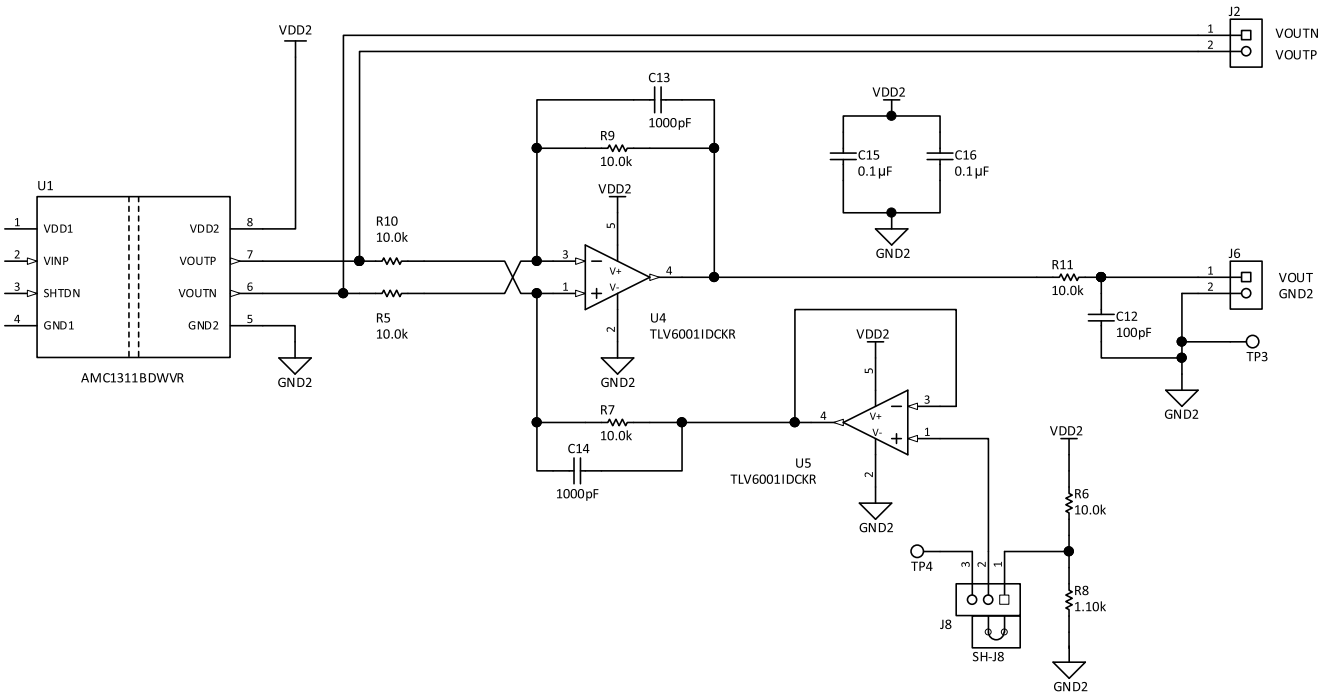

Figure 2. AMC1311EVM Schematic – Analog Output Section

3 Power Supplies

The AMC1311EVM requires two separate power rails, VDD1 and VDD2. VDD1 is on the high voltage side of the amplifier. VDD2 is on the user side of the amplifier.

3.1 VDD1 Input

The default configuration of the EVM provides 5V to VDD1 through transformer T1 via U3, an SN6501 push-pull driver. A shunt on jumper J5 is shorting pins 1-2 which routes the regulated 5V from U2, a TPS76350, to pin 1 of U1. The screw terminal at J4 allows the user to provide their own VDD1 source when the shunt on J5 is covering pins 2-3. The VDD1 supply should be between 3 and 5.5 VDC when using an external voltage source. The input power scheme is shown in Figure 3.

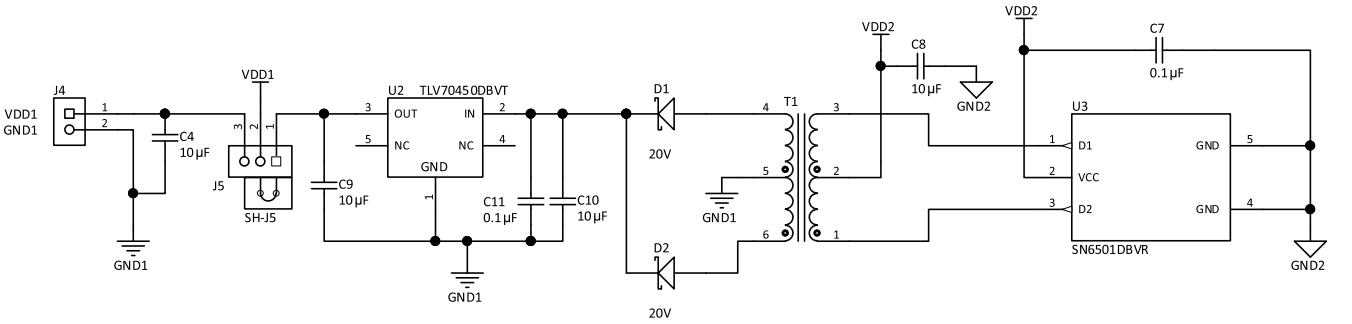

Figure 3. VDD1 Input

3.2 VDD2 Input

The user side of the AMC1311 isolation amplifier is rated for 3.0 to 5.5 VDC and is applied to the amplifier using J3 pin 1. When using the on-board transformer for VDD1, a minimum of 3.6 V is needed at J3. Figure 4 depicts the power input for VDD2.

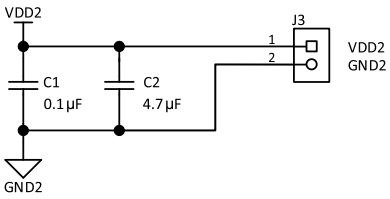

Figure 4. VDD2 Input Connector

4 EVM Operation

The following section describes the general operation of the AMC1311EVM.

4.1 Isolated Power and Analog Inputs: J1 and J4

The analog input voltage to the AMC1311EVM can be applied directly to J1 pins 1 and 2.

Table 1 lists the details of J1.

Table 1. J1 – Analog Input

Pin Number	Signal	Description
J1.1	VINP	Analog input to the AMC1311.
J1.2	GND1	Ground connection.
J1.3	ShutDown	Optional input to drive the shutdown pin from an external source.

The isolated power input to the AMC1311EVM printed circuit board (PCB) can be applied directly to J4 pins 1 and 2. Table 2 lists the details of J4.

Table 2. J4 - VDD1 Power

Pin Number	Signal	Description
J4.1	VDD1	Connection to the AMC1311 VDD1 terminal (pin 1) with SH-J5 shorting pins 2-3 on J5.
J4.2	GND1	Connection to the AMC1311 GND1 terminal (pin 4).

CAUTION

Carefully review the AMC1311 product data sheet for the limitations of the analog input range, and ensure that the appropriate analog/digital voltages are applied prior to connecting any analog input to the EVM. The transformer on the evaluation module is rated to 2500 Vrms, but the board is not certified for high voltage operation.

4.2 User Power and Analog Outputs: J2, J3 and J6

The differential analog output voltage from the AMC1311EVM printed circuit board is applied directly to J2 pins 1 and 2. Table 3 lists the details of J2.

Table 3. J2 – Differential Analog Output

Pin Number	Signal	Description
J2.1	VOUTN	Non-inverting analog output from the AMC1311 (pin 6).
J2.2	VOUTP	Inverting output from the AMC1311 (pin 7).

The VDD2 power input to the AMC1311EVM printed circuit board can be applied directly to J3 pins 1 and 2. Table 4 lists the details of J3.

Table 4. J3 – VDD2 Power

Pin Number	Signal	Description
J3.1	VDD2	Connection to the AMC1311 VDD2 terminal (pin 8).
J3.2	GND2	Connection to the AMC1311 GND2 terminal (pin 5).

The single-ended analog output voltage from the AMC1311EVM printed circuit board is applied directly to J6 pin 1 referenced to pin 2. Table 5 lists the details of J6.

Table 5. J6 – Single-Ended Analog Output

Pin Number	Signal	Description
J6.1	VOUT	Single-ended analog output from the AMC1311 through U4.
J6.2	GND2	Ground reference.

4.3 Device Operation

Once the VDD1 and VDD2 power is applied to the AMC1311EVM, the analog output will be available with a fixed gain of one and a DC offset equal to 1.44 V (typical).

An analog input signal may be applied directly at screw terminal J2. Refer to Figure 1 and Table 2 for details. The analog input range is specified at 0 to 2 V.

The analog output has a nominal gain of 1 through the AMC1311 isolation amplifier. With an input voltage of 0 – 2 V, the nominal output is ±1 V differential. The output voltage is centered on 1.44 V providing a convenient analog input range to the embedded ADCs of the MSP430 and TMS320C2000 series of digital processors.

5 Board Layout

This section contains the and printed circuit board (PCB) layout of the AMC1311EVM.

NOTE: Board layouts are not to scale. These are intended to show how the board is laid out, and are not intended to be used for manufacturing AMC1311EVM PCBs.

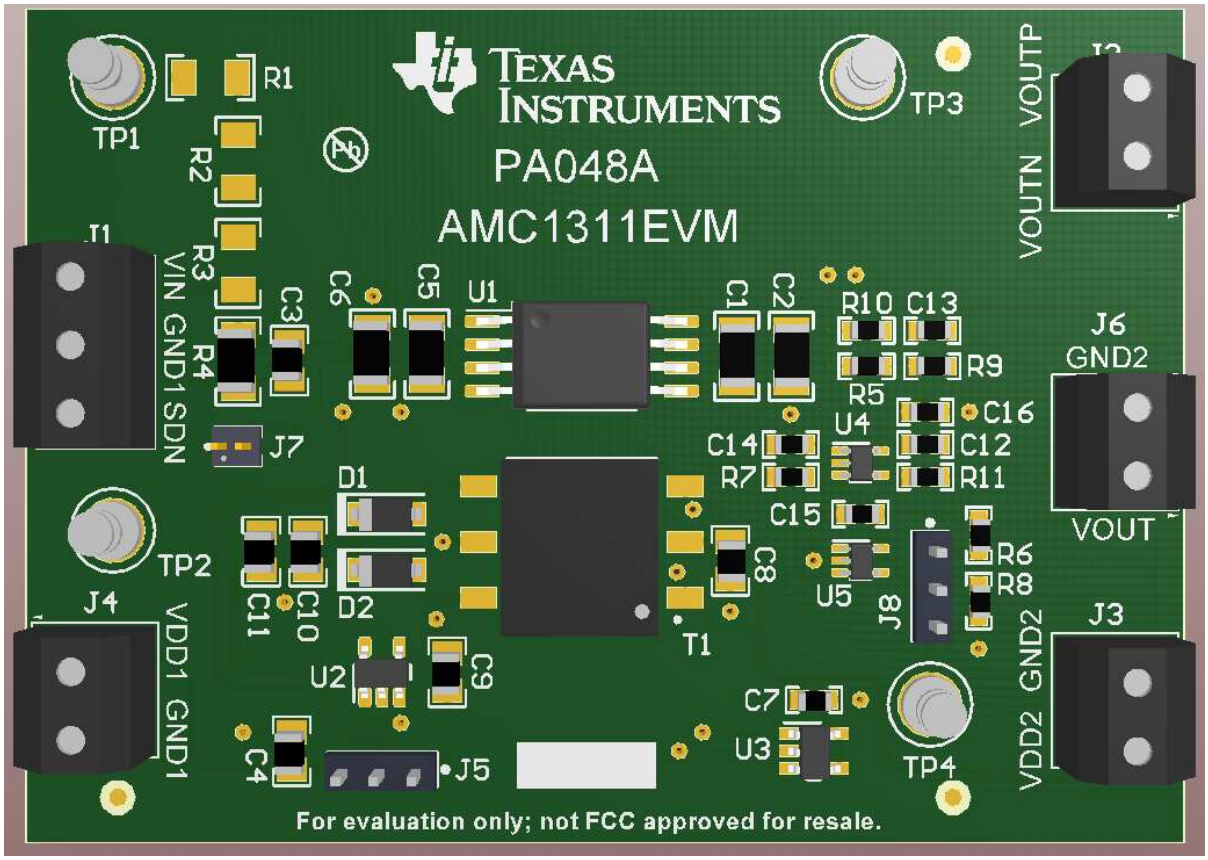

Figure 5. AMC1311 Silk Screen Drawing

6 Schematic and Bill of Materials

This section contains the complete bill of materials, and schematic diagram of the AMC1311EVM.

6.1 Bill of Materials

Table 6. Bill of Materials

Designator	Description	Manufacturer	Mfg. Part Number
C1, C6	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, 1206	AVX	12065C104KAT2A
C2, C5	CAP, CERM, 4.7 µF, 25 V,+/- 20%, X5R, 1206	AVX	12063D475MAT2A
C3	CAP, CERM, 0.022 µF, 50 V, +/- 1%, C0G/NP0, 0805	Kemet	C0805C223F5GACTU
C4, C8, C9, C10	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	Taiyo Yuden	EMK212BJ106KG-T
C7, C15, C16	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	AVX	06035C104KAT2A
C11	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0805	Kemet	C0805C104K3RACTU
C12	CAP, CERM, 100 pF, 10 V, +/- 10%, X7R, 0603	AVX	0603ZC101KAT2A
C13, C14	CAP, CERM, 1000 pF, 10 V, +/- 10%, X7R, 0603	AVX	0603ZC102KAT2A
D1, D2	Diode, Schottky, 20V, 0.5A, SOD-123	ON Semiconductor	MBR0520LT1G
J1	Terminal Block, 3.5mm Pitch, 3x1, TH	On-Shore Technology	ED555/3DS
J2, J3, J4, J6	Terminal Block, 3.5mm Pitch, 2x1, TH	On-Shore Technology	ED555/2DS
J5, J8	Header, 2mm, 3x1, Tin, TH	Samtec	TMM-103-01-T-S
J7	Header, 50mil, 2x1, Gold, TH	Sullins Connector Solutions	GRPB021VWVN-RC
R4	RES, 10.0 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW120610K0FKEA
R5, R6, R7, R9, R10, R11	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA
R8	RES, 1.10 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K10FKEA
T1	Transformer, 340uH, SMT	Wurth Elektronik	750313769
TP1, TP2, TP3, TP4	Terminal, Turret, TH, Double	Keystone	1502-2
U1	Precision, 2-V Input, Reinforced Isolated Amplifier, DWV0008A (SOIC-8)	Texas Instruments	AMC1311DWVR
U2	Single Output LDO, 150 mA, Fixed 5 V Output, 2.5 to 24 V Input, with Ultra-Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TLV70450DBVT
U3	Transformer Driver for Isolated Power Supplies, DBV0005A	Texas Instruments	SN6501DBVR
U4, U5	Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems, DCK0005A (SOT-5)	Texas Instruments	TLV6001IDCKR
R1, R2, R3	Not Installed		

6.2 Schematic

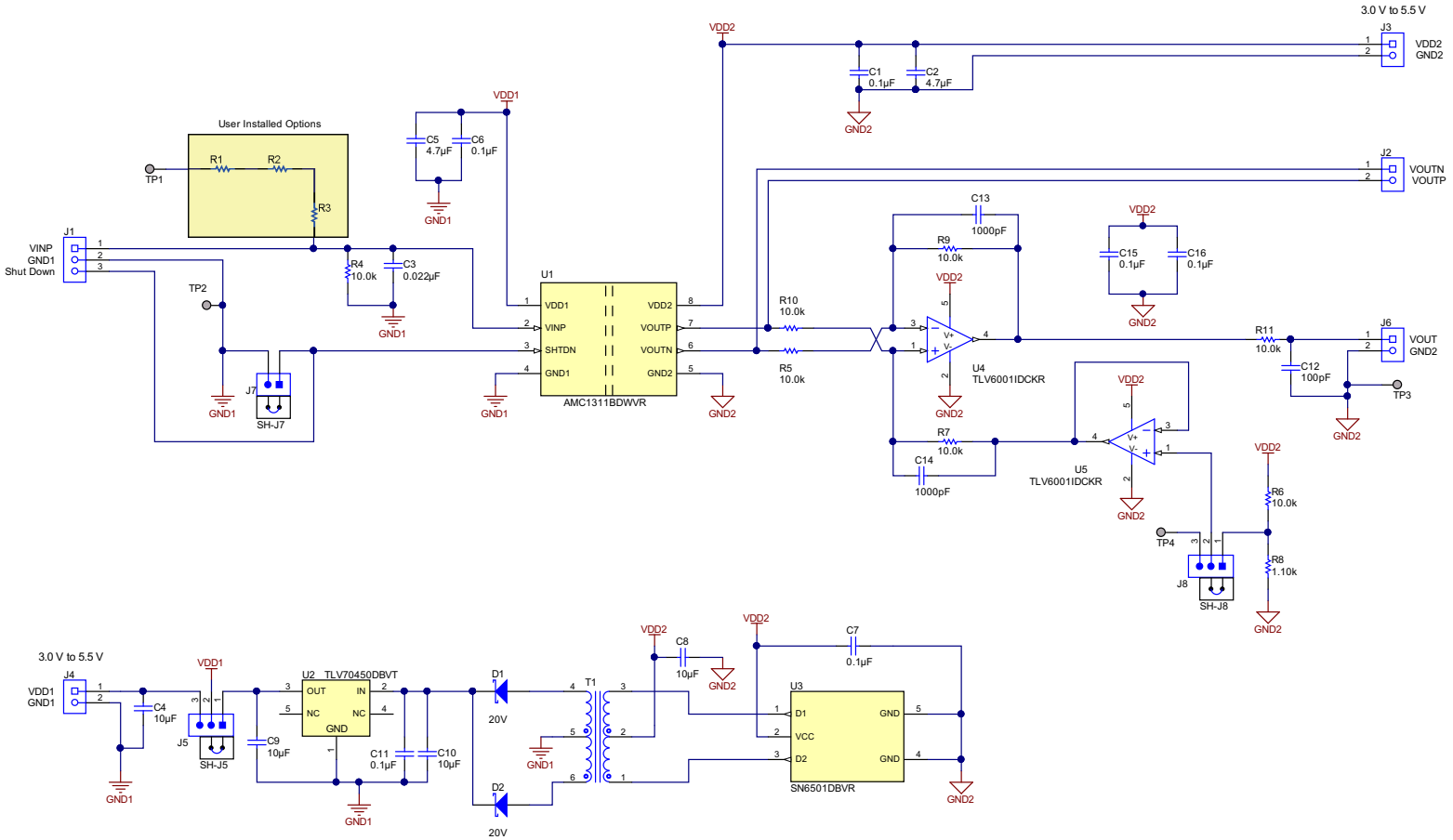

Figure 6. AMC1311EVM Schematic

7 Related Documentation

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, please identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com/.

- AMC1311 Precision, 2-V Input, Reinforced Isolated Amplifier, SBAS786
- SN6501 Transformer Driver for Isolated Power Supplies, SLLSEA0
- TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Op Amp for Cost-Sen, SBOS779

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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