

# MSP430FW423 Device Erratasheet

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## 1 Functional Errata Revision History

Errata impacting device's operation, function or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
FLL3	✓	✓
PORT4		✓
PORT5		✓
PORT7		✓
SIF1	✓	✓
SIF2	✓	✓
SIF3	✓	✓
SIF4	✓	✓
TA12	✓	✓
TA16	✓	✓
TA21	✓	✓
TAB22	✓	✓
WDG2	✓	✓
XOSC9	✓	✓

## 2 Preprogrammed Software Errata Revision History

Errata impacting pre-programmed software into the silicon by Texas Instruments.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Software in ROM errata.

## 3 Debug only Errata Revision History

Errata only impacting debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
EEM20	✓	✓

## 4 Fixed by Compiler Errata Revision History

Errata completely resolved by compiler workaround. Refer to specific erratum for IDE and compiler versions with workaround.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev C
<a href="#">CPU4</a>	✓	✓

Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

**TI MSP430 Compiler Tools (Code Composer Studio IDE)**

- [MSP430 Optimizing C/C++ Compiler](#): Check the --silicon\_errata option
- [MSP430 Assembly Language Tools](#)

**MSP430 GNU Compiler (MSP430-GCC)**

- [MSP430 GCC Options](#): Check -msilicon-errata= and -msilicon-errata-warn= options
- [MSP430 GCC User's Guide](#)


**IAR Embedded Workbench**

- [IAR workarounds for msp430 hardware issues](#)

## 5 Package Markings

### PM64

### LQFP (PM), 64 Pin

 NNNNNNN <u>G4</u>  M430Fxxxx REV # ○	# = Die revision ○ = Pin 1 location N = Lot trace code
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## 6 Detailed Bug Description

### CPU4 *CPU Module*

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**Category** Compiler-Fixed

**Function** PUSH #4, PUSH #8CPU4 - Bug

**Description** The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

**Workaround** Refer to the table below for compiler-specific fix implementation information.

IDE/Compiler	Version Number	Notes
IAR Embedded Workbench	IAR EW430 v2.x until v6.20	User is required to add the compiler flag option below. --hw_workaround=CPU4
IAR Embedded Workbench	IAR EW430 v6.20 or later	Workaround is automatically enabled
TI MSP430 Compiler Tools (Code Composer Studio)	v1.1 or later	
MSP430 GNU Compiler (MSP430-GCC)	MSP430-GCC 4.9 build 167 or later	

### EEM20 *EEM Module*

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**Category** Debug

**Function** Debugger might clear interrupt flags

**Description** During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

**Workaround** None.

### FLL3 *FLL+ Module*

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**Category** Functional

**Function** FLLDx = 11 for /8 may generate an unstable MCLK frequency

**Description** When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g. averaged over 2sec) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

**Workaround** None

### PORT4 *PORT Module*

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**Category** Functional

<b>Function</b>	SIF clock output depends on P2.7 AND P3.0
<b>Description</b>	The SIF - clock output is not available at port P2.7 when setting P2.7 as secondary function and output as described in data sheet
<b>Workaround</b>	Also set P3.0 to alternate function and output. The SIF clock signal is then available at P2.7.

## **PORT5** *PORT Module*

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<b>Category</b>	Functional
<b>Function</b>	SIF comparator output is not available at P6.3
<b>Description</b>	The SIF comparator output is not available at port P6.3 when setting P6.3 as secondary function and output as described in data sheet
<b>Workaround</b>	None

## **PORT7** *PORT Module*

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<b>Category</b>	Functional
<b>Function</b>	SIFDAC output function not available at P6.6
<b>Description</b>	The SIFDAC output is not available at port P6.6 when setting P6.6 as secondary function and output as described in data sheet
<b>Workaround</b>	None

## **SIF1** *SCANIF Module*

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<b>Category</b>	Functional
<b>Function</b>	SIFCLK and MCLK dependency
<b>Description</b>	When the CPU clock source MCLK is faster than the SIF clock source SIFCLK, the PSM processing state-machine output register can become corrupted and result in incorrect SIFCNT operation.
<b>Workaround</b>	None. Ensure that the MCLK frequency is slower than or equal to the frequency of SIFCLK.

## **SIF2** *SCANIF Module*

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<b>Category</b>	Functional
<b>Function</b>	SIFACLK and TSM0 dependency
<b>Description</b>	When the SIFACLK bit for the TSM0 state is set, the behavior of the TSM state machine can be unpredictable.
<b>Workaround</b>	Don't set SIFACLK in TSM0. This shortens the duration of the TSM0 state only. If the duration of TSM0 is of concern for an application, insert a dummy state at TSM0 with a

cleared SIFACLK bit and use TSM1 as the first valid user state.

**SIF3**
**SCANIF Module**


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**Category**

Functional

**Function**

Bit SIFCACI3 cleared results in unexpected signal value if SIFCI is configured as input

**Description**

When SIFCI is configured as input for Scan IF by setting SIFCISEL bit, SIFCACI3 bit should be a don't care. However, clearing it will cause wrong scanned signal value.

**Workaround**

Set SIFCACI3 Bit (in SIFCTL2 register) if SIFCI is configured as input for Scan IF.

**SIF4**
**SCANIF Module**


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**Category**

Functional

**Function**

Unpredictable CPU behavior if SMCLK (DCO) is used by SCAN IF and interrupts are enabled

**Description**

If the SCAN module is configured using the SMCLK (DCO) while CPU is in LPMx and any interrupt is enabled, unexpected short pulses of DCO clock (visible on MCLK) might occur. This rare scenario is triggered if an interrupt is fired during a small time window (hundreds of ps) after the Timing State Machine (TSM) of SCAN IF is releasing its clock request. Because of unexpected short pulses on MCLK, the behavior of CPU is unpredictable potentially leading to a non-responding device.

**Workaround**

Use the SCAN IF internal oscillator instead of SMCLK as the clock source for SCAN IF.

**TA12**
**TIMER\_A Module**


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**Category**

Functional

**Function**

Interrupt is lost (slow ACLK)

**Description**

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer\_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

**Workaround**

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

**TA16**
**TIMER\_A Module**


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**Category**

Functional

**Function**

First increment of TAR erroneous when IDx > 00

**Description**

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

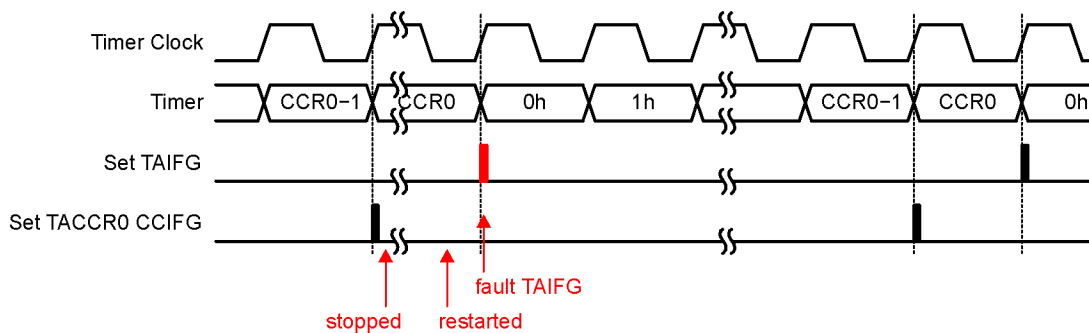
**Workaround** None

**TA21** *TIMER\_A Module*

**Category** Functional

**Function** TAIFG Flag is erroneously set after Timer A restarts in Up Mode

**Description** In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLK bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



**Workaround** None.

**TAB22** *TIMER\_A/TIMER\_B Module*

**Category** Functional

**Function** Timer\_A/Timer\_B register modification after Watchdog Timer PUC

**Description** Unwanted modification of the Timer\_A/Timer\_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer\_A/Timer\_B counter register TACCRx/TBCCRx is incremented/decremented (Timer\_A/Timer\_B does not need to be running).

**Workaround** Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

**WDG2** *WDT Module*

**Category** Functional

<b>Function</b>	Incorrectly accessing a flash control register
<b>Description</b>	If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to the expected PUC.
<b>Workaround</b>	None
<b>XOSC9</b>	<b><i>XOSC Module</i></b>
<b>Category</b>	Functional
<b>Function</b>	XT1 Oscillator may not function as expected in HF mode
<b>Description</b>	XT1 oscillator does not work correctly in high frequency mode at supply voltages below 2.0V with crystal frequency > 4MHz.
<b>Workaround</b>	None. When XT1 oscillator is used in HF mode with crystal frequency > 4MHz ensure a supply voltage > 2.2V.



## 7 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Revision D was removed

Changes from device specific erratasheet to document Revision A.

1. Errata EEM20 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Errata SIF4 was added to the errata documentation.

Changes from document Revision C to Revision D.

1. Package Markings section was updated.

Changes from document Revision D to Revision E.

1. TA21 Description was updated.

Changes from document Revision E to Revision F.

1. Function for CPU4 was updated.
2. Workaround for CPU4 was updated.

Changes from document Revision F to Revision G.

1. Erratasheet format update.
2. Added errata category field to "Detailed bug description" section

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